

FAST VISUAL TARGET IDENTIFICATION FOR LOW-COST BCI SPELLER

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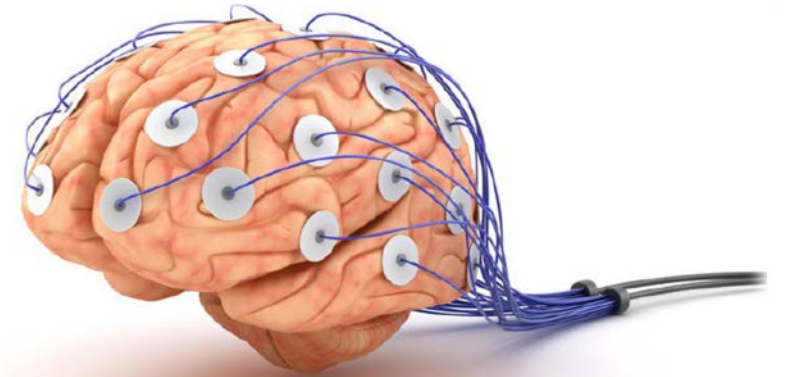
²Chungnam National University

⁴Ewha Womans University



OUTLINE

- What is the brain-computer interface?
- Research goal
- Previously developed wearable BCI device
- Proposed target identification algorithm
- Experimental results
- Further work – make our own hardware
- Conclusion



BRAIN-COMPUTER INTERFACE

- Brain-Computer Interface (BCI) - emerging communication channel for humans



Jan Scheuermann, DARPA



Courtesy Georgia Tech BrainLAB



Samsung



Lyon Neuroscience Research Center, 2012

BRAIN-COMPUTER INTERFACE

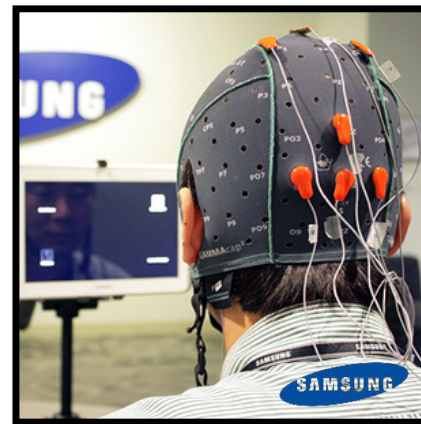
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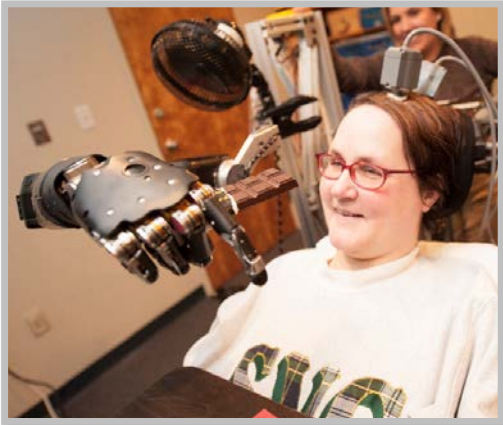
Lyon Neuroscience Research Center, 2012

Invasive

Non-invasive

BRAIN-COMPUTER INTERFACE

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Lyon Neuroscience Research Center, 2012

BCI Speller

BRAIN-COMPUTER INTERFACE

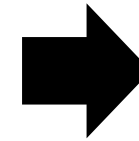
- Brain-Computer Interface (BCI) - emerging communication channel for humans



Graffiti artist, Tempt



Physicist, Hawking



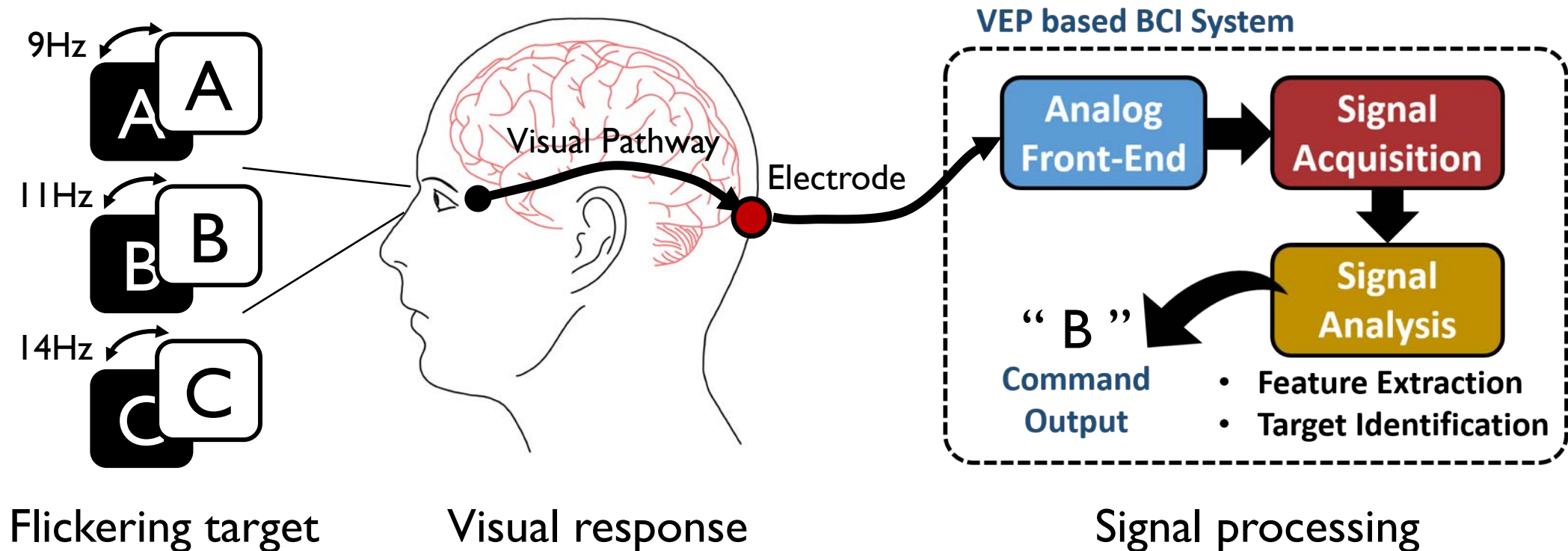
Lyon Neuroscience Research Center

BCI Speller

- Can help patients with paralysis **communicate with other people** (stroke, spinal cord injury, ...)
- Using non-invasive electroencephalogram (EEG)
→ non-invasiveness, simple operation

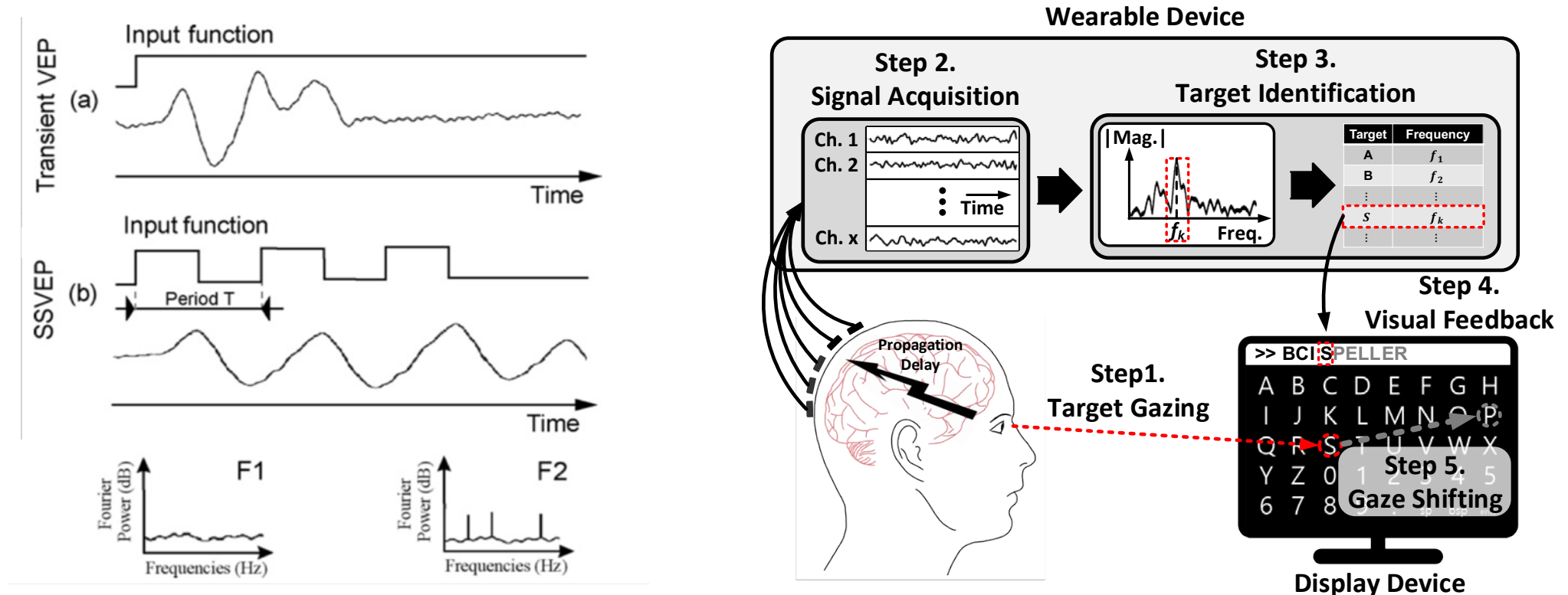
STEADY-STATE VISUAL EVOKED POTENTIAL

- Information transfer through visual evoked potentials (VEPs)
 - SSVEP: EEG response to flickering visual stimulation at a specific frequency



VISUAL TARGET IDENTIFICATION IN BCI SPELLER

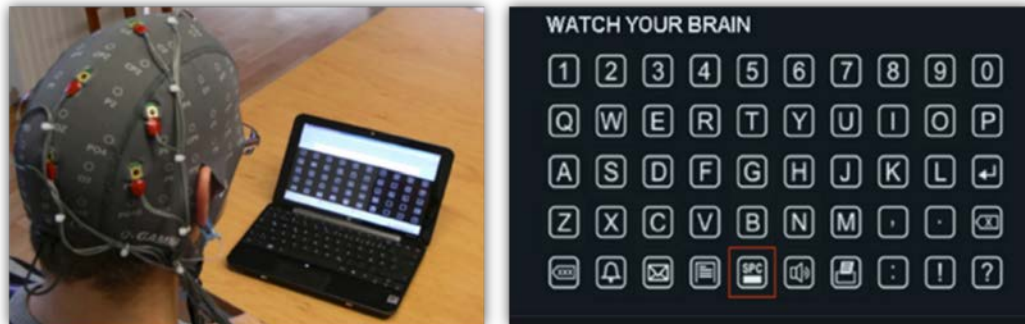
- Information transfer through visual evoked potentials (VEPs)
 - SSVEP: EEG response to flickering visual stimulation at a specific frequency



RESEARCH GOAL


Previous BCI speller system

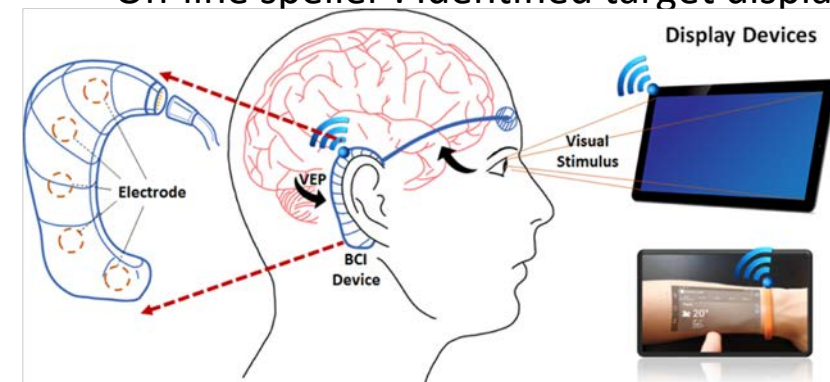
- Attaching many electrodes on the head
 - Discomfort to wear
 - Long preparation/setup time
- EEG signal processing in PC
 - Need powerful computing resource



Previous BCI speller system

Goal : Wearable BCI speller system

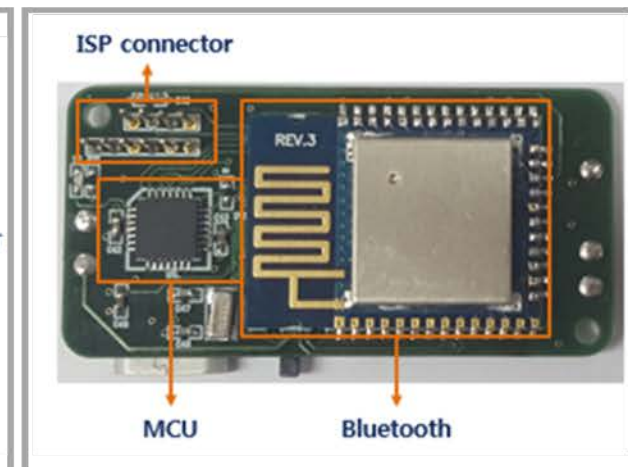
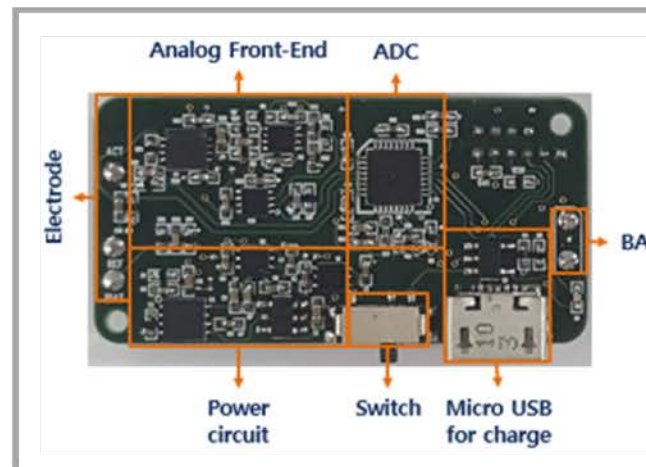
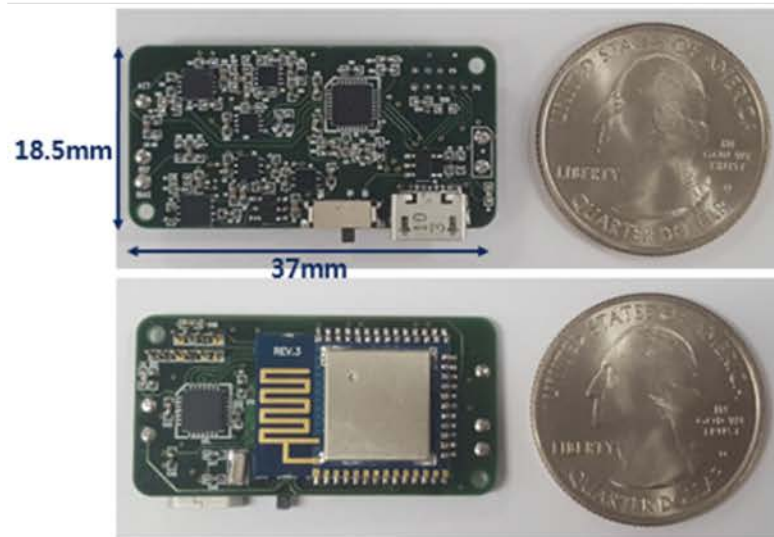
- BCI device with better wearability
 - Support on-device EEG processing
 - Based on Low-power MCU platform
- Display device with  **Bluetooth**
 - Target character display : visual stimulus
 - On-line speller : Identified target display



Wearable BCI speller system

WEARABLE BCI DEVICE PROTOTYPE

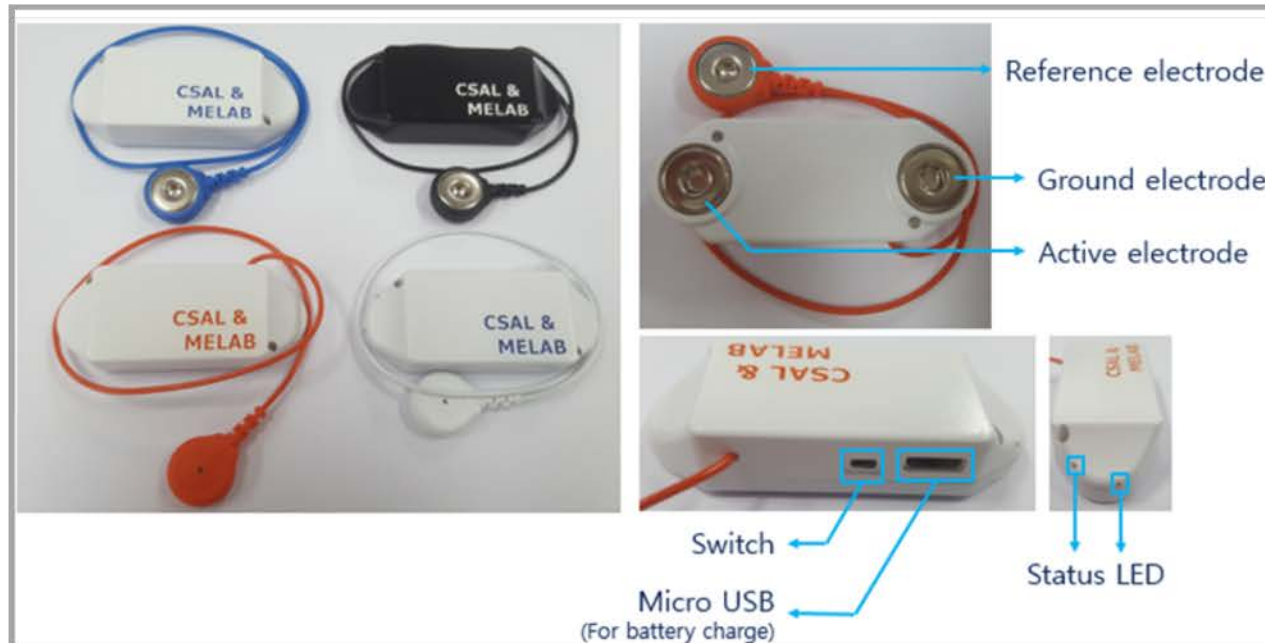
- Behind-the-ear type device
 - Single-channel EEG + Bluetooth 4.0
 - Target identification software on host PC (EEG data transfer through Bluetooth)
 - 24-bit resolution ADC chip (for performance evaluation)



Co-work with Seoul National University (SNU)

WEARABLE BCI DEVICE PROTOTYPE



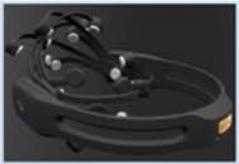

- Behind-the-ear type device
 - Single-channel EEG + Bluetooth 4.0
 - Target identification software on host PC (EEG data transfer through Bluetooth)
 - 24-bit resolution ADC chip (for performance evaluation)



IRB (Institutional Review Board) approved

COMPARISON TO COMMERCIAL DEVICES

- Small size & low power
 - Comfortable
 - Long battery life
- High performance
 - Low noise
 - High resolution
- But...
 - Requires powerful computing PC

	This Work	Neuroscan	EMOTIV EPOC	Neurosync	
					
Dimension (mm)	54 x 20 x 10	-	-	63 x 40 x 25	
Weight (g)	14.3	-	104.3	43	
Number of Ch.	1	64-512	14	1	
Sampling rate (SPS)	250 / 500	Up to 20,000	127	N/A	
ADC reference (V)	±2.42	Adjustable	N/A		
Amplification (V/V)	59,400	Adjustable	N/A		
Dynamic range	±40.74	Adjustable	8,400		
Noise level (µVrms)	0.11	0.5	about 1		
Resolution	24bit / 48.4nV	24bit / 3nV	14bit / 0.51µV		
Bandwidth (Hz)	1-35	DC-3,500	0.2-45		
Communication	Bluetooth 4.0	USB	2.4GHz		
Power	Li-polymer	Wall power	Li-polymer		AAA battery
Power consumption	19 hour		12 hour		N/A

IMPROVEMENT DIRECTION OF PROTOTYPE DEVICE

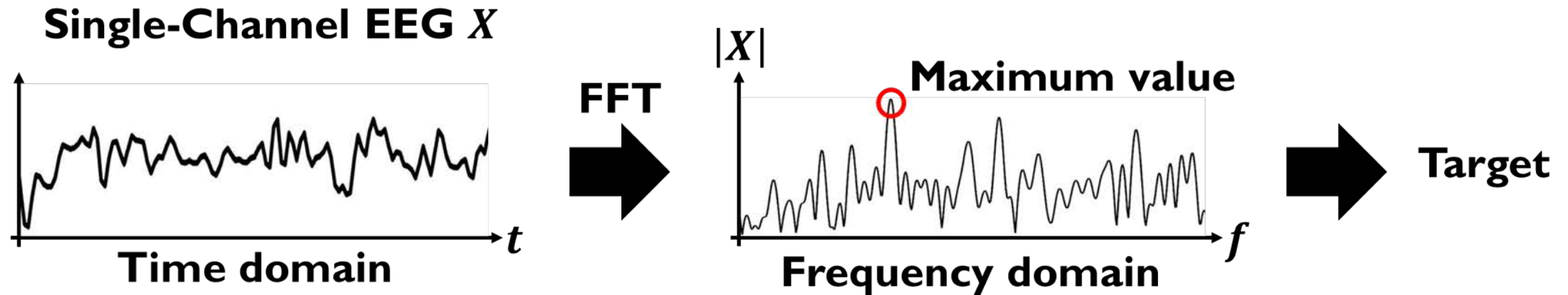
- **Not Enough SNR: Poor SSVEP quality at behind-the-ear position**
- **Not Enough Computing Power: Requires external computing device**
- **Not Enough Communication Speed**

IMPROVEMENT DIRECTION OF PROTOTYPE DEVICE

- **Not Enough SNR: Poor SSVEP quality at behind-the-ear position**
 - Move the electrode to back of the head (occipital region, Oz)
- **Not Enough Computing Power: Requires external computing device**
 - Propose the target identification algorithm for low-cost MCU and small memory
 - Maintain the BCI speller performance with negligible accuracy loss
- **Not Enough Communication Speed**
 - Reduce the signal processing time especially the timing dependent procedures

TARGET IDENTIFICATION ALGORITHMS

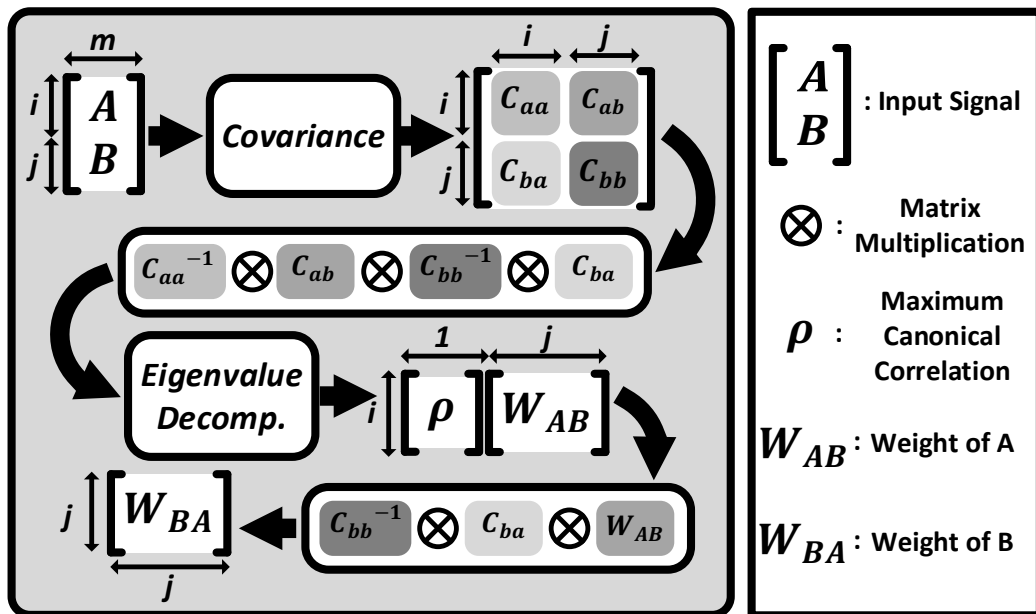
- PSDA (Power Spectral Density Analysis)
 - For single-channel SSVEP target identification
 - Simple operation: FFT & find maximum index
 - Weak performance for low SNR (signal-to-noise) SSVEP signal



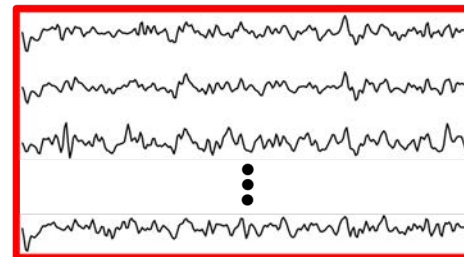
TARGET IDENTIFICATION ALGORITHMS

- Standard-CCA (Canonical Correlation Analysis)*
 - Correlation between EEG signal X and reference sinusoidal signal Y for each frequency
 - Should be computed for each target frequency \rightarrow Maximum correlation: target

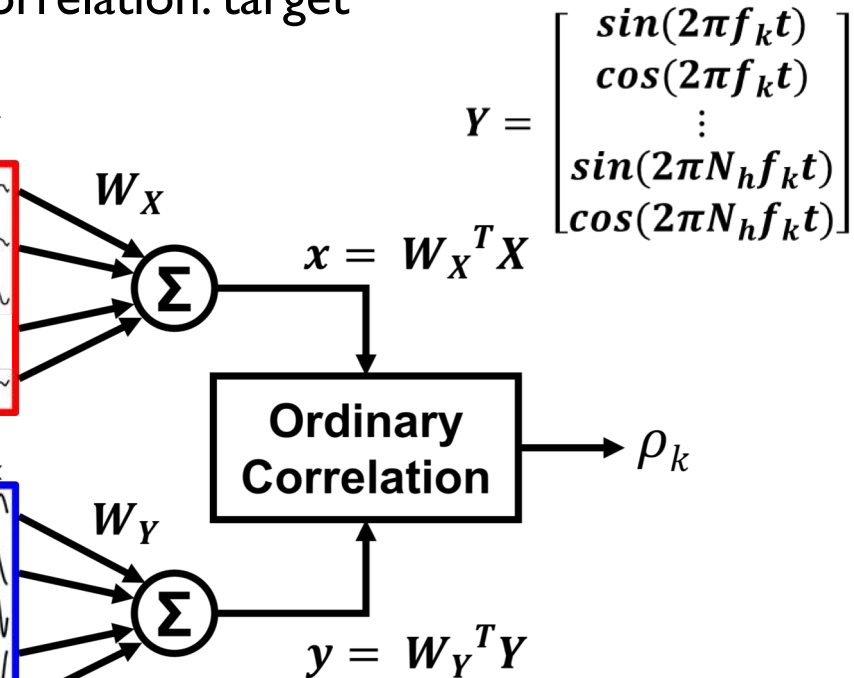
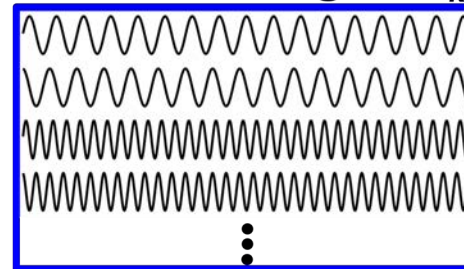
Canonical Correlation Analysis (CCA)



Multichannel EEG X

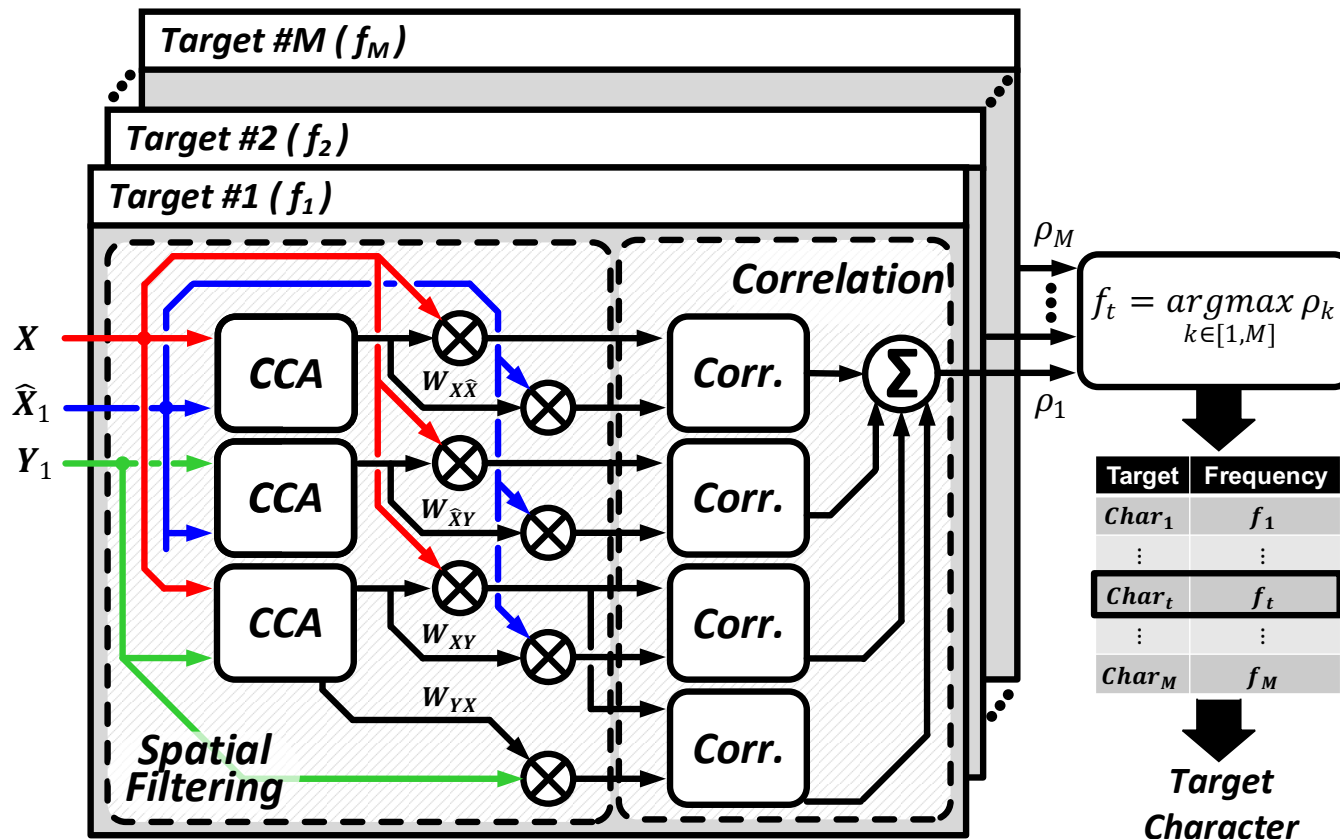


Reference Signal Y_k



TARGET IDENTIFICATION ALGORITHMS

- Combination-CCA (Comb-CCA)*



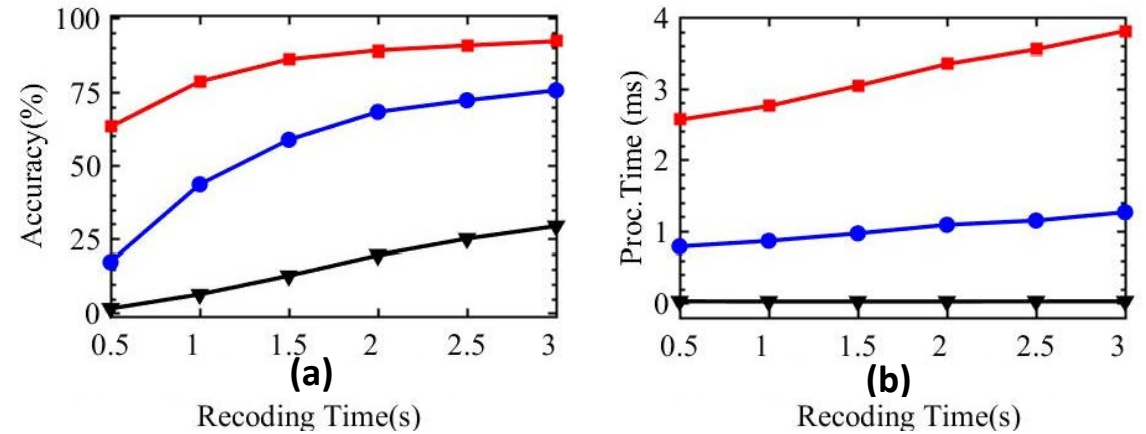
- User-specific target identification using training data \rightarrow more accurate!
- Uses three datasets
 - X : Input SSVEP signal set
 - \hat{X} : Training signal set (average of SSVEP)
 - Y : Reference sinusoidal signal set
- 3 CCA calculations & 4 correlations \rightarrow huge computational complexity

TARGET IDENTIFICATION COMPARISON

- Performance evaluation in terms of accuracy, processing time, and ITR (information transfer rate)

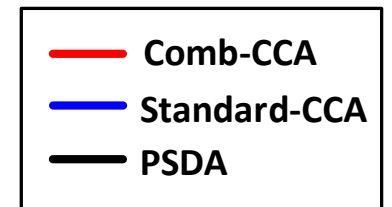
Algorithm	Performance	Complexity
Comb-CCA	High	High
Standard-CCA	Medium	Medium
PSDA	Low	Low

- Comb-CCA was chosen for the baseline algorithm in this research



$$ITR = \left(\log_2 N_f + P \log_2 P + (1 - P) \log_2 \left[\frac{1 - P}{N_f - 1} \right] \right) \times \left(\frac{60}{T} \right)$$

- P : classification accuracy
- T : average time for selection
- N_f : number of targets



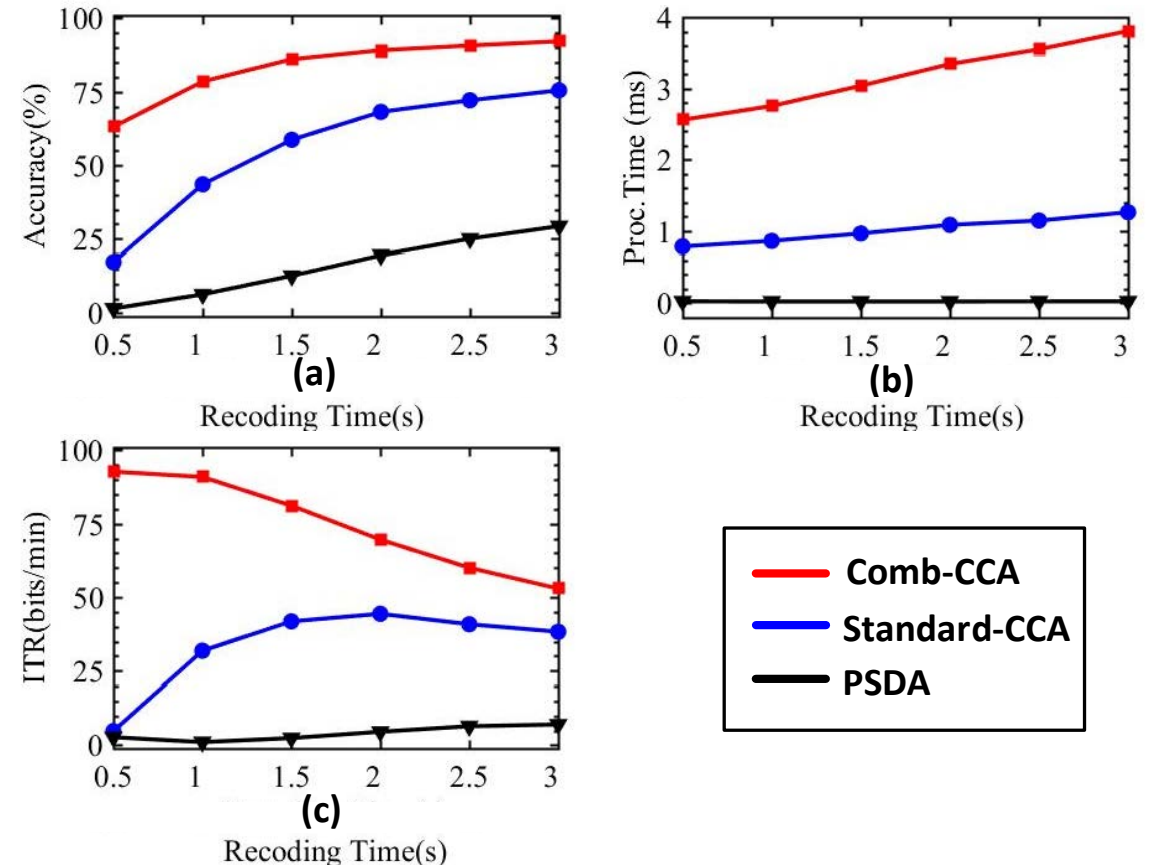
Performance comparison of target identification algorithms
(a) Accuracy, (b) Processing time (in PC), (c) ITR (Information Transfer Rate)

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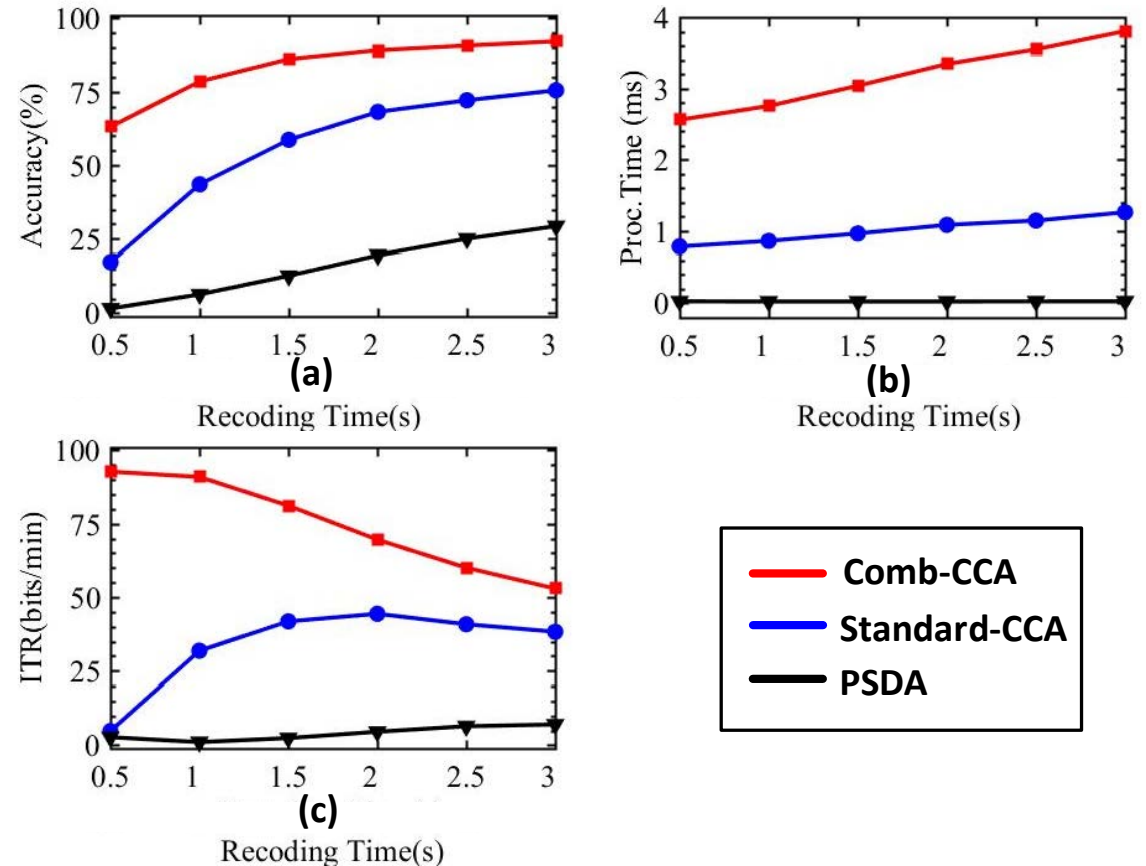
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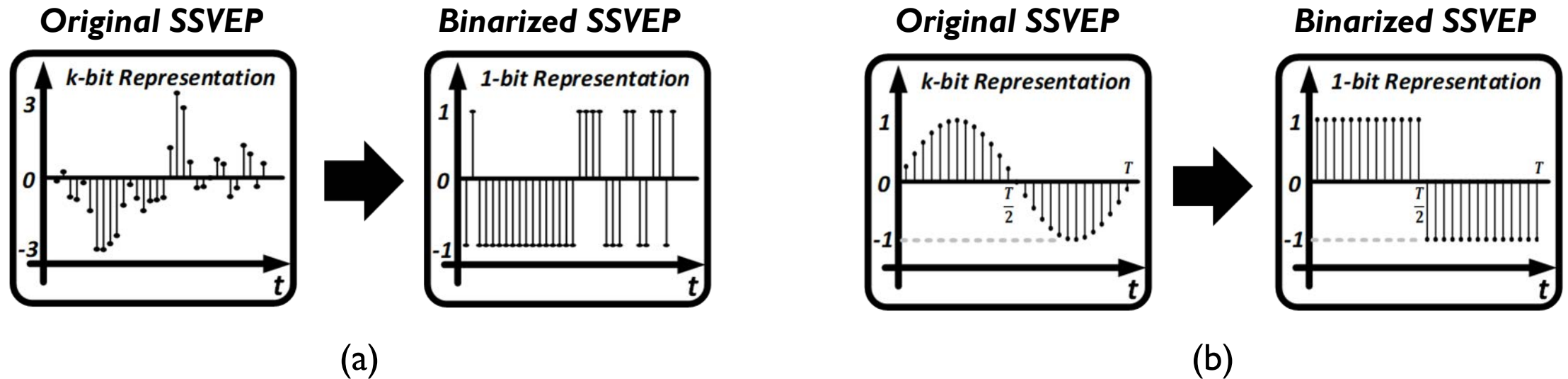


Performance comparison of target identification algorithms
 (a) Accuracy, (b) Processing time (in PC), (c) ITR (Information Transfer Rate)

PROPOSED ALGORITHM: CCA-LITE

- **Optimization method #1: Signal Binarization**

- Comb-CCA with multi-bit EEG & reference signal → **High computational complexity / memory**
- Comb-CCA with signal binarization → **Low computational complexity w/ negligible accuracy loss**
Low memory requirement



Proposed signal binarization concept for (a) EEG signal, (b) Reference sinusoidal signal

PROPOSED ALGORITHM: CCA-LITE

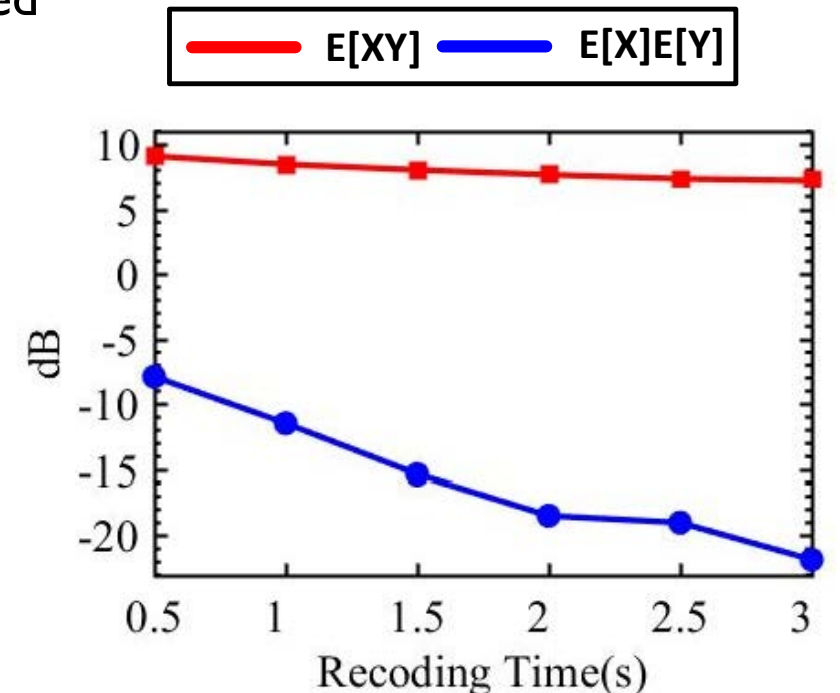
- **Optimization method #2: *On-the-fly* Covariance**

- $Cov(X, Y) = E[(X - E[X])(Y - E[Y])] = E[XY] - E[X]E[Y]$

PROPOSED ALGORITHM: CCA-LITE

- **Optimization method #2: On-the-fly Covariance**

- $Cov(X, Y) = E[(X - E[X])(Y - E[Y])] = E[XY] - E[X]E[Y] \approx E[XY]$
- If $E[XY] \gg E[X]E[Y]$ then $E[X]E[Y]$ can be ignored
 - In our application, $E[XY]$ more bigger than $E[X]E[Y]$



Comparison of $E[XY]$ and $E[X]E[Y]$

PROPOSED ALGORITHM: CCA-LITE

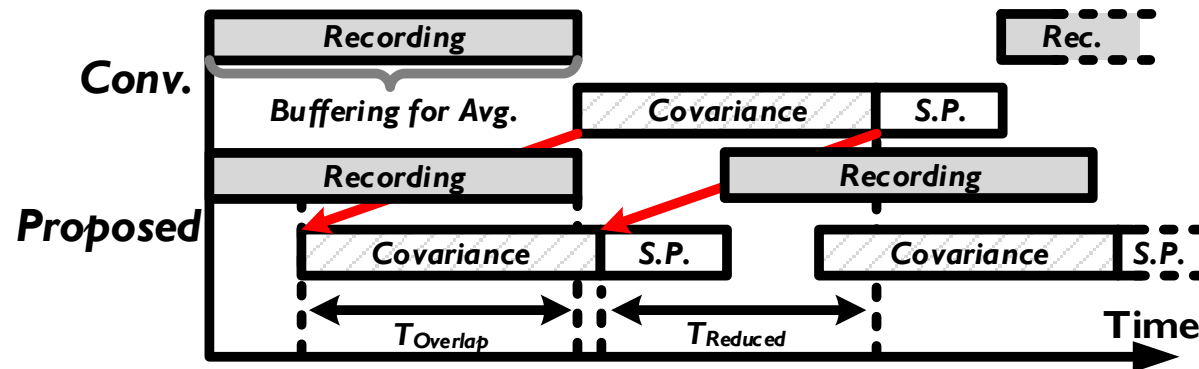
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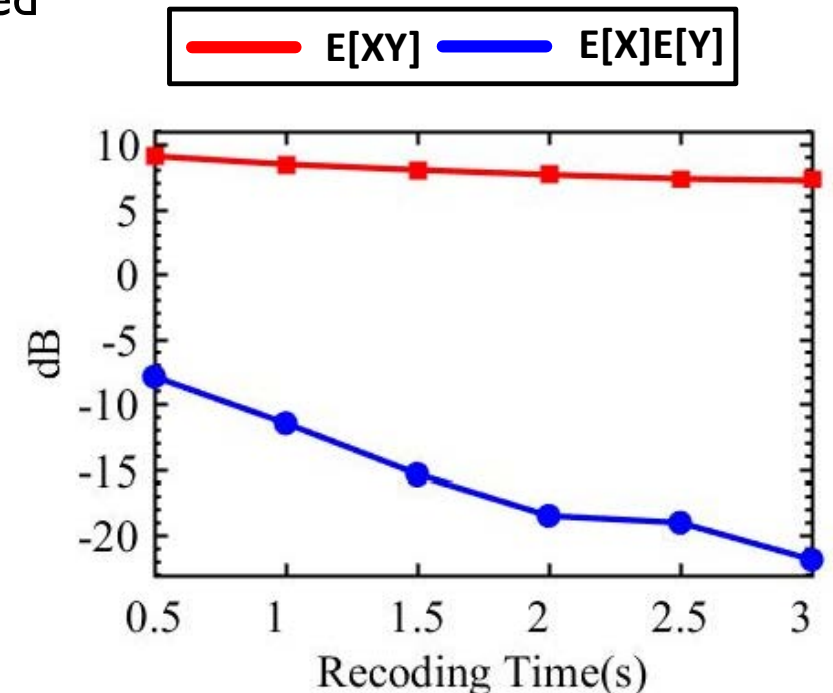
- If $E[XY] \gg E[X]E[Y]$ then $E[X]E[Y]$ can be ignored

- In our application, $E[XY]$ more bigger than $E[X]E[Y]$

- Covariance matrix calculation can be performed simultaneously with SSVEP recording



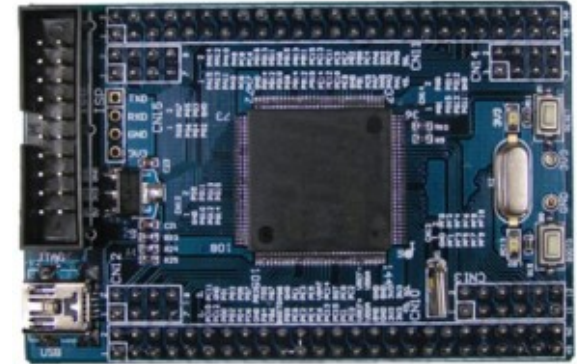
Advantage from *On-the-fly* Covariance Calculation



Comparison of $E[XY]$ and $E[X]E[Y]$

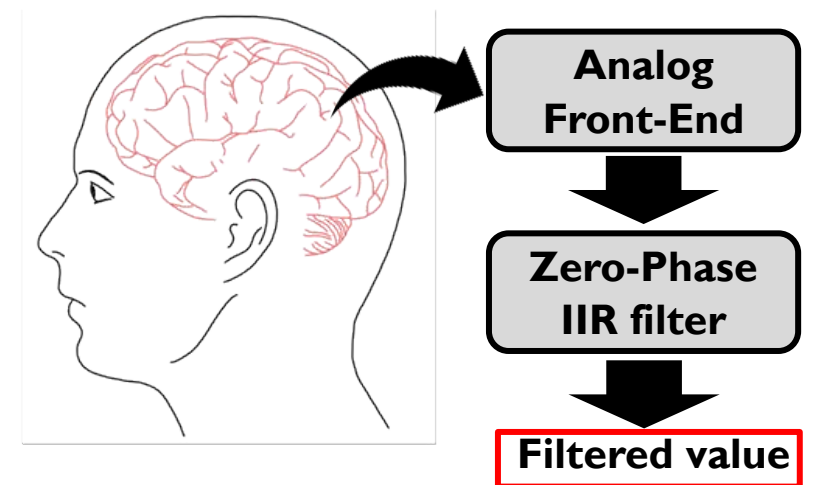
EXPERIMENTAL ENVIRONMENTS

- Low-power MCU platform
 - STM32F103ZET6 ARM MCU
 - ARM Cortex-M3 (Operating Frequency : 72MHz)
 - 512KB flash memory, 64KB SRAM



STM32F103ZET6 board

- Dataset Description *
 - EEG acquisition using *Biosemi's ActiveTwo*
 - ADC : 24-bit resolution
 - Sampling Frequency : 256Hz
 - Number of channel : 8 channels (We used Oz)
 - Recording Time : 4s
 - # of Target, # of subjects : 12 targets, 10 subjects

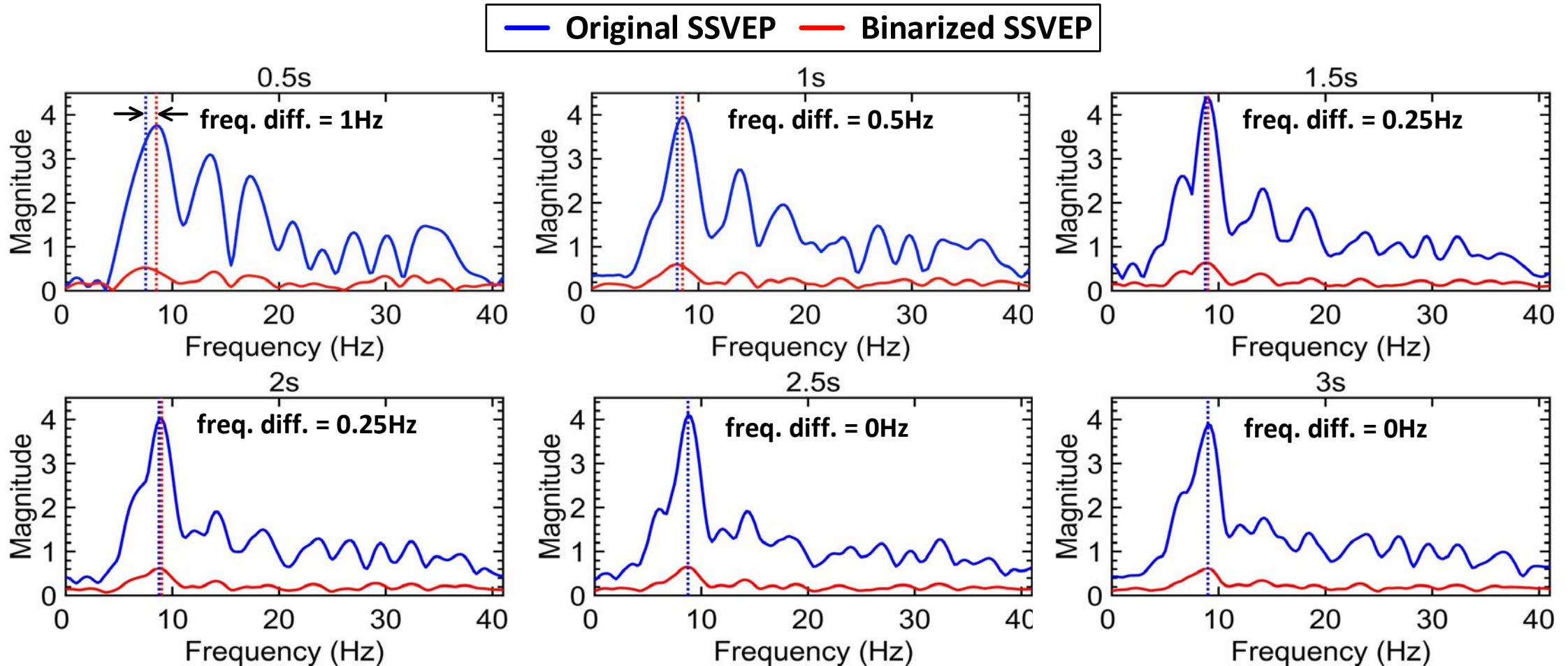


Pre-processing before writing the data file

EXPERIMENTAL RESULTS

- Subject #4
- Target: 9.25Hz

- Power spectrum of training signal according to the SSVEP recording length



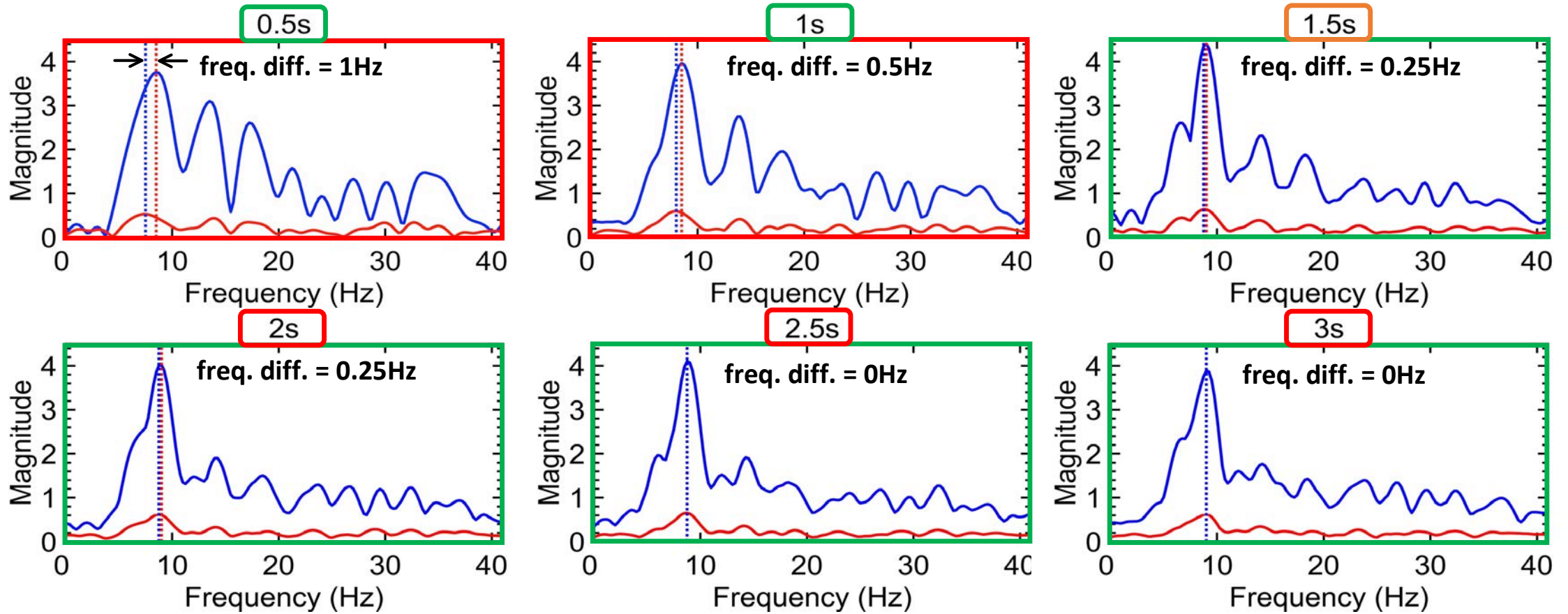
- Good
- Moderate
- Bad

EXPERIMENTAL RESULTS

- Subject #4
- Target: 9.25Hz

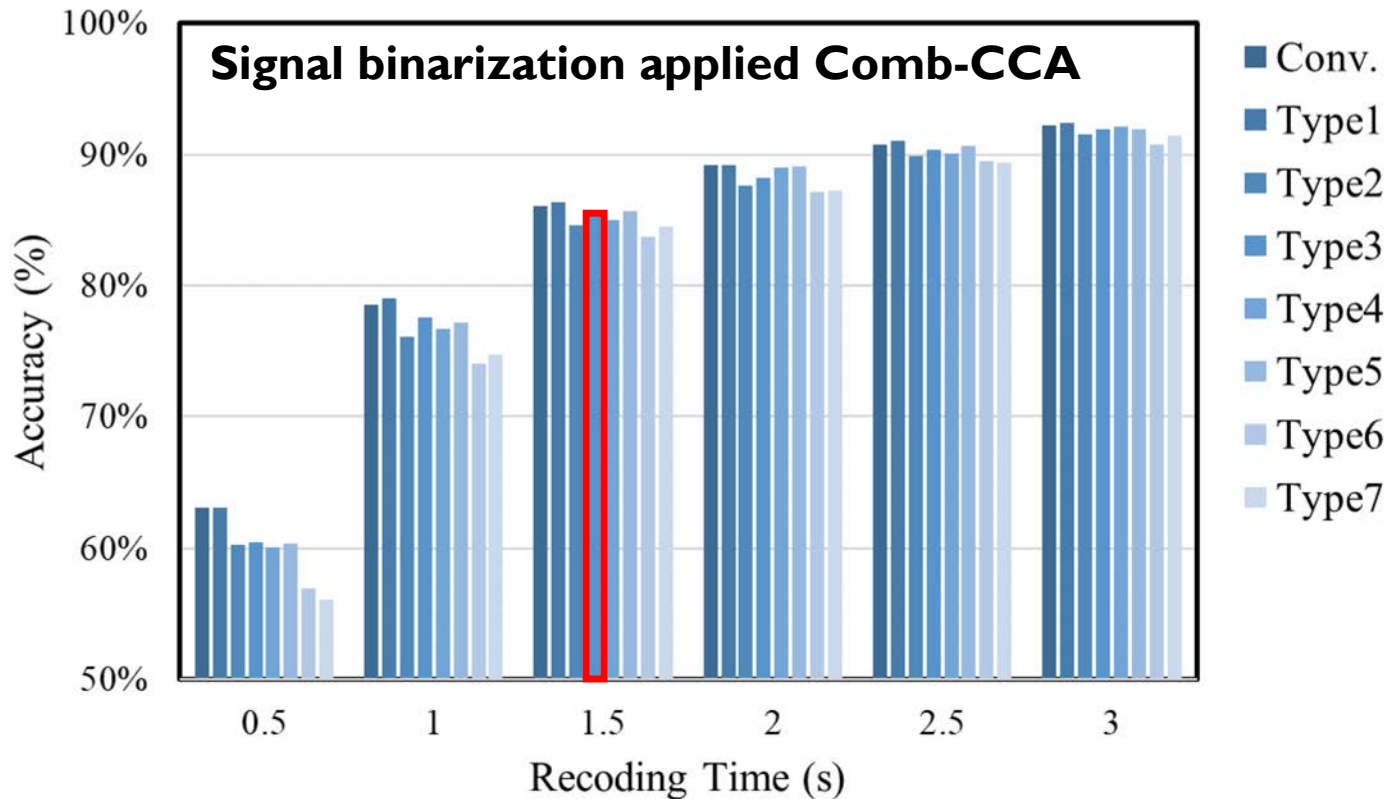
- Power spectrum of training signal according to the SSVEP recording length

— Original SSVEP — Binarized SSVEP



EXPERIMENTAL RESULTS

- Accuracy performance according to the combination of binarization application



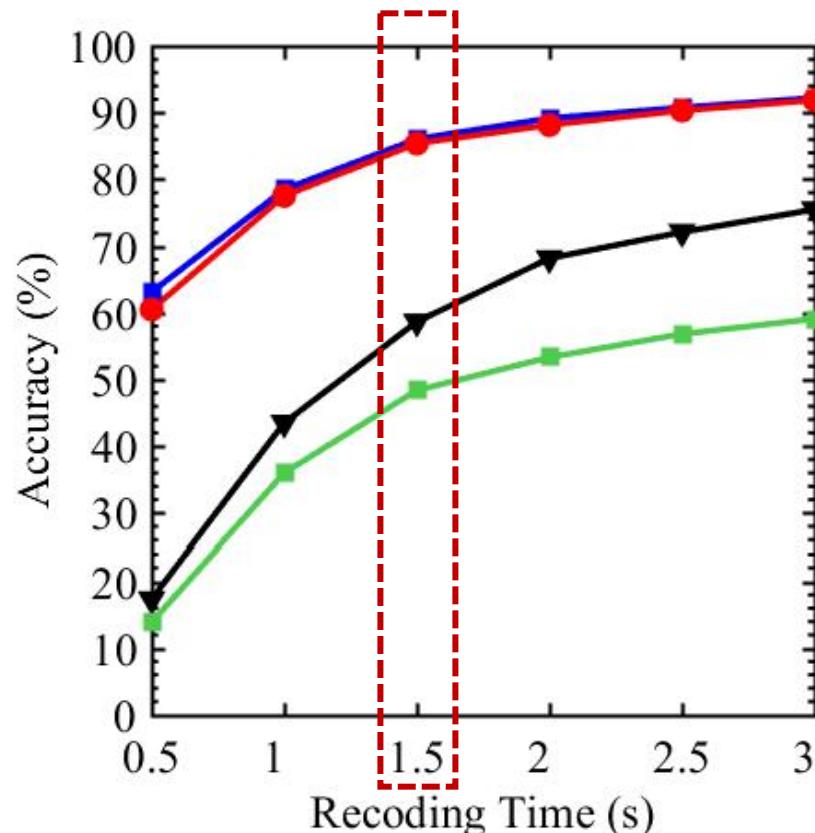
Type3: High accuracy with small memory requirement
 -- Training & Reference : pre-stored data

Type	Measured EEG	Training EEG	Reference Sinusoidal
Conv.	X	X	X
Type1	X	X	O
Type2	X	O	X
Type3	X	O	O
Type4	O	X	X
Type5	O	X	O
Type6	O	O	X
Type7	O	O	O

O: Signal binarization was applied
 X: Signal binarization was not applied

EXPERIMENTAL RESULTS

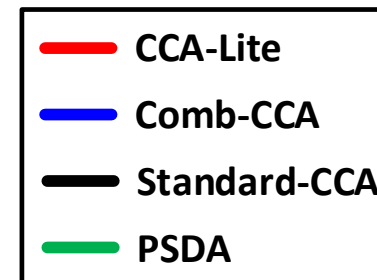
- Accuracy performance for various target identification algorithms
 - **CCA-Lite** : Comb-CCA + Signal Binarization (for Train & Ref.) + *on-the-fly* Covariance



Accuracy at 1.5s

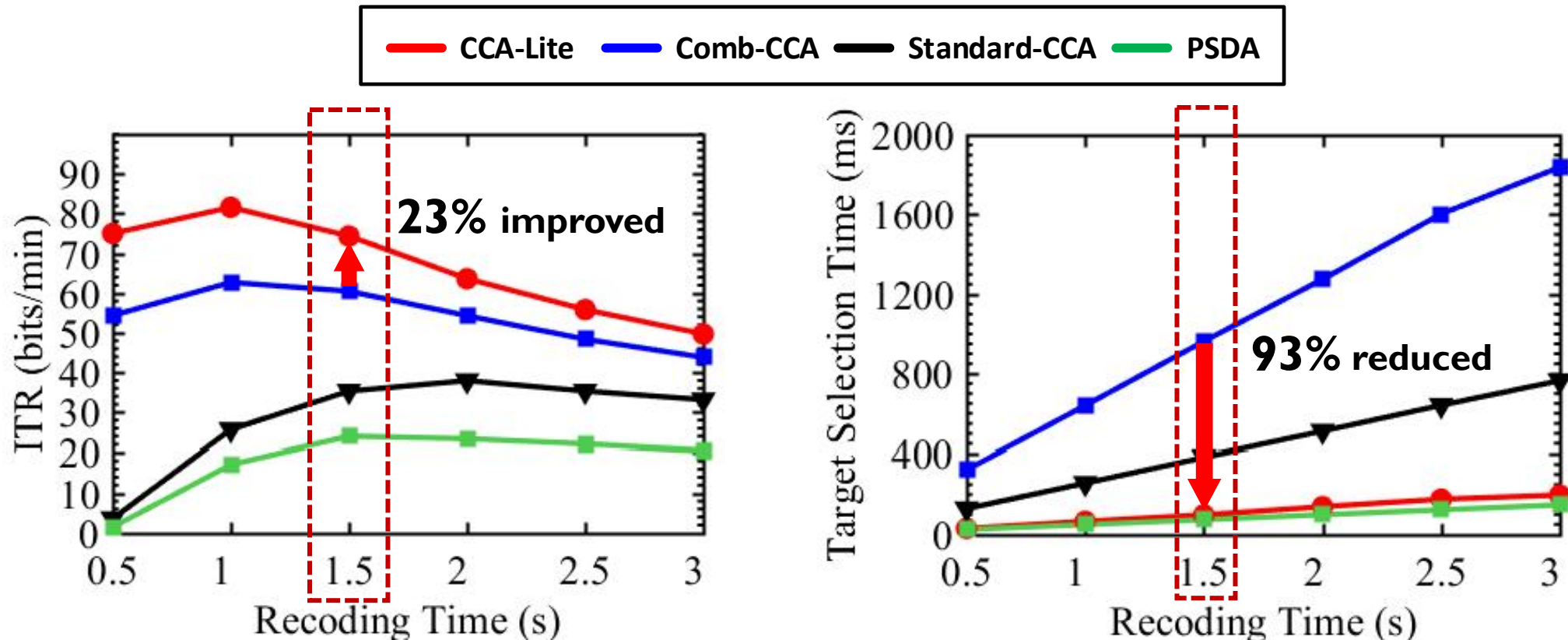
CCA-Lite	: 85.39%
Comb-CCA	: 86.06%
Standard-CCA	: 58.67%
PSDA	: 48.39%

} Negligible
Accuracy Loss



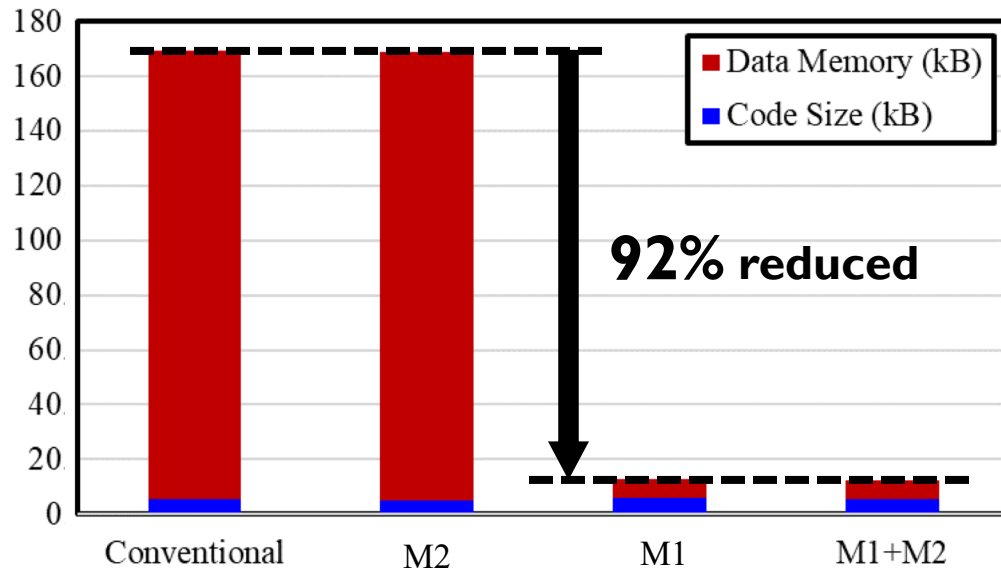
EXPERIMENTAL RESULTS

- Performance of target selection time & ITR (Information Transfer Rate)
 - Tested on Cortex-M3 based STM board (operating frequency: 72MHz)

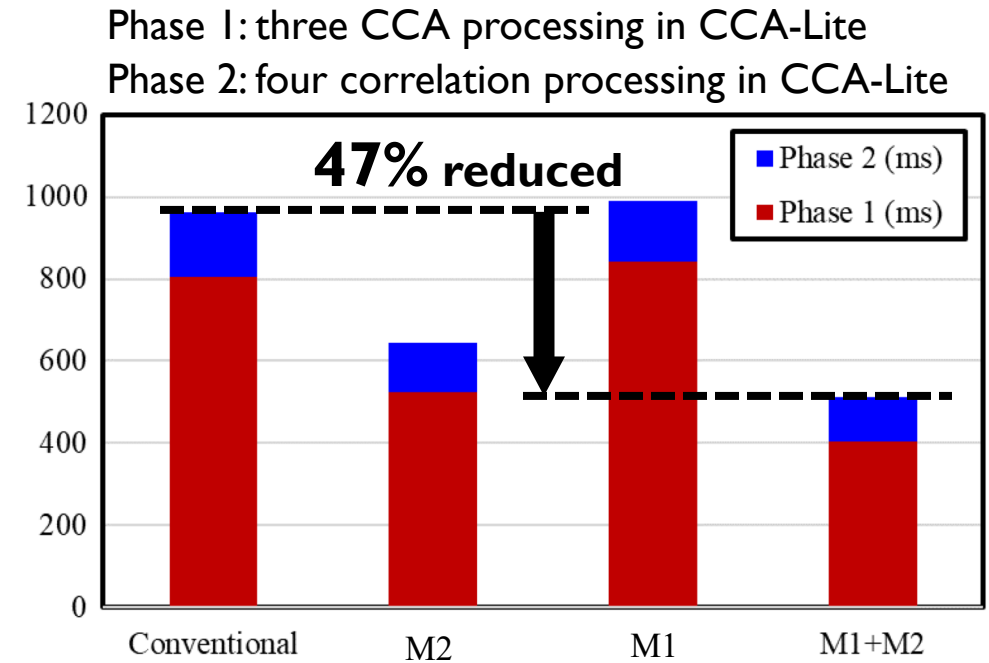


EXPERIMENTAL RESULTS

- CCA-Lite software performance evaluation on Cortex-M3
 - **M1**: Signal binarization applied Comb-CCA / **M2**: *on-the-fly* covariance applied Comb-CCA
 - **M1+M2**: proposed CCA-Lite



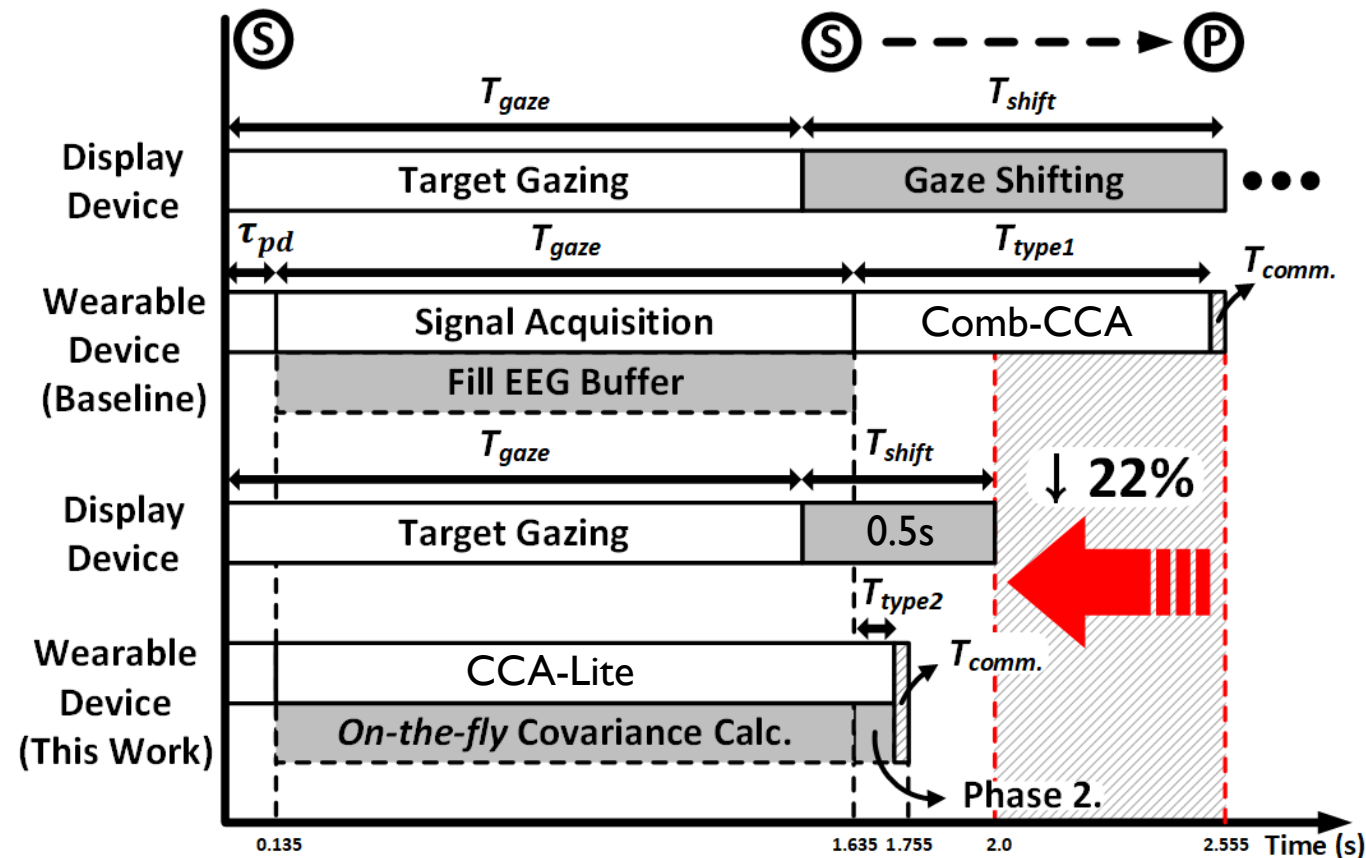
Memory footprint



Pure signal processing time on Cortex-M3 for single target identification

EXPERIMENTAL RESULTS

- Overall BCI speller system performance in terms of communication speed



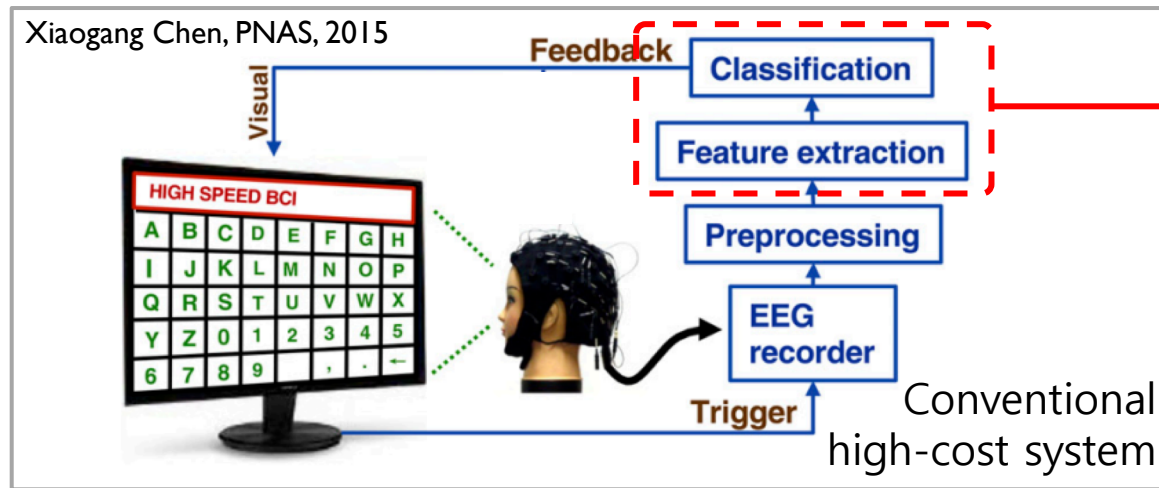
- Fixed target gazing time: 1.5s
- Minimum gaze shift time: 0.5s^{1,2)}
- Single target identification time
 - **22%** reduced !
 - Guaranteed gaze shift time 0.5s (signal processing will be done before the end of gaze shift time)

1) X. Chen et al, "High-speed spelling with a noninvasive brain-computer interface", PNAS, 2015

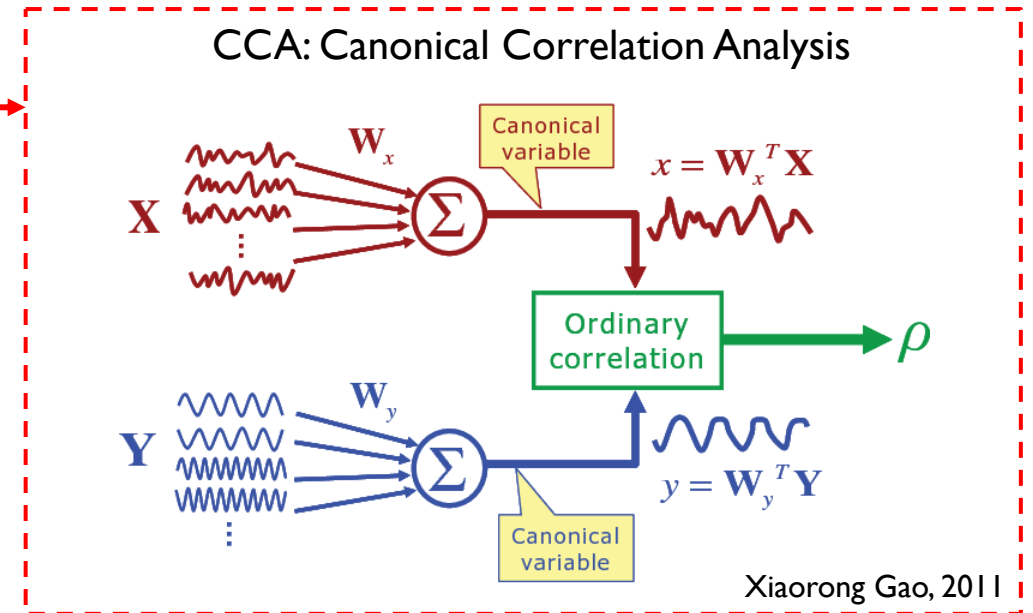
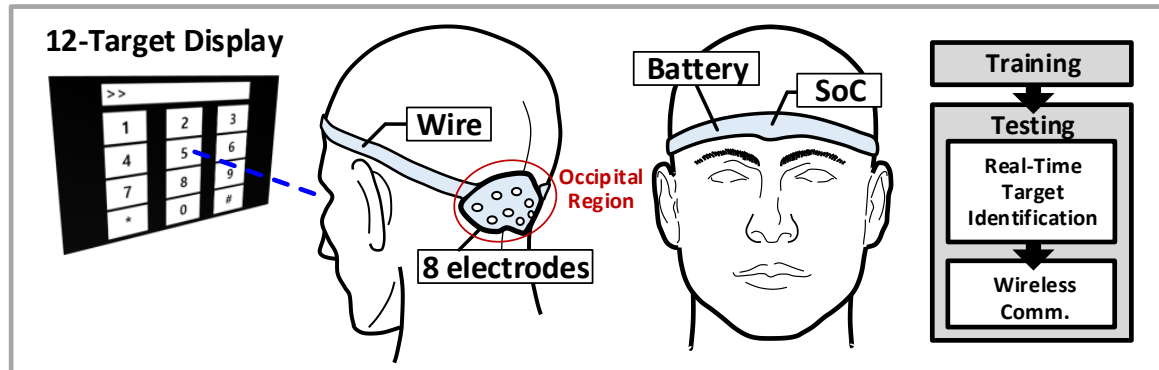
2) M. Nakanishi et al, "Enhancing Detection of SSVEPs for a High-Speed Brain Speller Using Task-Related Component Analysis", IEEE TBME, 2018

REUSABLE MATRIX ARITHMETIC ARCHITECTURE

- SSVEP-based Target Identification SoC with Highly Reusable 8x8 QRD



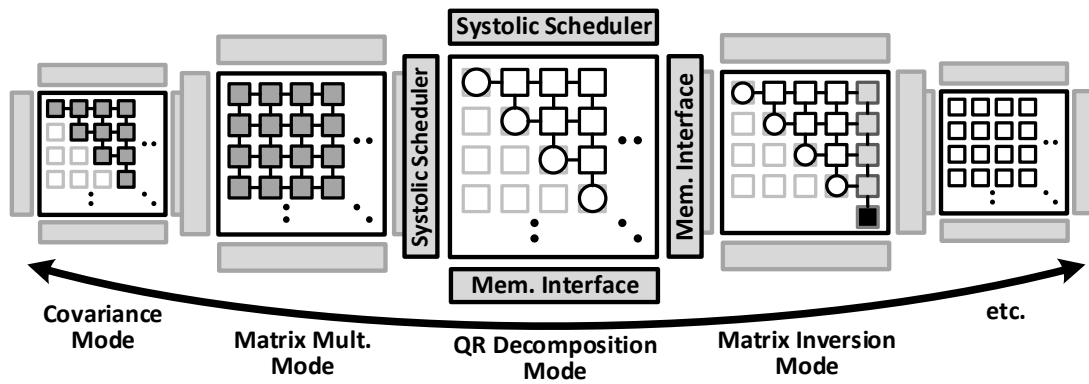
wearable system



- CCA finds the weights W_x, W_y which gives the largest correlation between X and Y (target frequency identification)
- We use CCA-Lite consisting of three CCAs.
 - Requires QRD, Inverse, Covariance, Mult. ...

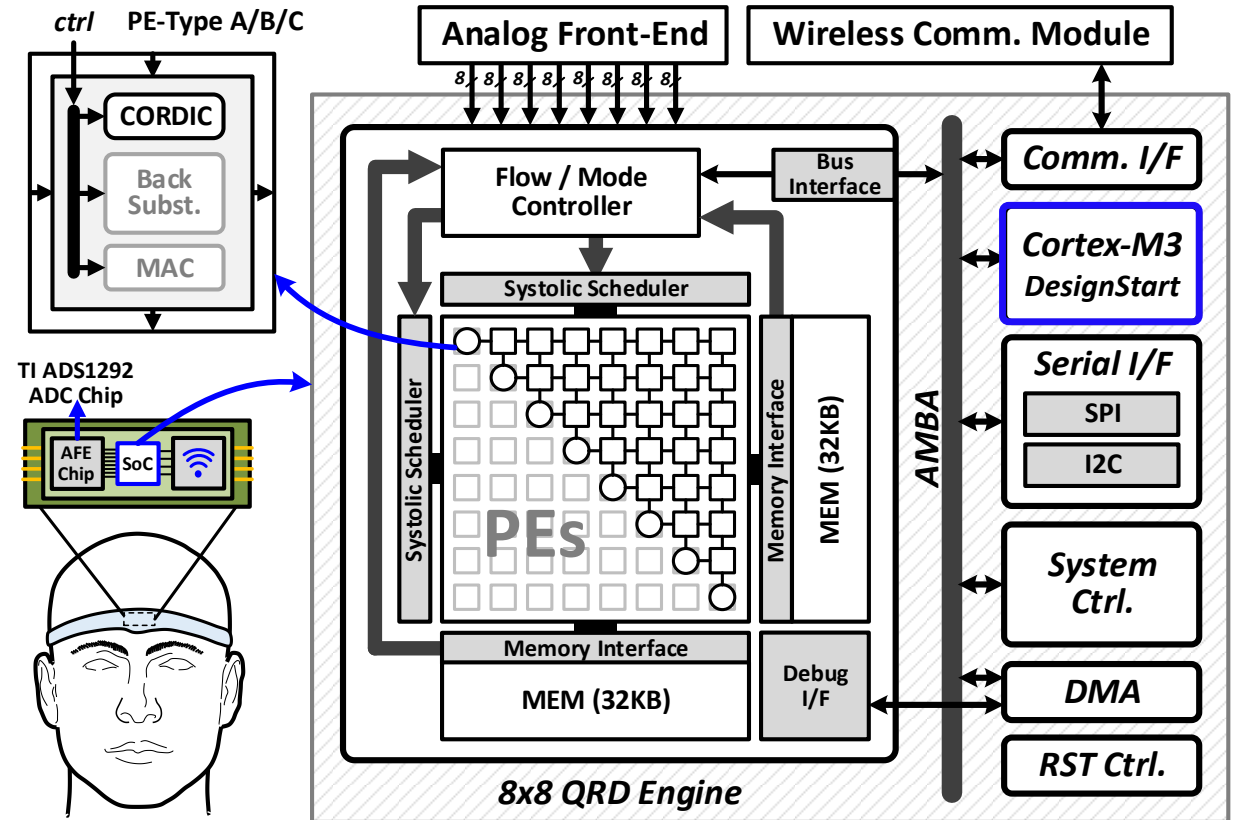
REUSABLE MATRIX ARITHMETIC ARCHITECTURE

- SSVEP-based Target Identification SoC with Highly Reusable 8x8 QRD
 - Systolic architecture based QR decomposition engine



- Same hardware, different operations → high reusability (covariance, mult, QRD, inversion, ...)
- “High throughput, reduced area & memory access, reduced power consumption” compared to same operations
- Target frequency identification on the low-cost edge devices.
- System implementation w/ AFE & Wireless Comm.

Optionally single chip



CONCLUSION

- **Research for patients with paralysis**
 - Low-cost wearable BCI system
- **Propose CCA-Lite for low-complexity target identification**
 - Target selection time reduction : **93%**
 - ITR (Information Transfer Rate) improvement : **23%**
 - Total performance improvement (for single target identification time) : **22%**
- **Further work - support multi-ch EEG processing for better accuracy**
 - SoC (System-on-chip) design with AFE (Analog Frontend) + dedicated hardware accelerator

THANK YOU

Any questions or comments -  jihoonkim@ewha.ac.kr