#### Post-Quantum Isogeny-based Cryptography on ARM processors

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ARM Research Summit 2018

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## Why Quantum Computing? Why now?

- The history of Integrated Circuits (IC)
  - 1958: First integrated circuit (1cm<sup>2</sup>, 2 transistors)
  - 1971: Moore's Law is born (2,300 transistors)
  - 2014: IBM P8 Processor, 16 cores (650mm<sup>2</sup>, > 4.2 billion transistors)
- Quantum Computers<sup>1</sup>









2015: 4-Qbit

2016: 8-Qbit

2018: 72-Qbit

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• Photon-based Quantum Computers are under construction!



<sup>1</sup>Pictures are taken from IBM Q Project

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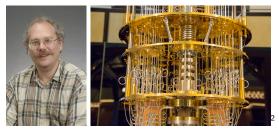
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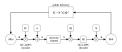
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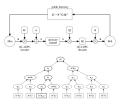


• Code-Based: McEliece

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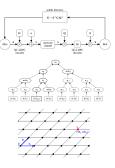


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• Lattice-Based: NTRU - LWE

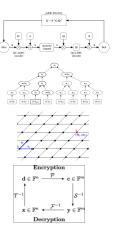


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• Multivariate: Rainbow Signatures

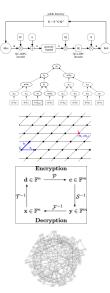


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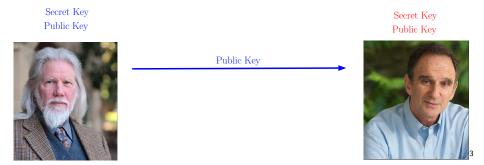
Secret Key Public Key



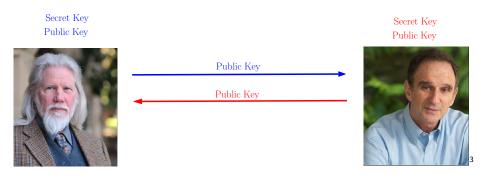
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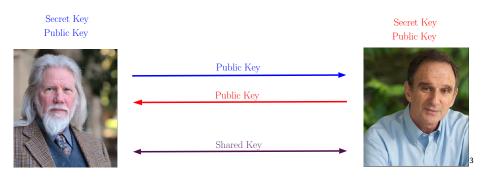
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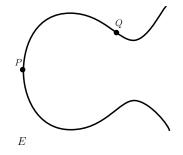


Figure: Classical Elliptic Curve Cryptography

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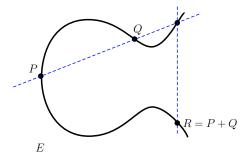


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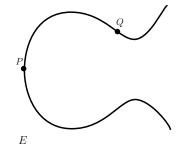


Figure: Post-Quantum Isogeny-based Cryptography

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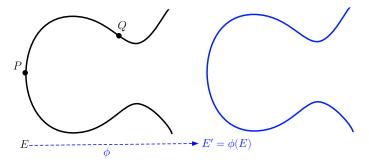


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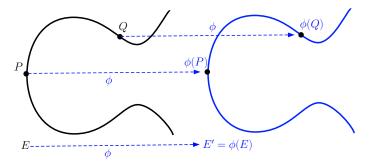


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• Supersingular Isogeny Key Encapsulation (SIKE) by Jao et al. submitted to NIST PQC Standardization 2017.

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Given  $P,Q\in E_1$  and  $\phi(P),\phi(Q)\in E_2$ , retrieve the secret isogeny map  $\phi$ 

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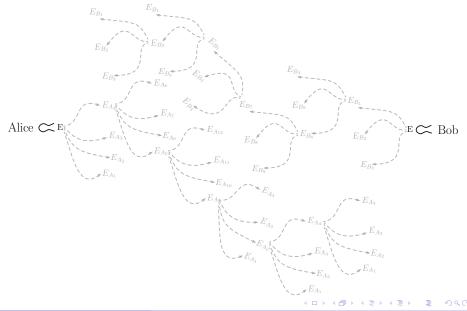
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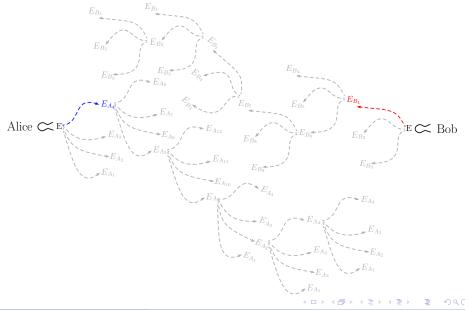
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- Claw finding algorithm complexity for SIKE and SIDH:
  - $\mathcal{O}(p^{1/6}) \rightarrow \mathsf{Quantum attacks}$
- The best known classical attack is based on meet in the middle
  - $\mathcal{O}(p^{1/4}) \rightarrow Classical attacks$

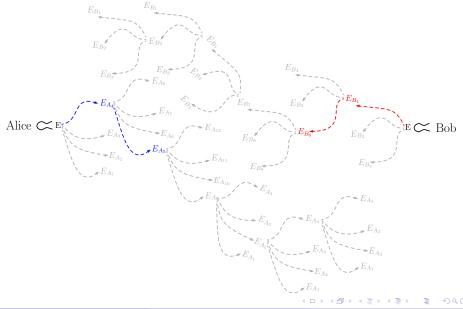
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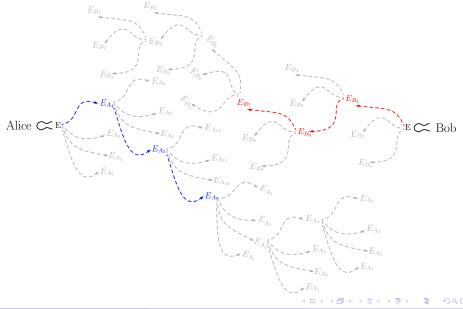


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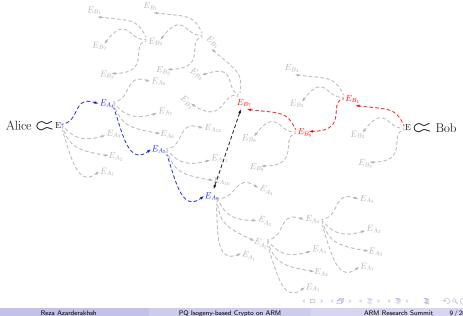


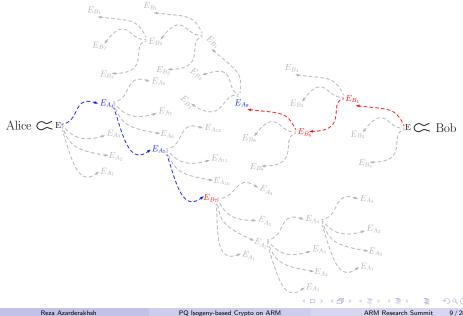
PQ Isogeny-based Crypto on ARM



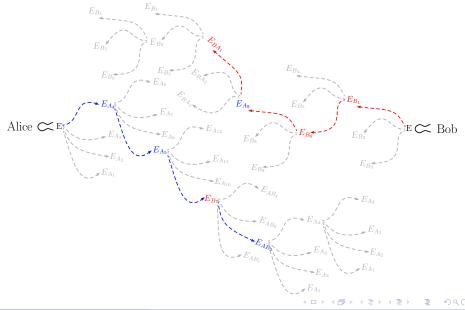


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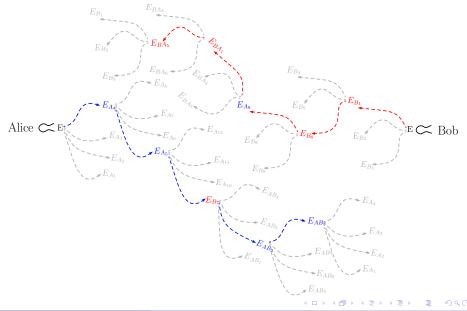
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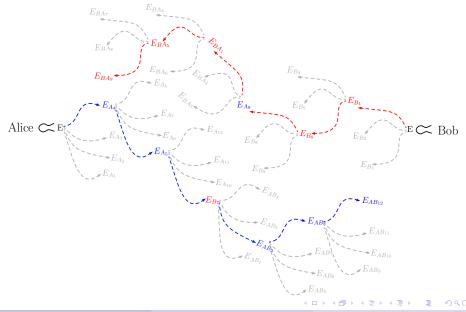


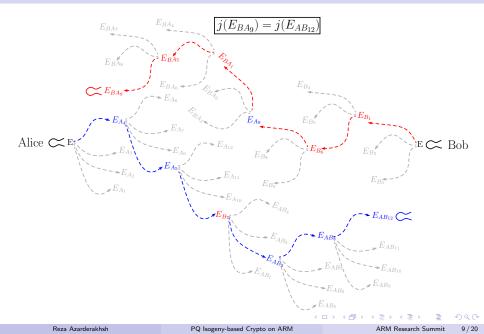
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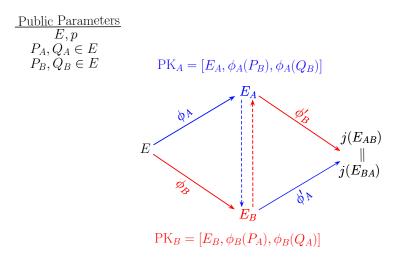
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## Supersingular Isogeny-Based Cryptography Pros and Cons

Pros

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## Cons

• Youngest PQC candidate.

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Table: Communication bandwidth of some NIST PQC candidate KEMs in terms of public-key, secret-key, and transmitted ciphertext during the key encapsulation process.

Candidate	Primitive	Size (Bytes)				
Candidate	Frintive	Public key	Secret key	Ciphertext		
NewHope1024	RLWE	1824	3680	2208		
Saber	Mod-LWR	992	2304	1088		
NTRU-HRSS17	LWE	1138	1418	1278		
Kyber-768	LWE	1088	2400	1152		
NTRU Prime	RLWE	1218	1600	1047		
SIKEp751	SI	<b>56</b> 4	644	596		

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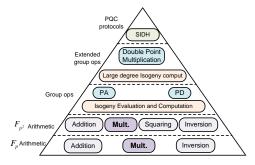
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Different Families of Processors:

- ARMv7-M  $\rightarrow$  32-bit Low-Power (Performance is challenging)
- $\bullet$  ARMv7-A  $\rightarrow$  32-bit High-Performance with NEON Instruction set
- $\bullet$  ARMv8-A  $\rightarrow$  64-bit High-Performance with Adv. SIMD instruction set





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Figure: ARMv7-A Cortex-A15 (Jetson TK1 Board) and ARMv8-A Cortex-A57 (Nexus smartphone)

<sup>&</sup>lt;sup>4</sup>Taken from https://developer.nvidia.com

<sup>&</sup>lt;sup>5</sup>Taken from https://www.huawei.com

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 $A.B = A_h B_h 2^n + [(A_h + A_l)(B_h + B_l) - A_h B_h A_l B_l] 2^{\frac{n}{2}} + A_l B_l.$ 

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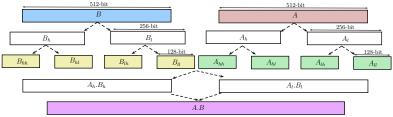
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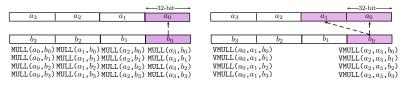
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- NEON Assembly Implementation:
  - SIMD multiplication instructions reduce the total number of multiplications significantly
  - 128  $\times$  128-bit multiplication using A32 and NEON:

			←32-bit →				←32-bit →
$a_3$	$a_2$	$a_1$	$a_0$	$a_3$	$a_2$	$a_1$	$a_0$
			^			*	J
$b_3$	$b_2$	$b_1$	$\dot{b}_0$	$b_3$	$b_2$	$b_1$	$b_0$
$MULL(a_0, b_0)$	MULL $(a_1, b_0)$	$MULL(a_2, b_0)$	$MULL(a_3, b_0)$	VMULL(a0,a1	1, <i>b</i> <sub>0</sub> )	VN	$(ULL(a_2, a_3, b_0))$
$MULL(a_0, b_1)$	$MULL(a_1, b_1)$	$MULL(a_2, b_1)$	$MULL(a_3, b_1)$	VMULL(a0,a1	1, <i>b</i> 1)	VN	$\text{MULL}(a_2, a_3, b_1)$
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• 16  $\times$  MULL instructions in A32 vs. 8  $\times$  VMULL in NEON Vector Instructions.

#### Performance Reports on Various Platforms

- SIDH performance evaluation on different families of ARM processors
- Different security levels

Work	Lang.	Device	Field	PQ	Total Time
WORK	Lang.		size	Security	(ms)
AFJ14	с	Cortex-A15	771	128	1,308
			1035	170	2,816
KJAJM16	ASM	Cortex-A15	1008	167	982
JAMJ17	ASM	Cortex-A57 751 964	751	125	331
			964	160	652
	С		751	125	1,846
			964	160	4,212
	ASM	Cortex-A72	751	125	271
			964	160	528
	С		751	125	1,495
			964	160	3,495

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AI J14		COLEX-AID	1035	170	2,816
KJAJM16	ASM	Cortex-A15	1008	167	982
JAMJ17	ASM	Cortex-A57	751	125	331
			964	160	652
	С		751	125	1,846
			964	160	4,212
	ASM	Cortex-A72	751	125	271
			964	160	528
	С		751	125	1,495
			964	160	3,495

• Reasonable performance, but we still need to improve these results.

- SIDH performance evaluation on different families of ARM processors
- Different security levels

Work Lang.		Device	Field	PQ	Total Time
WORK	Lang.	ang. Device		Security	(ms)
AFJ14	с	Cortex-A15	771	128	1,308
AI J14		COLEX-AID	1035	170	2,816
KJAJM16	ASM	Cortex-A15	1008	167	982
JAMJ17	ASM	Cortex-A57	751	125	331
			964	160	652
	С		751	125	1,846
			964	160	4,212
	ASM	Cortex-A72	751	125	271
			964	160	528
	С		751	125	1,495
			964	160	3,495

- Reasonable performance, but we still need to improve these results.
- ARMv7-M platforms require further investigations due to the low working frequency (latest reported timings are in seconds).

- Quantum computers and their exceptional computational power will solve all the underlying problems that current PKC is constructed upon.
- We need to be prepared for this threat.
- NIST has already started the PQC standardization procedure.
- Different proposals have been submitted.
- SIKE is the only primitive which is constructed on the popular elliptic curves.
- SIKE offers the smallest key and ciphertext size among other candidates and it is suitable for embedded devices.

# SIKE team

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## Thank You!

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