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# *Embedded Intelligence for Self-Aware and Adaptive VLSI Systems*

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# Overview



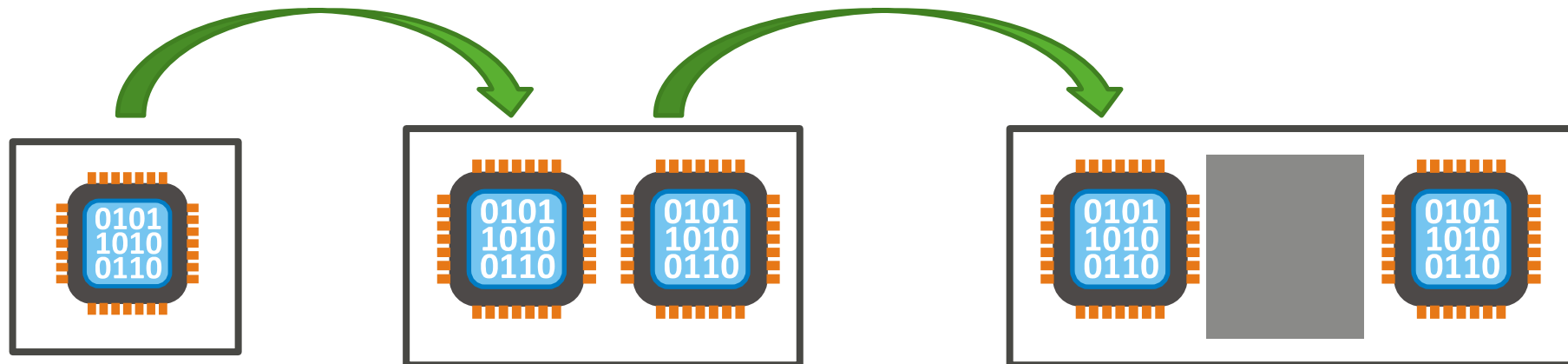
1. Nervous Systems in Nature
2. Nervous SoC concept
3. Early Experiments –  
Overclocking and Overheating  
FPGAs!

# High Density VLSI Design Challenges



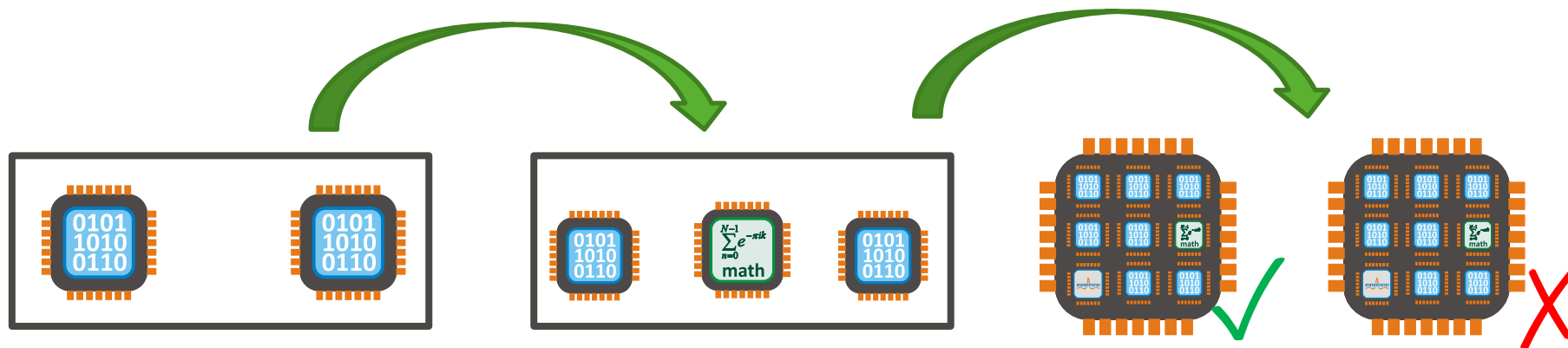
- Lots of challenges coming up for large scale SoCs:
  - Process variability
  - Dark Silicon
  - Ageing effects
- Mitigation so far has been pessimistic :
  - Slower clock frequencies
  - Silicon used as thermal buffering
  - Redundant units
- Anything added to compensate these problems *should not make them worse!*

# High Density VLSI Design Challenges



*“We’ve run out of power so we can’t speed this core up any more – time to add another”*

*“The cores are running too hot, we shall have to separate them”*



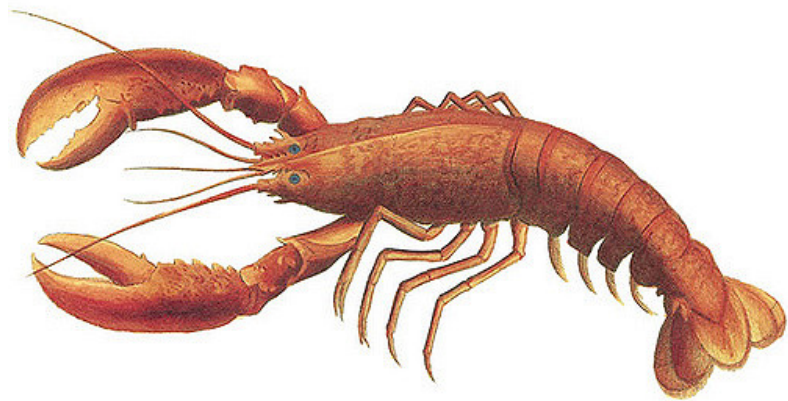
*“We can’t run all the cores at once, we shall have to specialise”*

*“Device variation means this device meets the spec but this one doesn’t – time to change the spec...”*

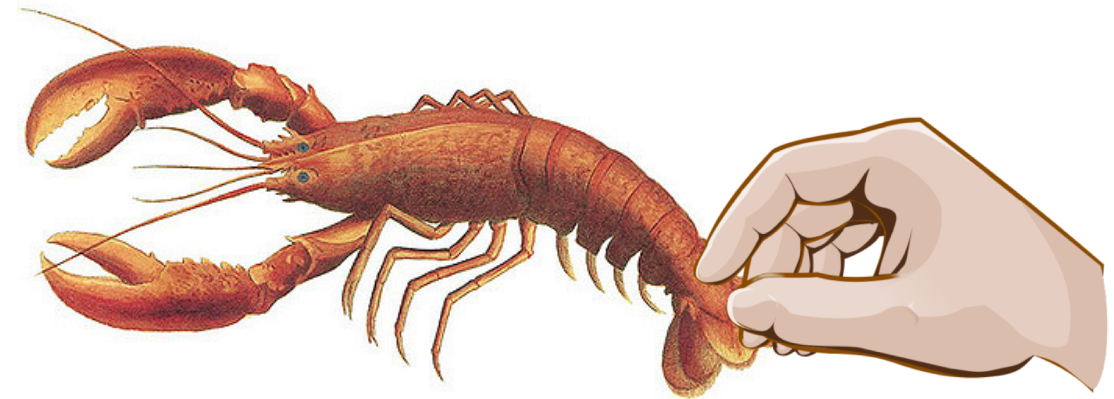


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# Natural Nervous Systems



# Crayfish Escape Response

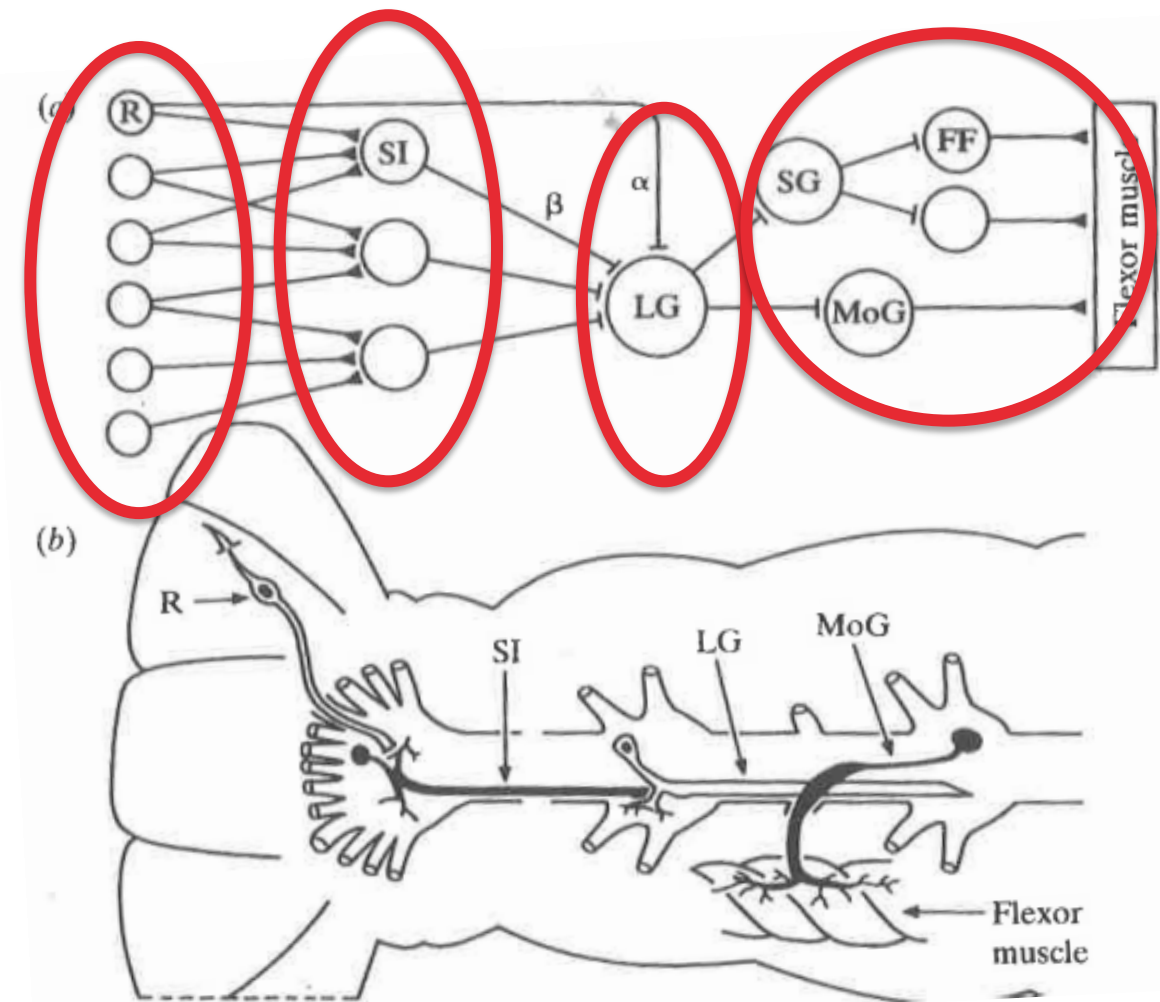


- Striking the tail of a crayfish will result in the crayfish swimming away at great speed
- However, strike a few times and then the crayfish stops reacting
- It will then react again after a “rest period”
- Swimming, water movement or a slow touch does not cause this response to be triggered

# Crayfish Escape Response



1. Receptor cell (R) sensitive to touch and  $>80\text{Hz}$  water movement (filters out water movement). Generates a spike when triggered and chemical signal to (SI)
2. Sensory Interneuron (SI) converges inputs from the (R) cells.
3. Spike from (R) cell is not enough to trigger Lateral Giant neuron (LG), requires SI spike as well. Has a short decay constant so a large number of spikes must arrive within a short amount of time to fire
4. (SG) segment giant, (MoG) motor giant and (FF) fast flexor are motor neurons that handle the tail flip locomotion



**Simmons, Young: *Nerve Cells and Animal Behaviour* (1999)**

# Leech Bending Control



A leech has three responses to threat depending on how hard it is attacked:

- A. Light press – slight bend away from source



- B. Harder press, leech will shrink

- C. Sometimes this press will result in a swimming “escape” response

**Durbin, Miall, Mitchinson: *The Computing Neuron (1989)***



# Leech Bending Control



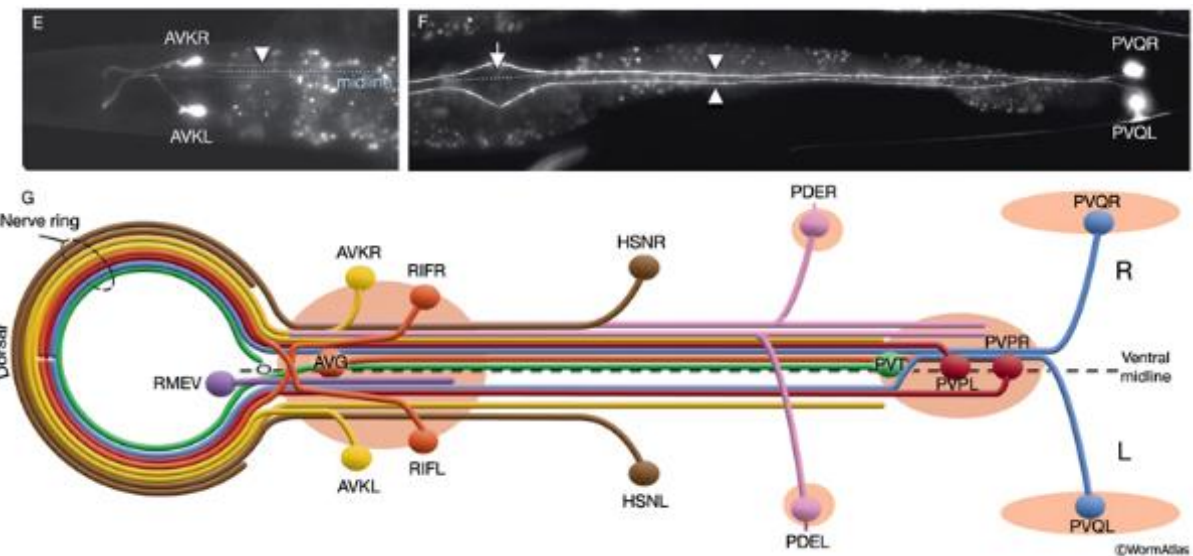
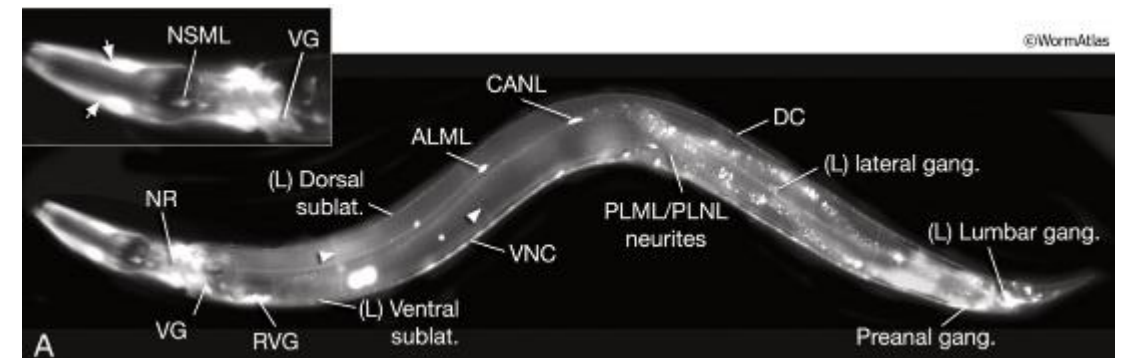
- A. Light press: slight bend away from source
- B. Harder press: leech will shrink
- C. Sometimes this press will result in a swimming “escape” response



Durbin, Miall, Mitchinson: *The Computing Neuron* (1989)

# C. Elegans

- Hermaphrodite and male (development specialisations)
- “Only” 302 neurons
- Nervous system fully mapped
- 118 “classes” of neural circuitry
- ~5000 synapses
- Attempt at simulating the worm’s behaviour at neuron level. ( the *openworm* project)



<http://www.wormatlas.org>: *C. Elegans* behavioural and structural anatomy

# C. Elegans



## Chemosensors (Taste)

*Cilia exposed to outside*

### Amphids

ADF (2, head) 5,9  
ASE (2, head) 6,7,9  
ASG (2, head) 5,9, 21  
ASH (2, head) 1,7, 8, 10, 13, 19, 22  
ASI (2, head) 5, 9, 20, 21  
ASJ (2, head) 5, 9, 21  
ASK (2, head) 6, 9, 19, 20, 21  
ADL (2, head) 10, 22

### Inner labials

IL2 (6, head)

### Phasmids 8

PHA (2, tail)  
PHB (2, tail)

## Odorsensors (Smell)

*Cilia embedded in sheath*

### Amphids

AWA (2, head) 11, 21  
AWB (2, head) 10  
AWC (2, head) 11, 20, 21

*Cilia exposed to outside*

### Amphids

ASH (2, head) 1,7, 8,10,13, 19, 22

## Oxygen sensors

*Cilia or cell body in psuedocoelomic cavity* 22

AQR (1, head)  
PQR (1, tail)  
URX (2, head)

*Unexposed ciliated endings in the lips*

BAG (2, head) 3

## Nociceptors (Pain)

### Amphids

ASH (2, head) 1,7, 8,10,13, 19, 22

## Osmoceptors

### Amphids

ASH (2, head) 1,7, 8,10,13, 19, 22

(Also AFD, FLP, PHC and PVD neurons as thermocceptive) 24

## Thermosensors

*Cilia embedded in sheath*

### Amphids

AFD (2, head) 23  
AWC (2, head) 23

*Extensively branched (thermonocceptive)*

FLP (2, head) 24  
PVD (2, body) 24

*Tail tip (thermonocceptive)*

PHC (2, tail) 24

## Mechanosensors

*Microtubule-filled dendrites (MT cells)*

### Bodywall 12

ALM (2, body)  
AVM (1, body)  
PLM (2, tail)  
PVM (1, body)

*Unexposed cilia ending in cuticle*

### Inner labials

IL1 (6, head) 3,13

### Cephalic

CEP (4, head) 4

### Outer labials

OLQ (4, head) 3,13  
OLL (2, head) 3,17

### Anterior and Posterior deirids

ADE (2, head) 4  
PDE (2, body) 4

*Cilia exposed to outside*

### Amphids

ASH (2, head) 1,7, 8,10,13, 19, 22

*Extensively branched*

FLP (2, head) 13, 23  
PVD (2, body)

## Possible sensory neurons with unknown modality

*Unexposed endings (no cilia)*

AUA (2, head)  
URY (4, head)  
URA (4, head)  
URB (2, head)

## Proprioceptors 18

*Putative stretch-sensitive processes*

### Somatic-bodywall

FLP (2, head) 13  
PVD (2, body) 14  
DVA (1, tail)  
PVC (2, tail) 14  
ALN (2, tail) 16, 22  
PLN (2, tail) 16, 22  
VA 15  
VB 15  
DA 15  
DB 15

### Head

SMB (4, head) 15  
SMD (4, head) 15  
SAA (4, head) 15

### Tail tip 16

AVG (1, head)  
PDB (1, tail)  
PHC (2, tail) 3  
PVR (1, tail)  
ALN (2, tail)  
PLN (2, tail)  
PLM (2, tail)

### Pharynx 2

I1 (2, head)  
I2 (2, head)  
I3 (1, head)  
I5 (1, head)  
I6 (1, head)  
MC (1, head)  
M3 (2, head)  
NSM (1, head)

# Nervous System-on-Chip

# Nervous SoC Concept



- Concept targets three increasingly complex layers of intelligence models:

## Stage 1

Individual sensing neurons embedded within the SoC sensing both digital and analogue properties of the fabric

## Stage 2

Small-scale SNNs capable of detecting and changing local behaviour and operation autonomously

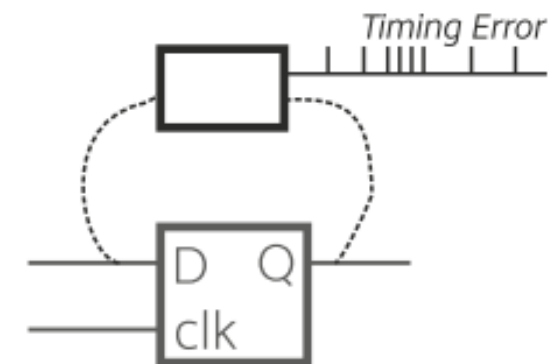
## Stage 3

Local “Anomaly Managers” are then connected together to form larger clusters of neurons capable of detecting and predicting system-wide anomalies and errors

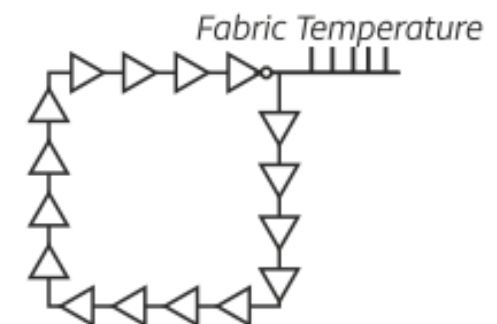
# Low Level Sensing

- Take off-the-shelf sensing circuitry and transform into a form capable with digital spiking neural networks
- Spike outputs can be frequency based or indication based
- By using spikes only single wires are required to carry monitoring information around the chip
- Information represented by frequency should be SEU tolerant
- Opportunity here for new VLSI embedded sensors (ASIC run included in the proposal)

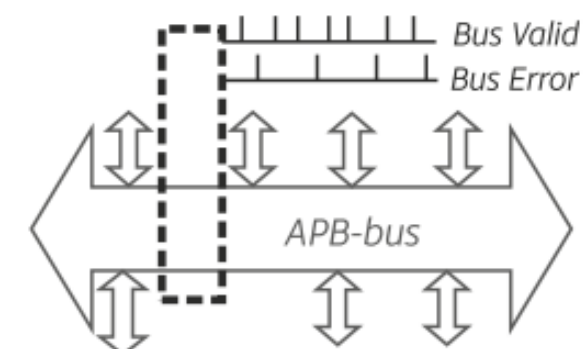
Timing Violation Detection



Die Temperature Sensing (localised)



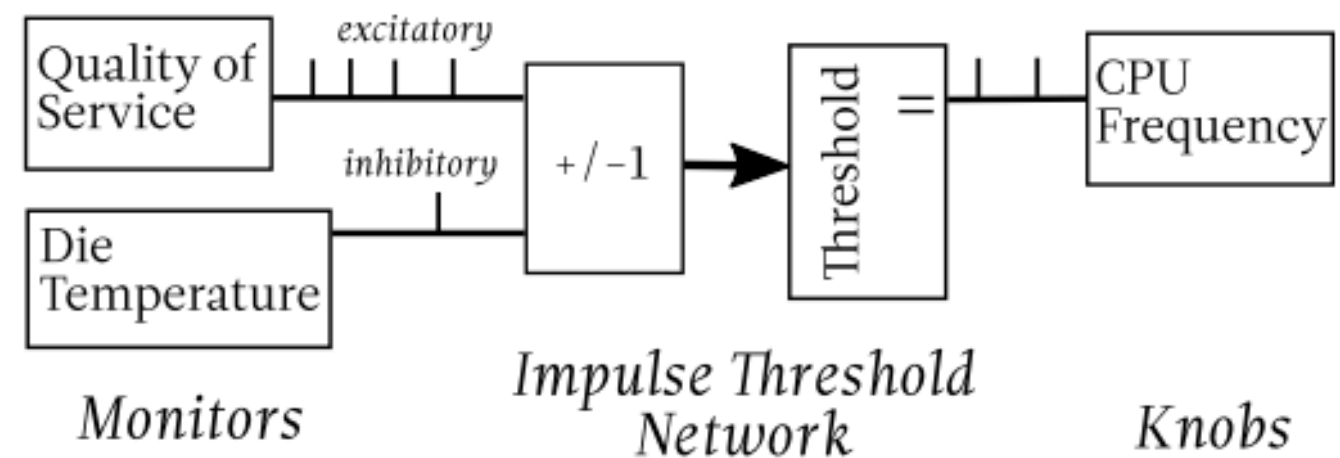
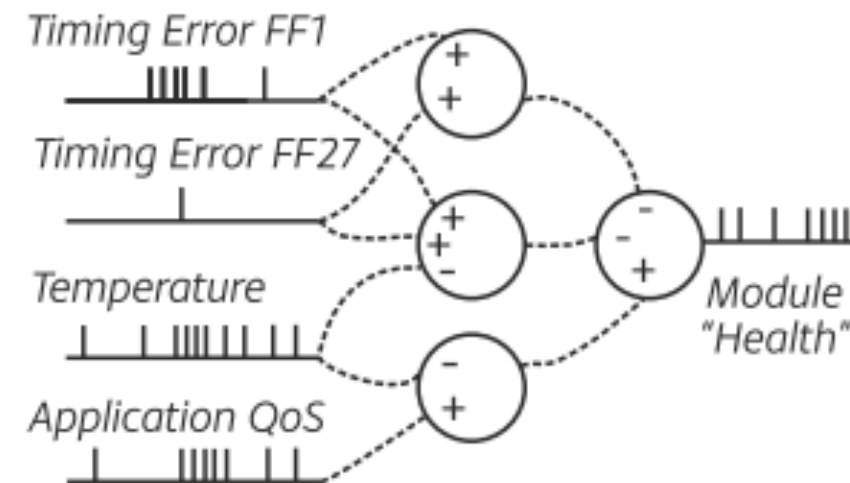
Bus Fault Detection



# Low Level Reactions

- Small networks will pull collections of spiking sensors together for analysis
- Outputs from these small networks will feed the higher levels of the Nervous SoC
- They will also be used within the local control networks for controlling relevant actuators
- These actuators will again consist of bespoke and off-the-shelf components e.g. programmable delay lines, PLLs

## Sensory Aggregation



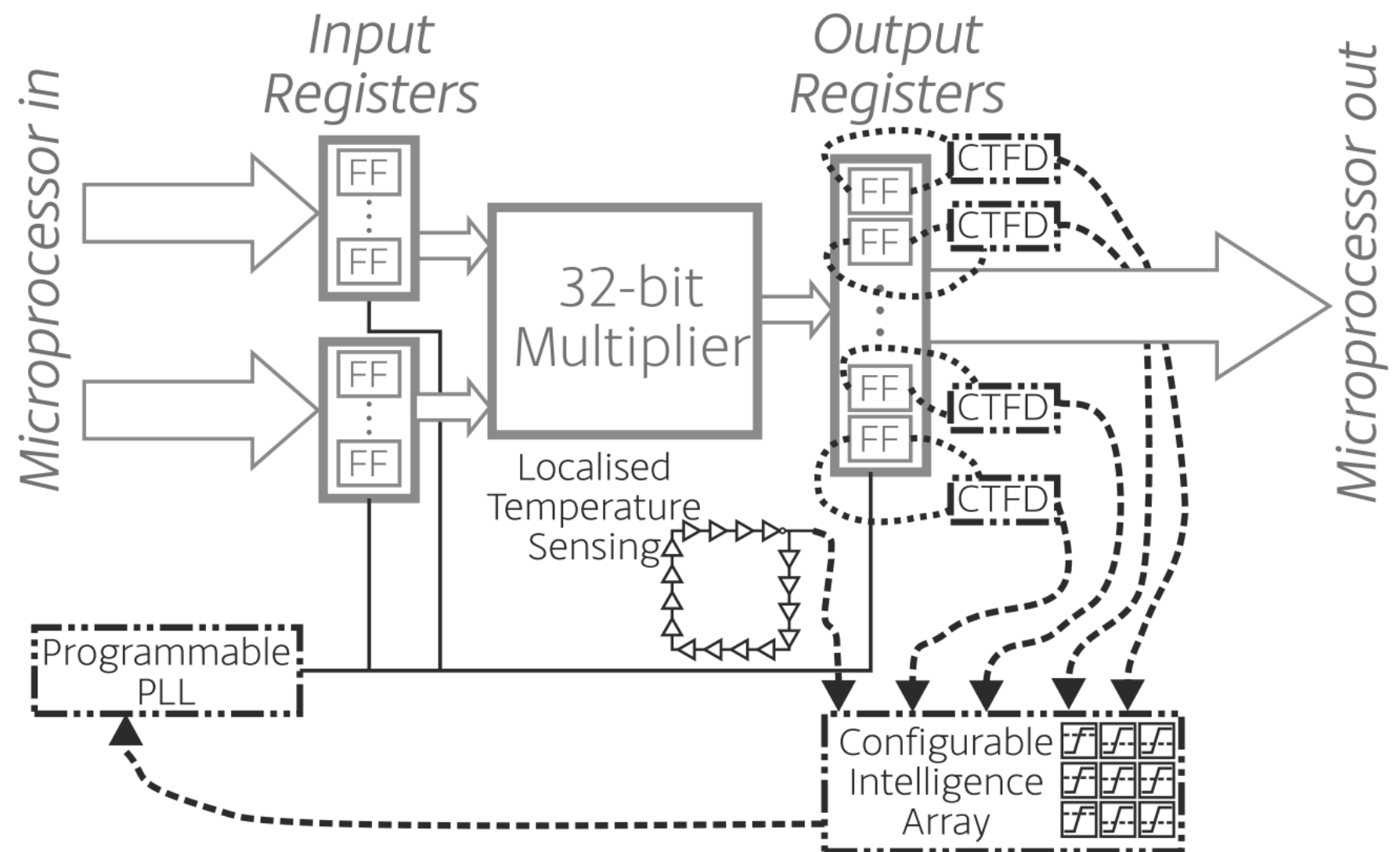
# Proof of Concept Hardware Experiments



# Experimental Testbench



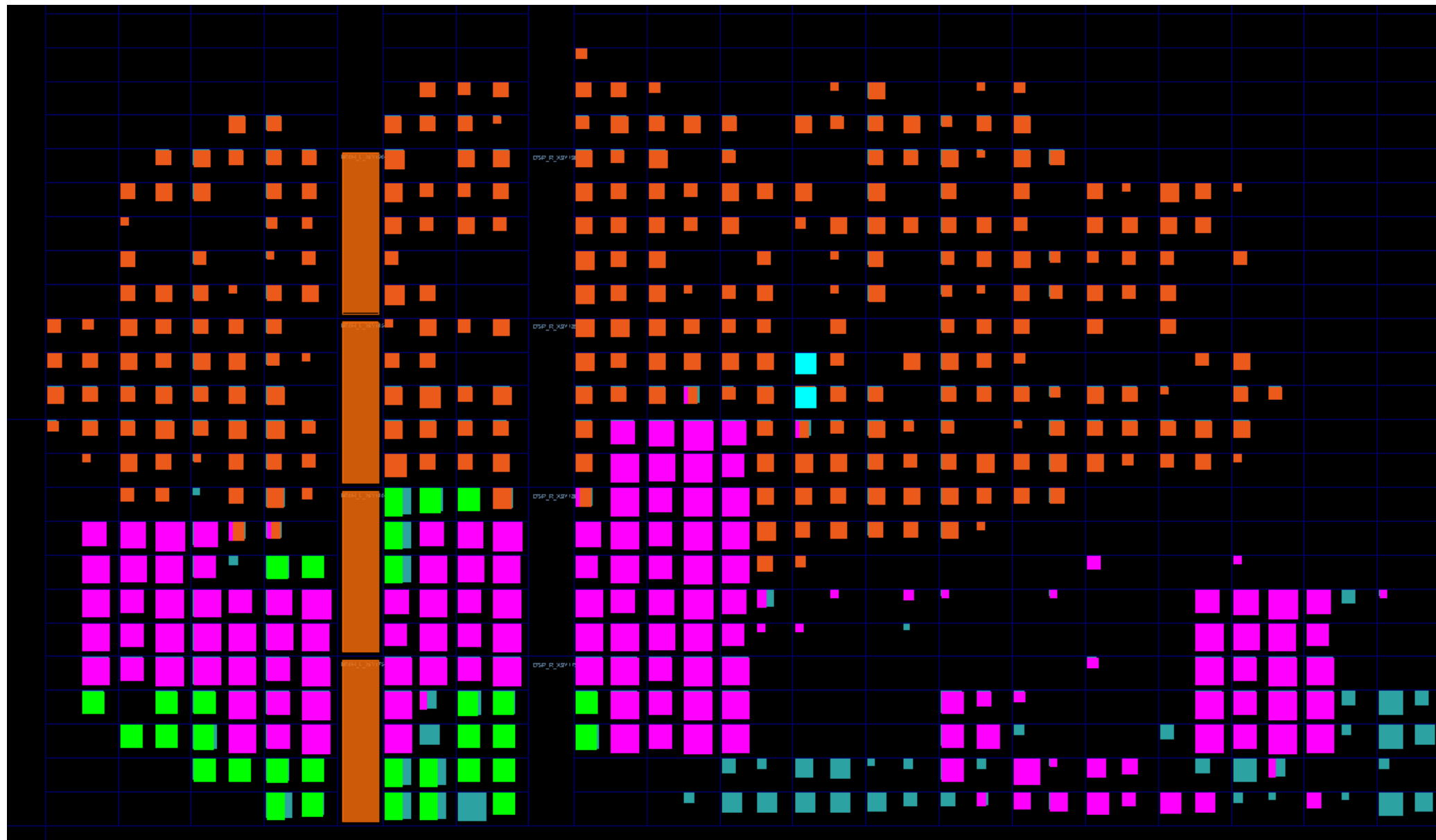
- Isolated test setup allows unit to be evaluated within a SoC.
- Input FIFOs, output FIFOs and error capture FIFOs allow all status signals to be captured
- Microprocessor –controlled DUT PLL and Peltier heater



# Experimental Testbench



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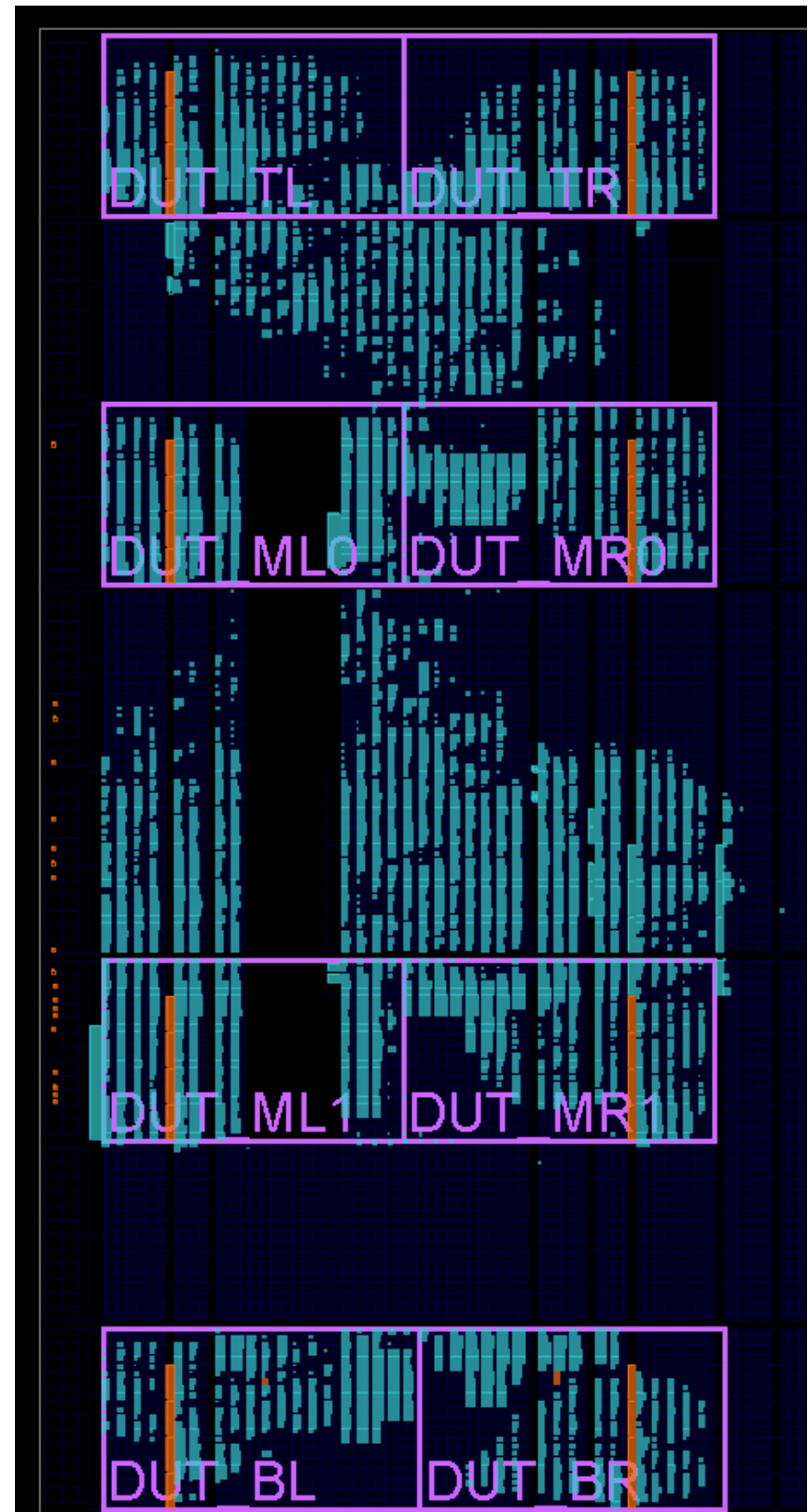
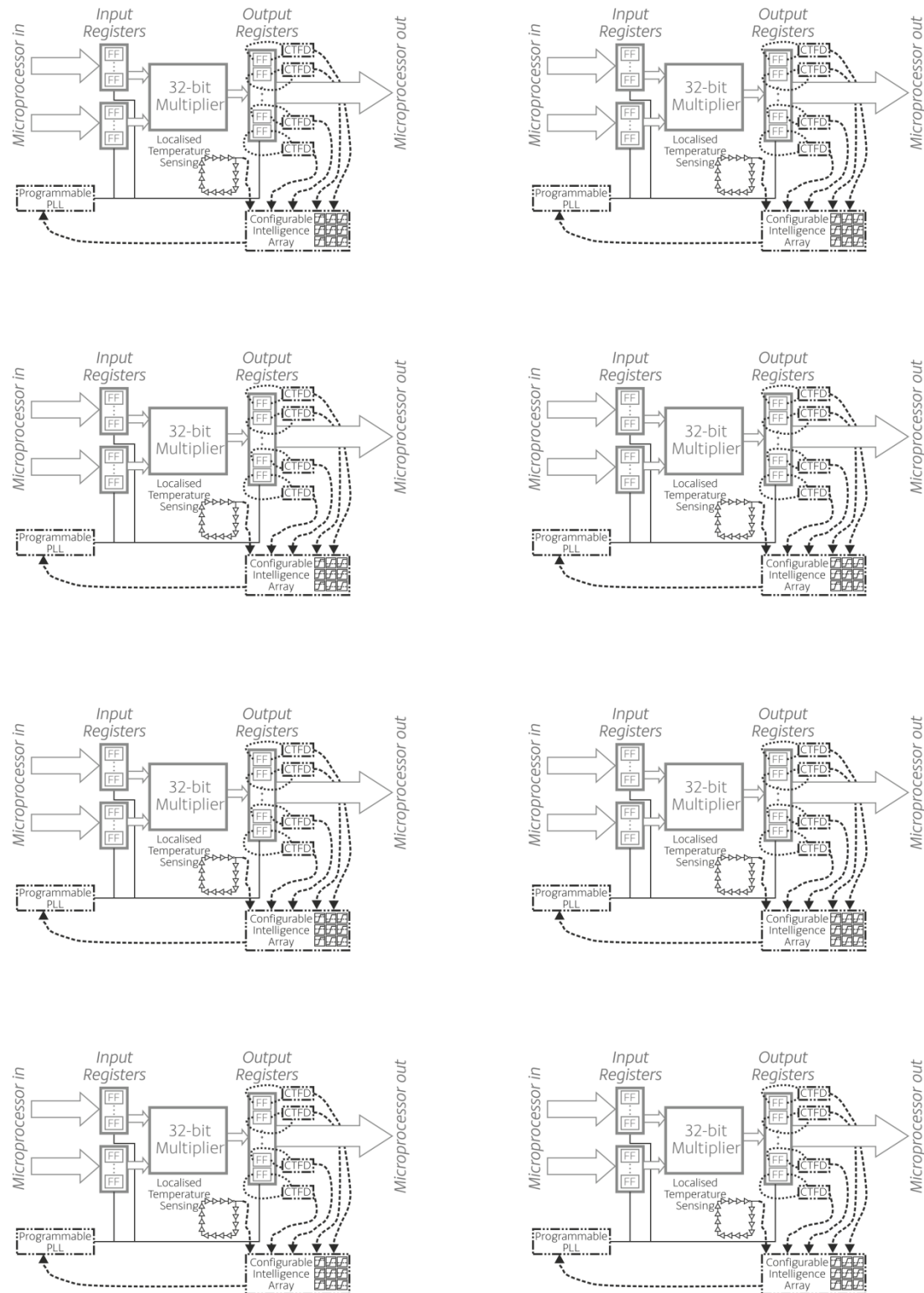


- DUT (32-bit multiplier) - Orange
- Timing fault detectors – Green
- Intelligence – Purple
- Ring Oscillator - Cyan

# Experimental Testbench



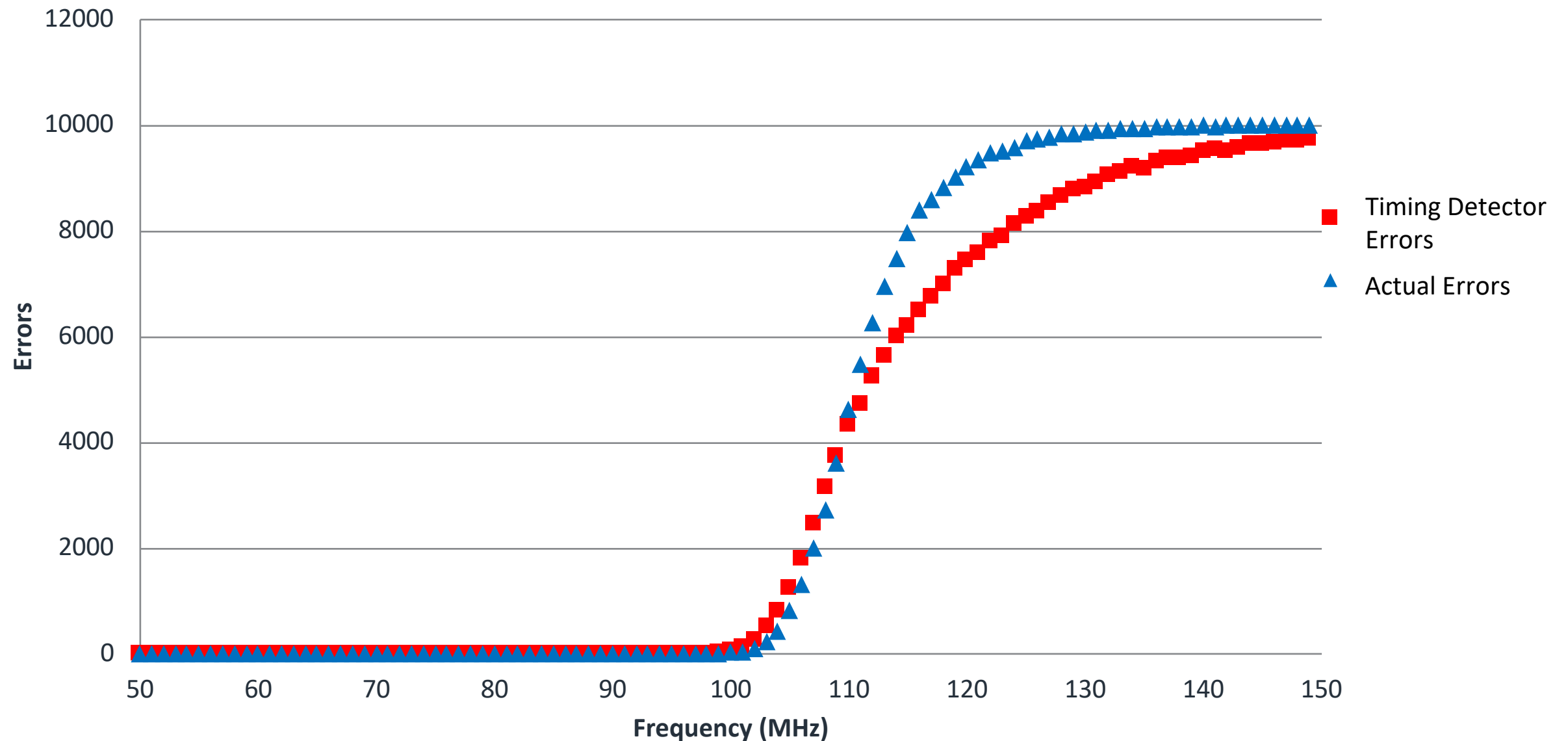
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# Experiment #1: Going beyond the EDA tools

- Tools report a critical path of 51.3 MHz through the multiplier

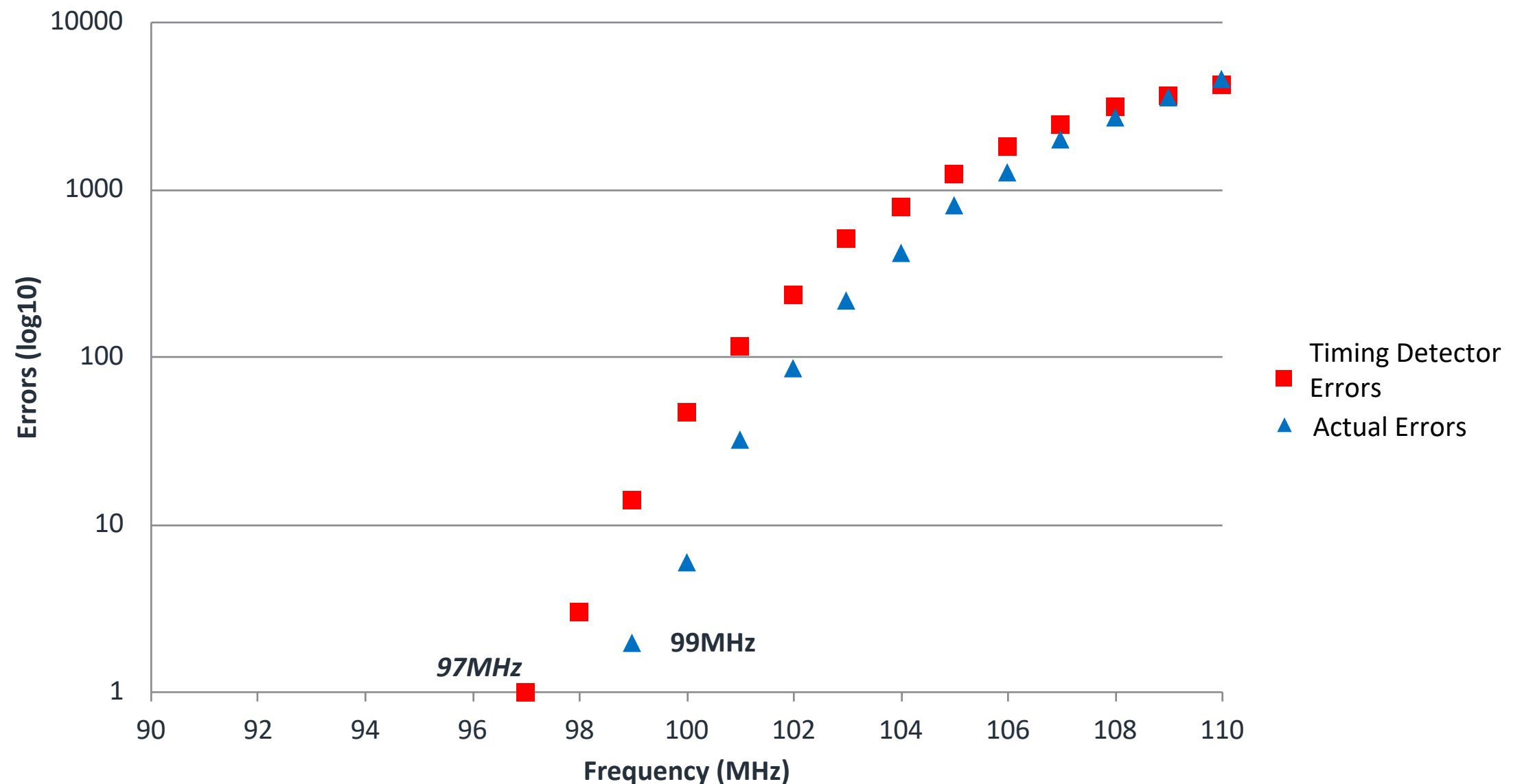
Timing Errors vs Frequency (32-bit multiplier, 50MHz)



# Experiment #1: Going beyond the EDA tools

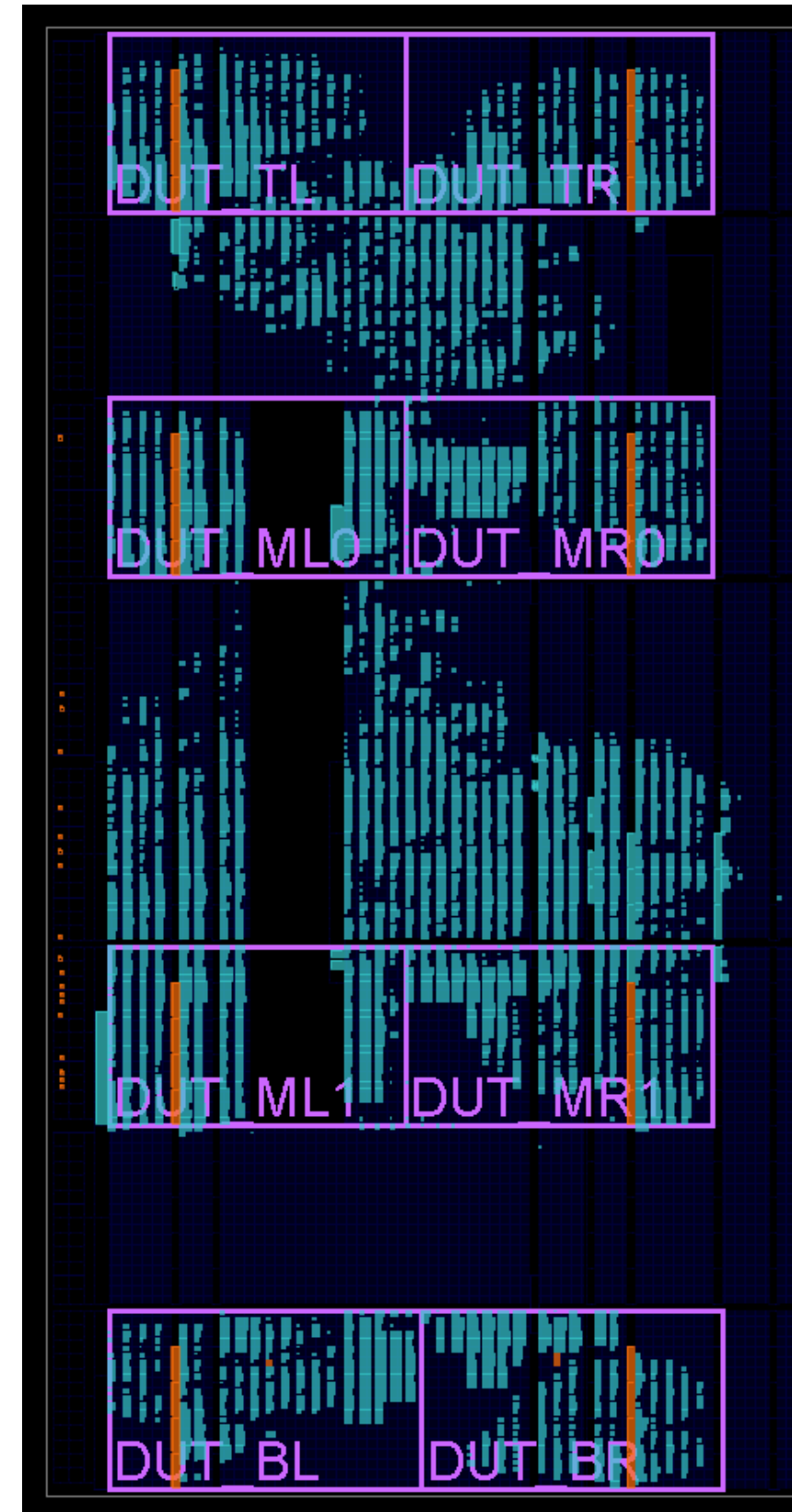
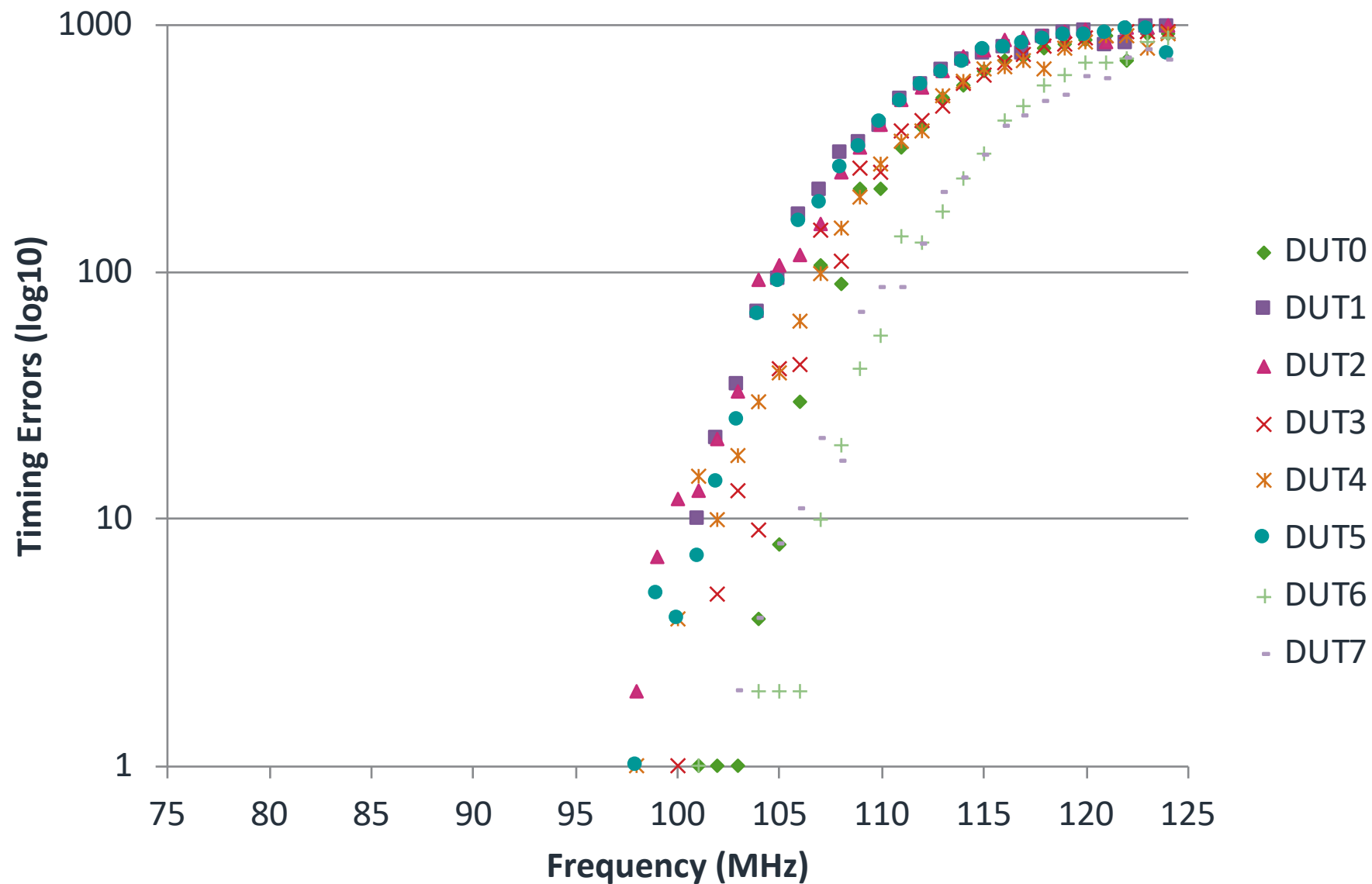
- Tools report a critical path of 51.3 MHz through the multiplier

Timing Errors vs Frequency (32-bit multiplier, 50MHz)



# Experiment #1: Going beyond the EDA tools

Timing Errors vs Frequency (32-bit multiplier, 50MHz)



# Experiment #2: Going beyond the datasheet

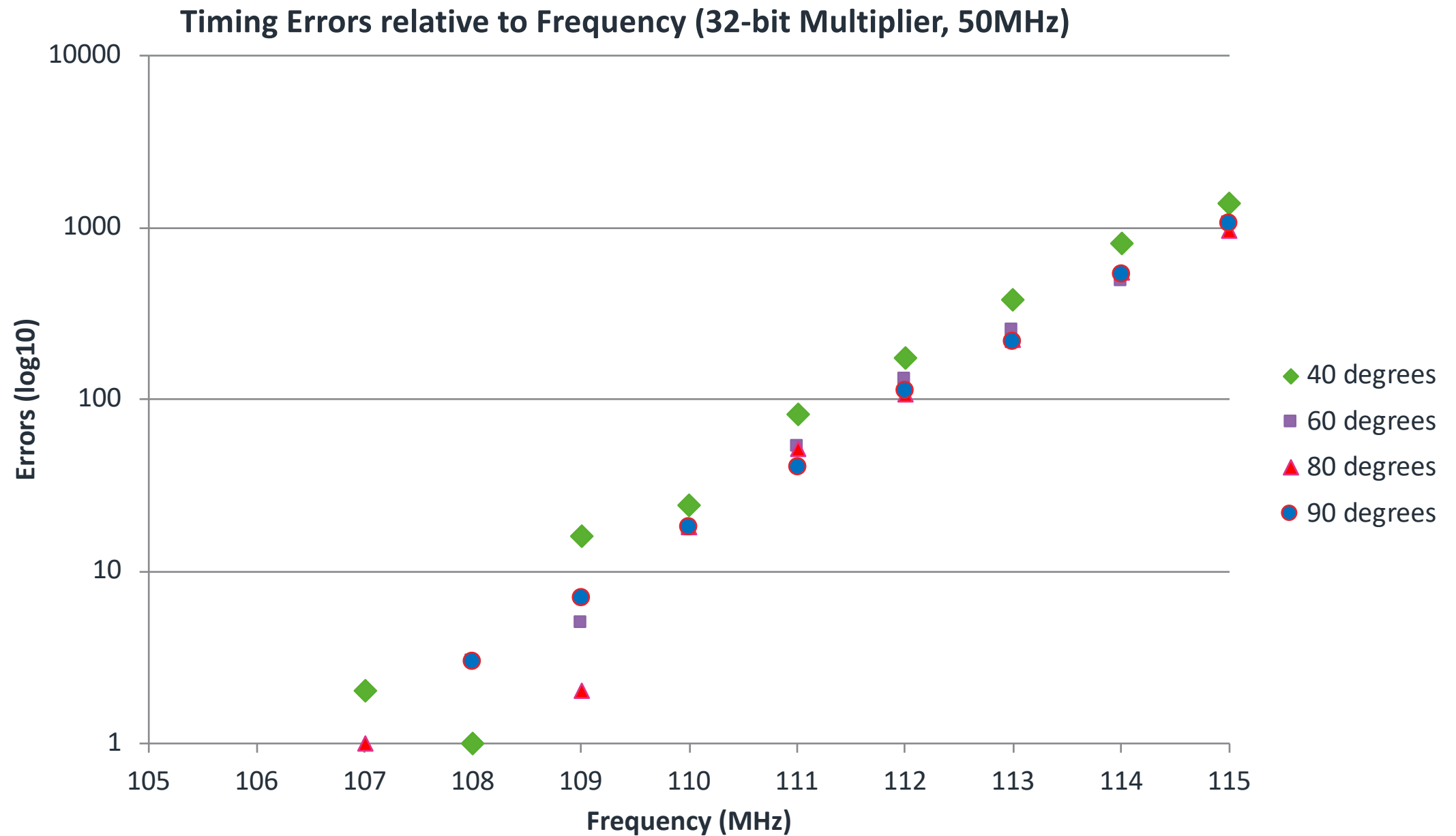


- We are using XC7A100T-1CSG324C as our test device:
  - Commercial grade device, should be fine up to 85 degrees

Temperature					
$T_j$	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices	–40	–	125	°C
	Junction temperature operating range for military (M) temperature devices	–55	–	125	°C

**Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics** *DS181 (v1.25) (Xilinx inc.)*

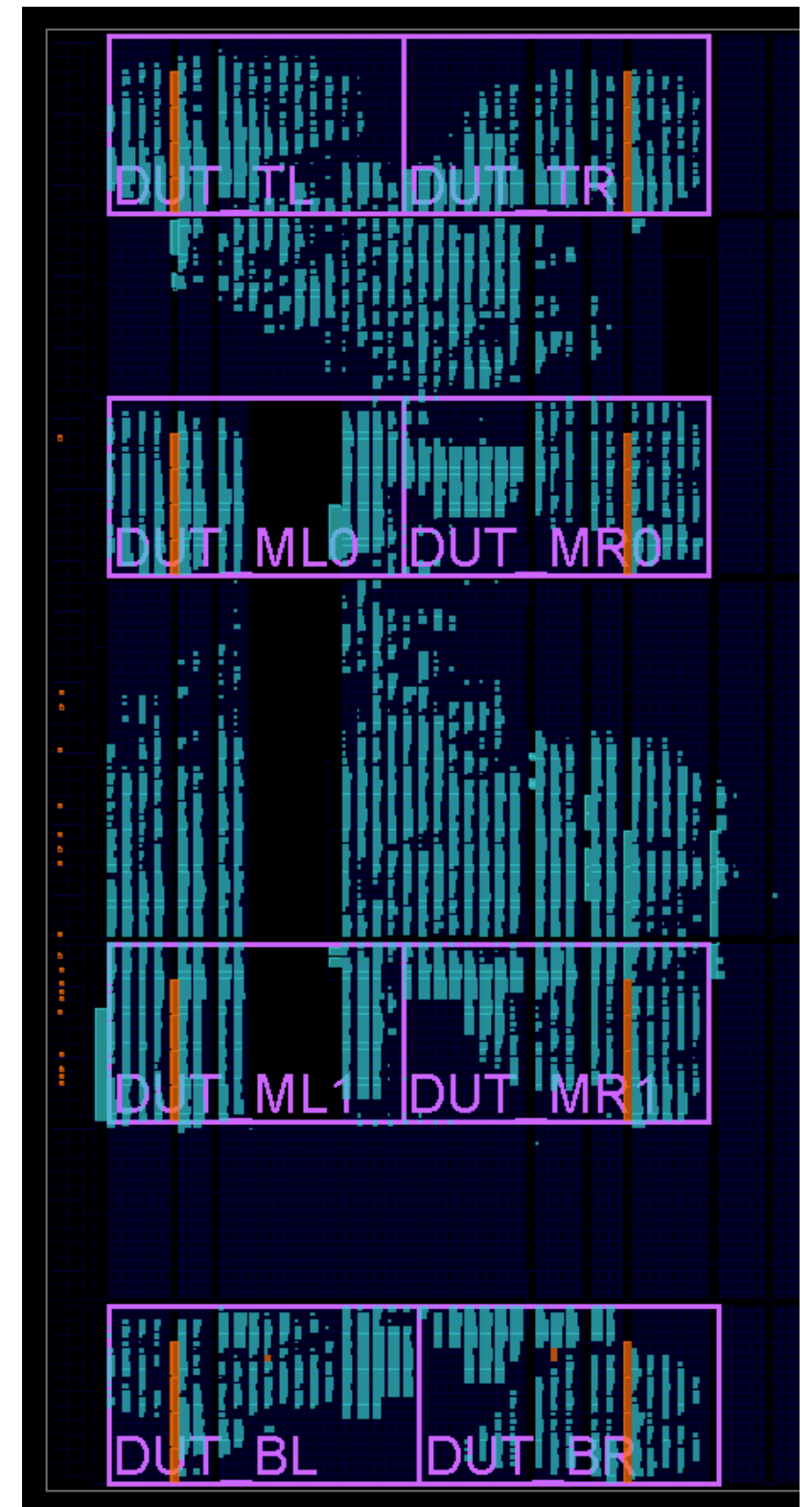
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# Experiment #2: Going beyond the datasheet

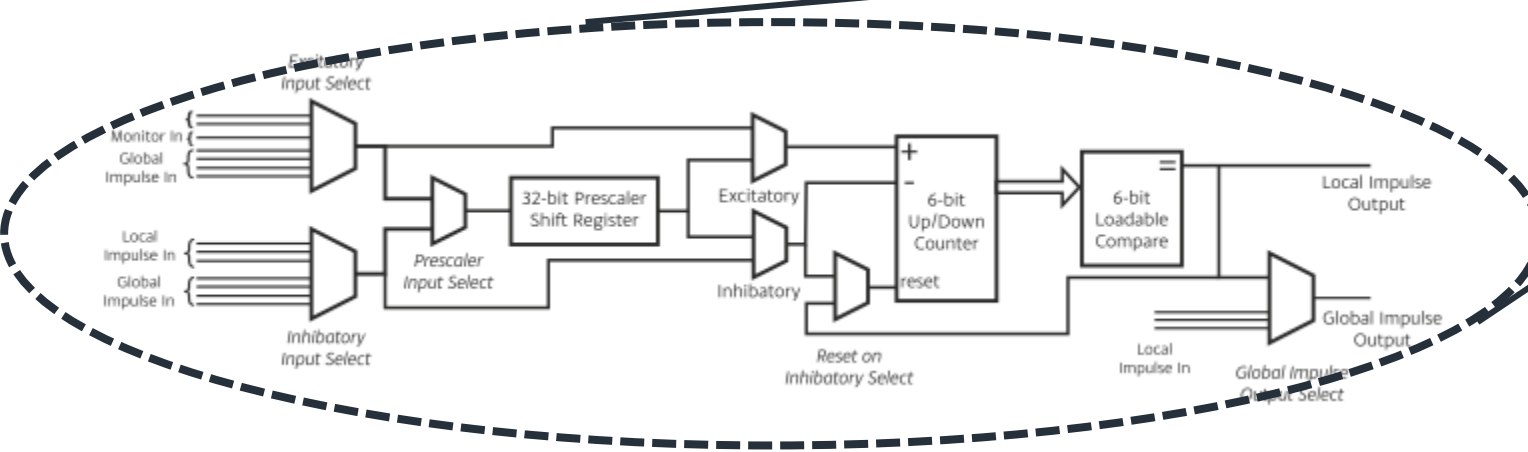
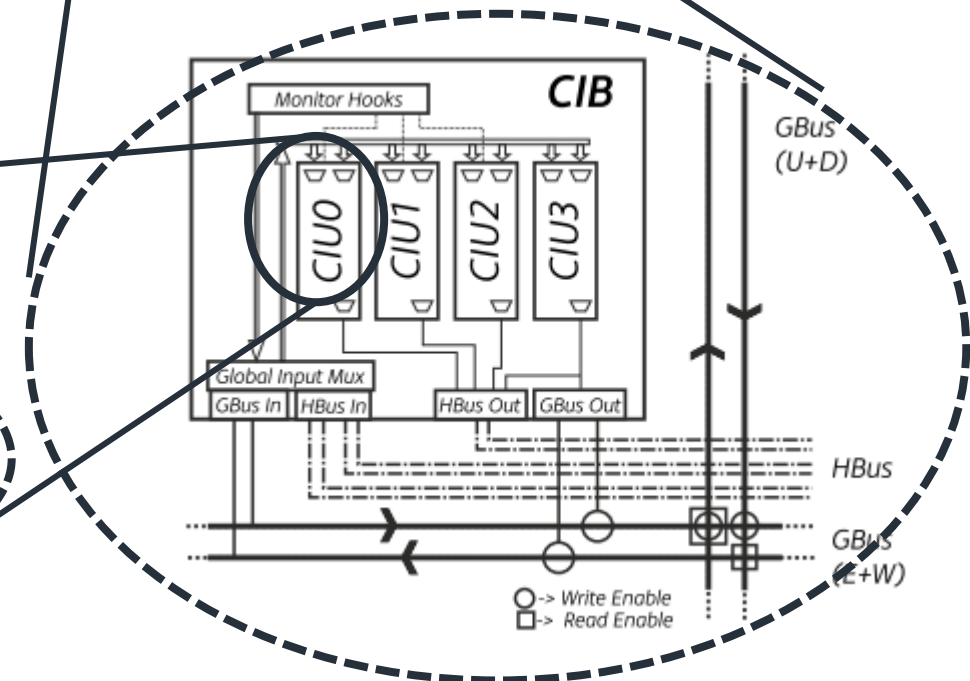
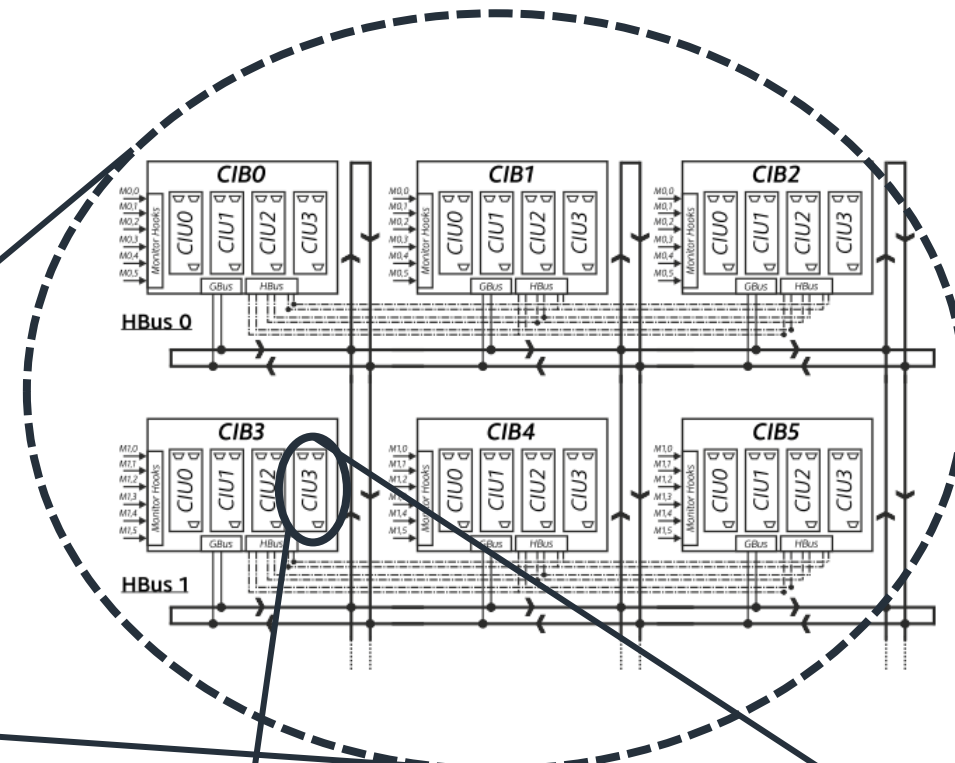
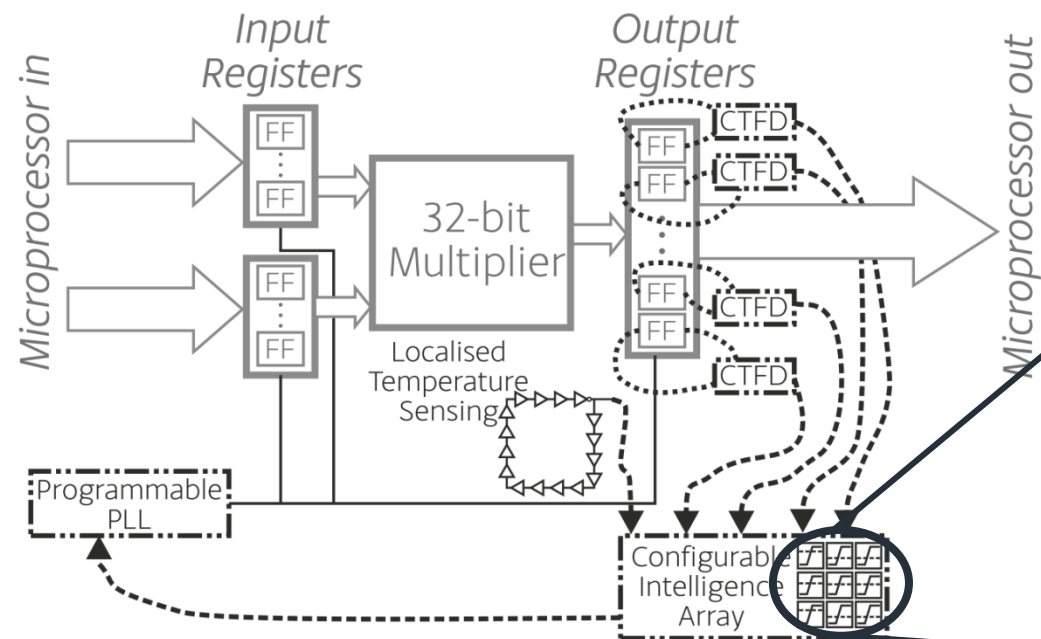
<u>First error frequency at 125°C</u>	
99MHz	100MHz
93MHz	95MHz
94MHz	98MHz
98MHz	99MHz



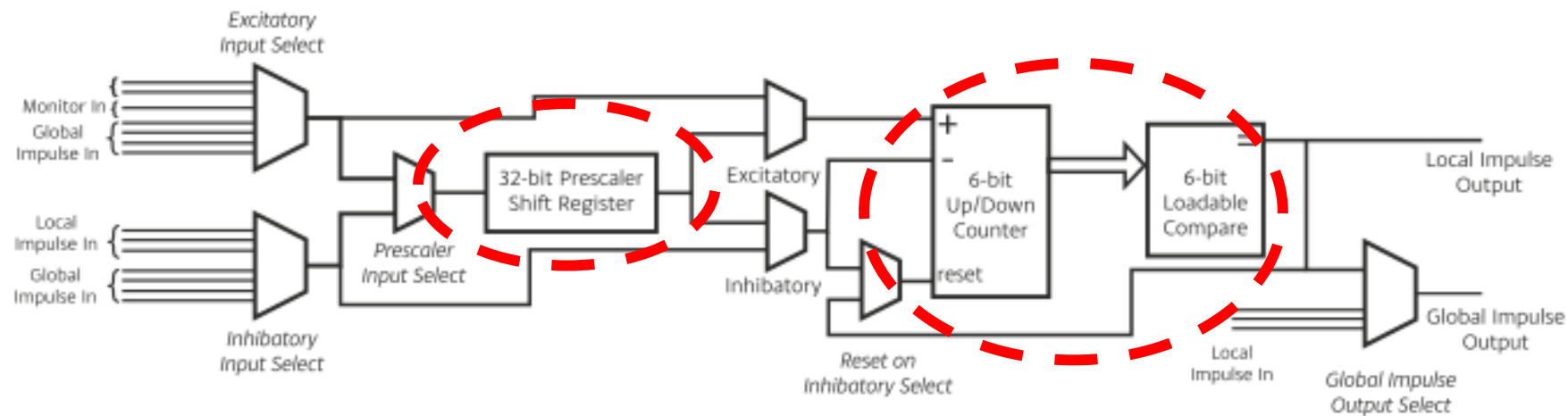
# Configurable Intelligence Array



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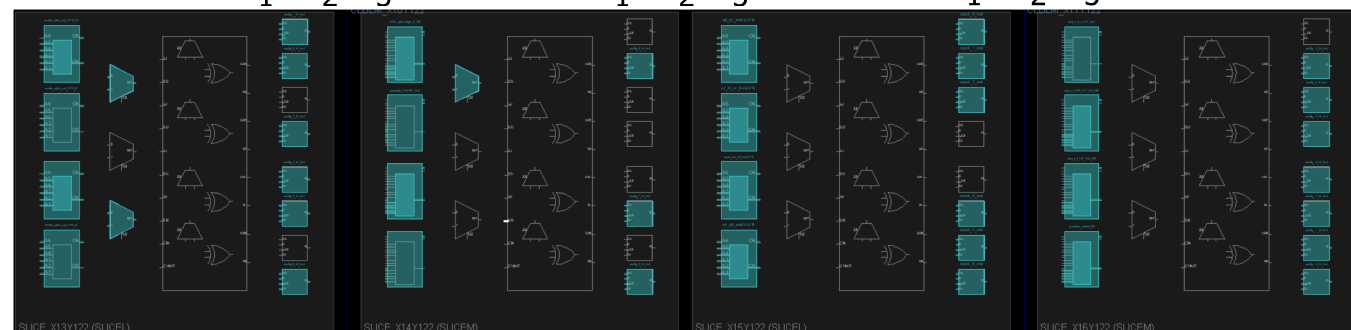
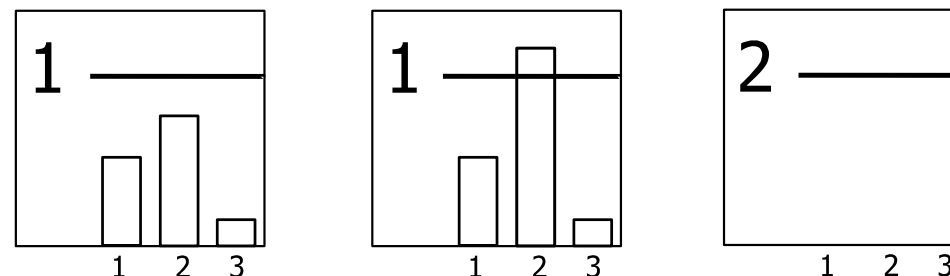


# Configurable Intelligence Unit

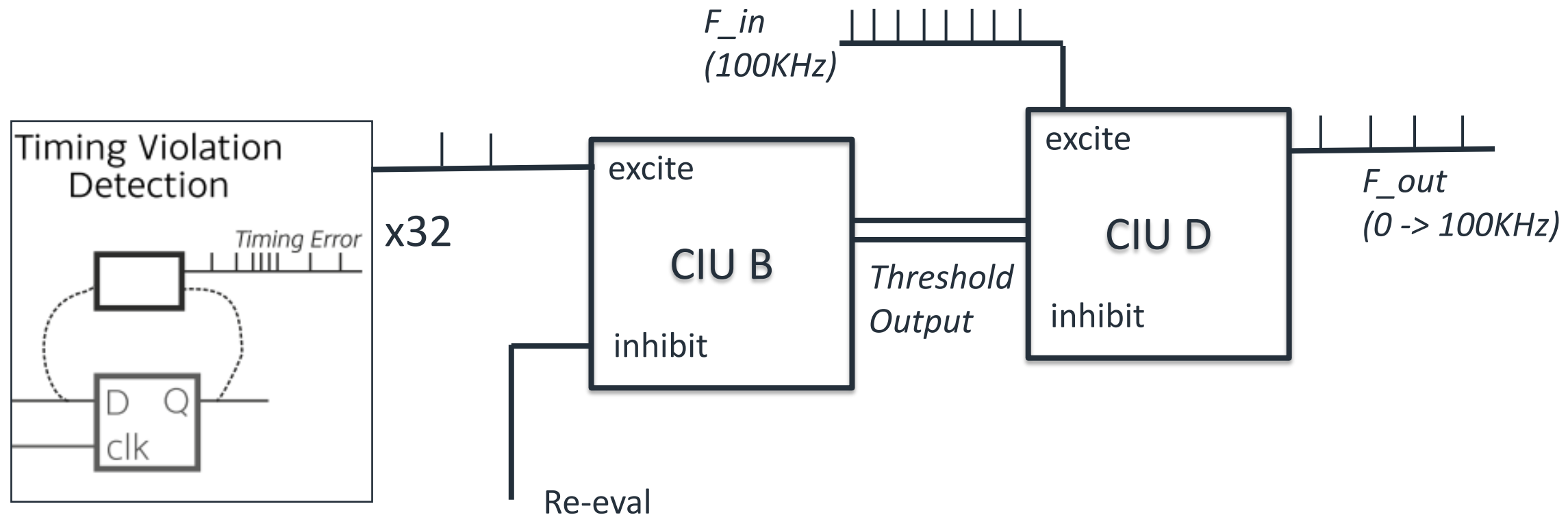


-> “Fundamental” decisions are made within this thresholder unit.

-> Hand mapped to FPGA slices, the “active elements” only requires two slices



# Experiment #3: Timing Fault Detection



-> As the number of timing faults increases, the internal count of threshold B will rise

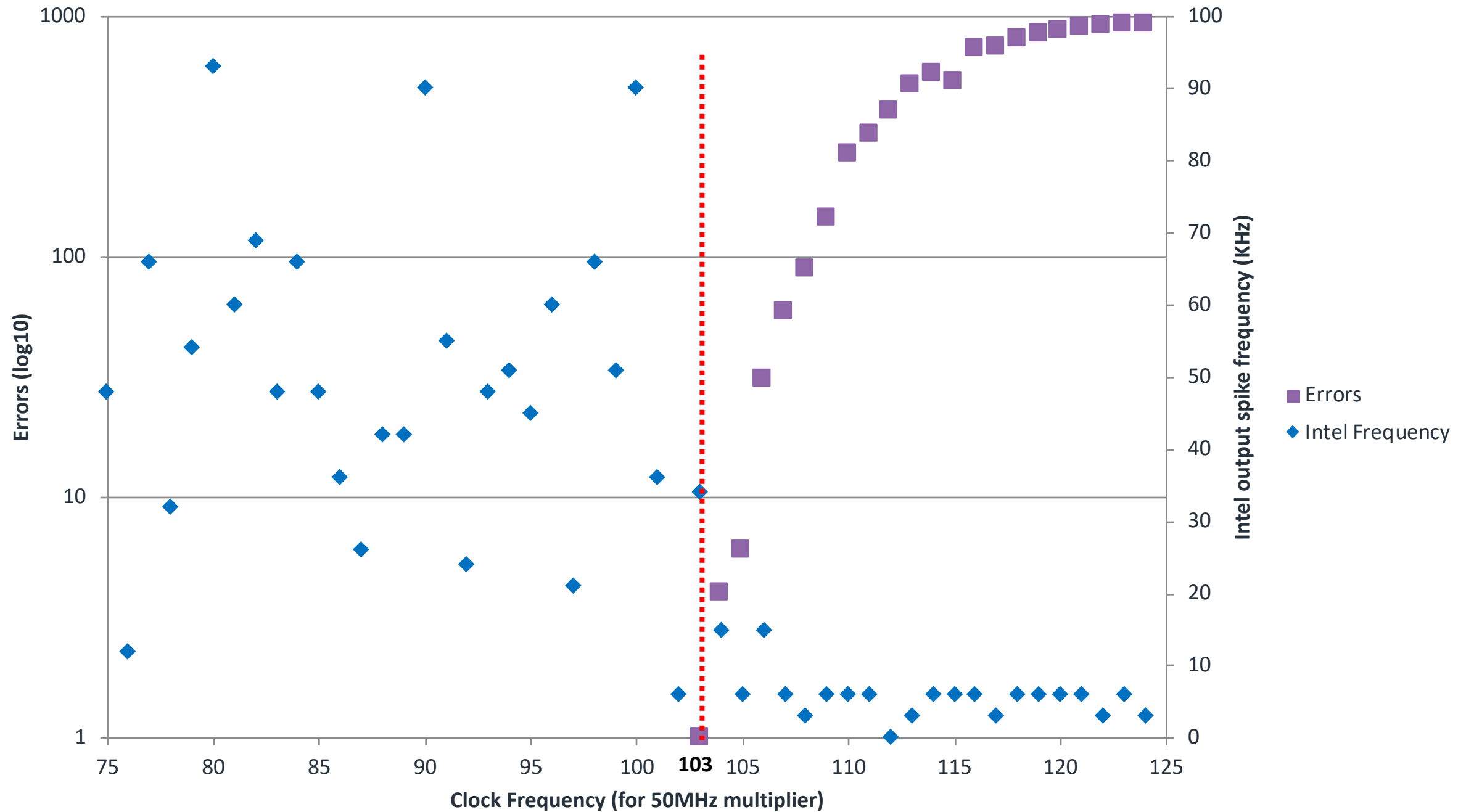
-> This will lower the output spike frequency of CIU D

-> Reevaluation is triggered by another part of the intelligence circuit

# Experiment #3: Timing Fault Detection

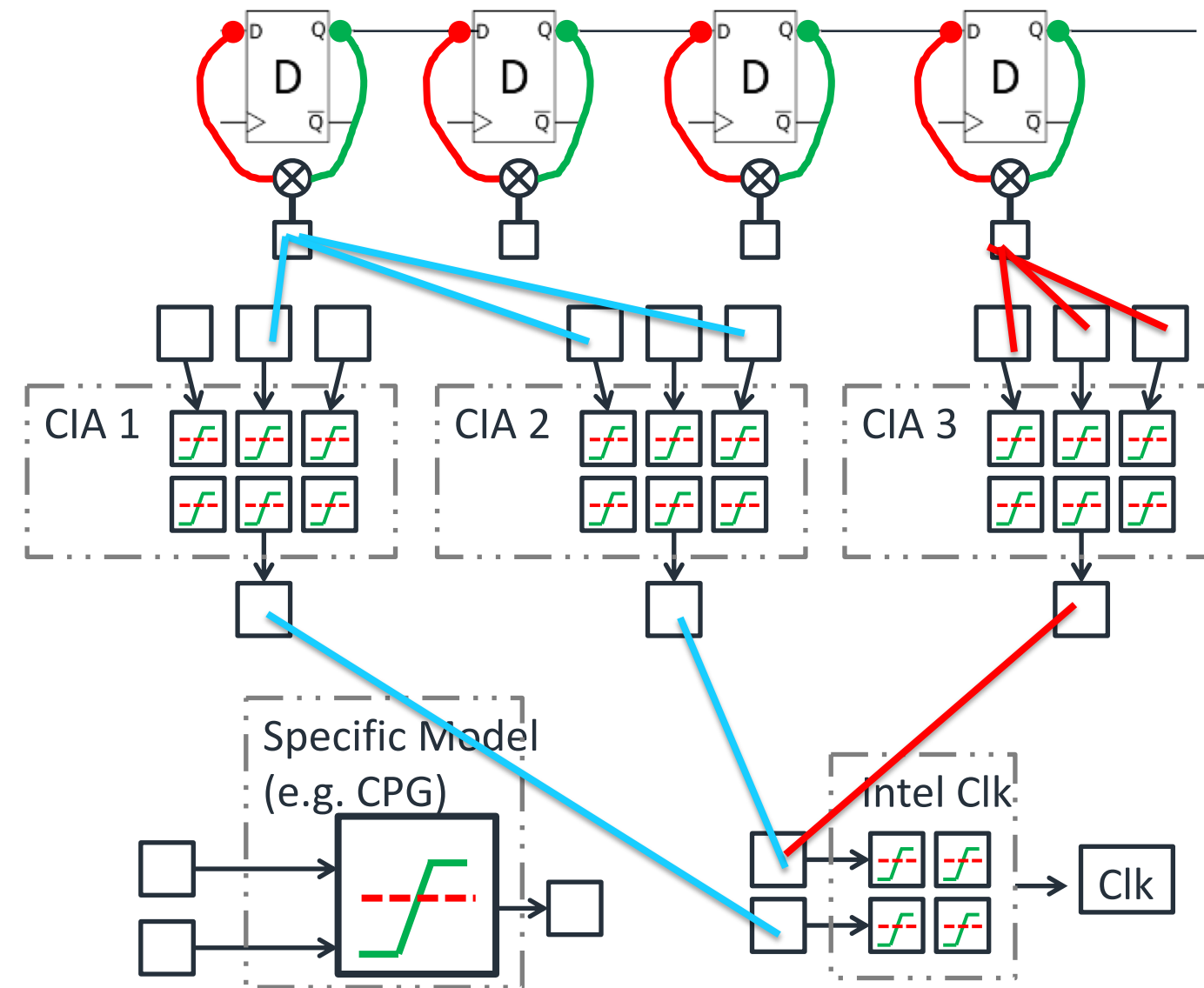


Errors for sweep 75MHz -> 125 MHz. Intel Frequency Suggested



# Next Steps

- Expand the capabilities of the digital neuron as required (e.g. multiple input integration, better self learning capabilities)
- Learn the thermal envelope of the DUT
- Expand to more complex SoCs, and how do we train such a network?
- In the natural nervous system - what is set by genes, what is set by development and what is learnt “online”?
- How simple organisms nervous systems grow and develop?





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# Any Questions?