

Formal architectural modelling

Opportunities and challenges

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joint work with

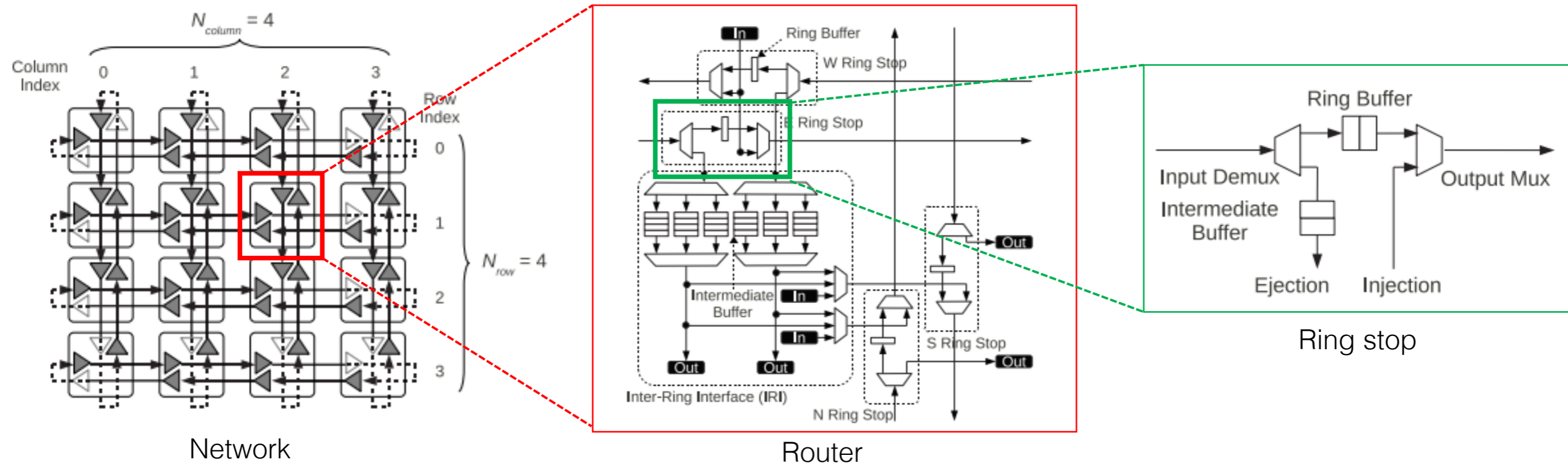
Perry van Wesel and Alexander Fedotov

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Where innovation starts

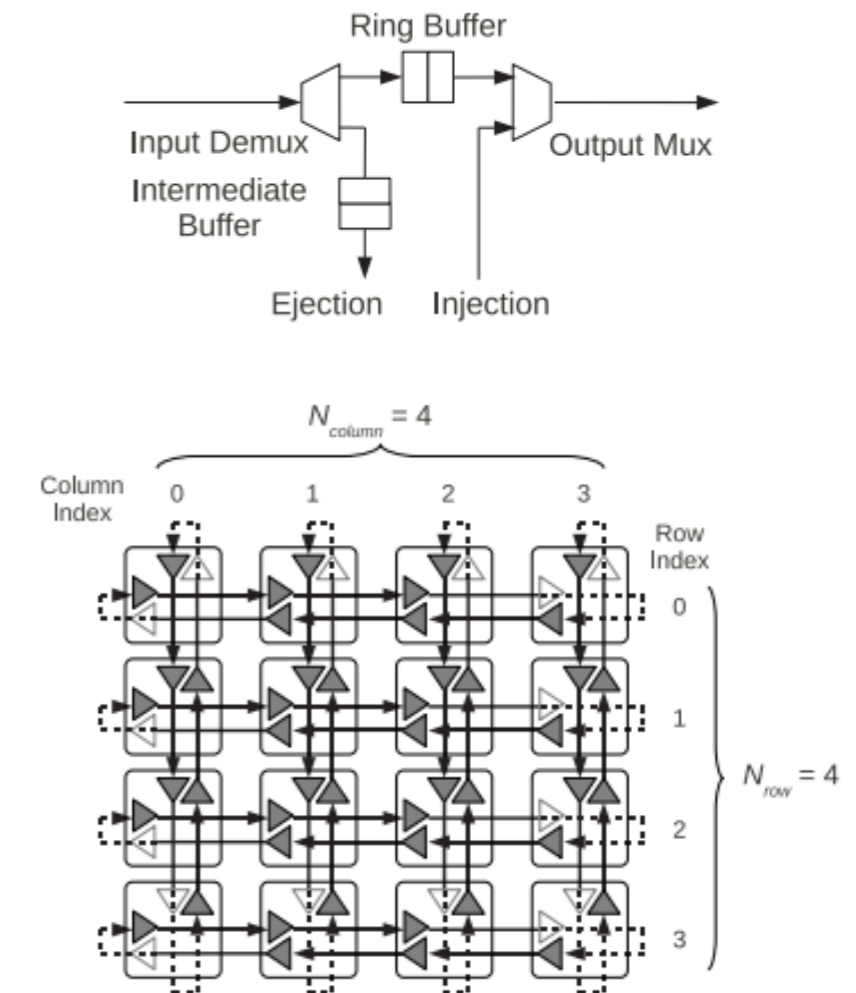
Architectural model example: TornadoNoC (I)



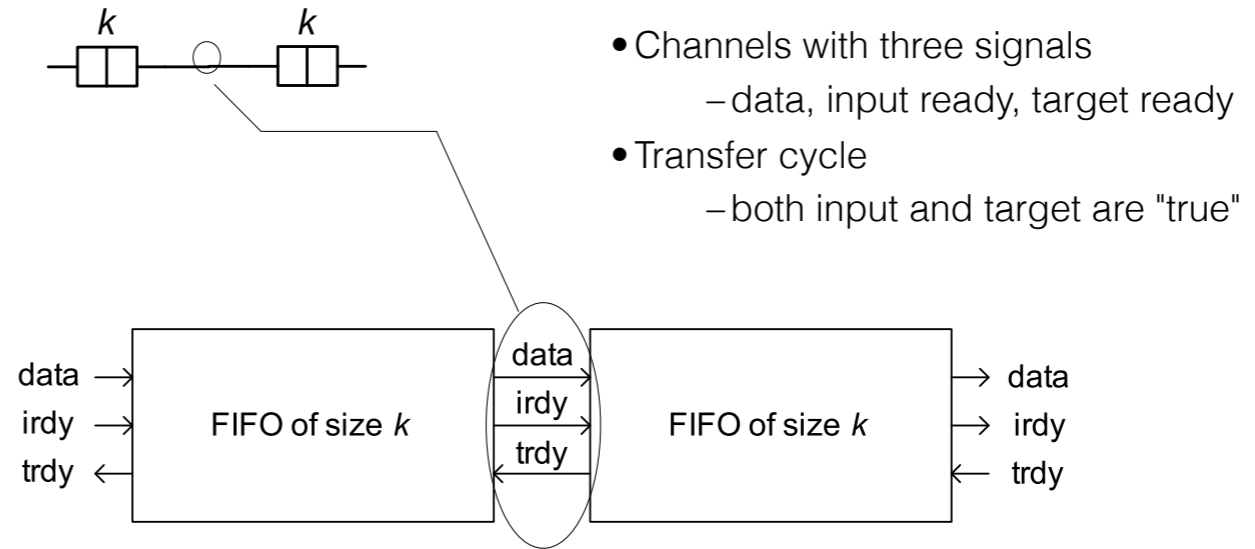
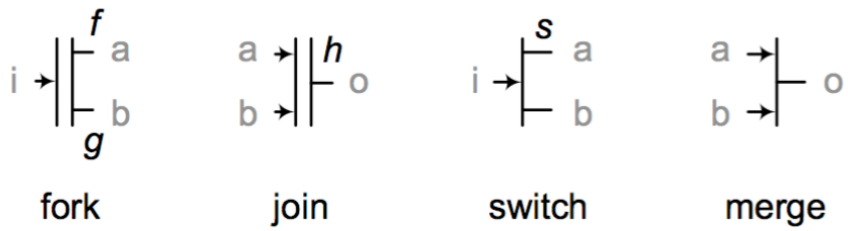
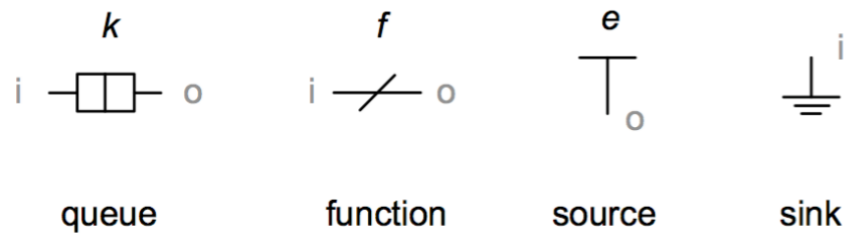
Architectural model example: TornadoNoC (II)

Additional mechanisms:

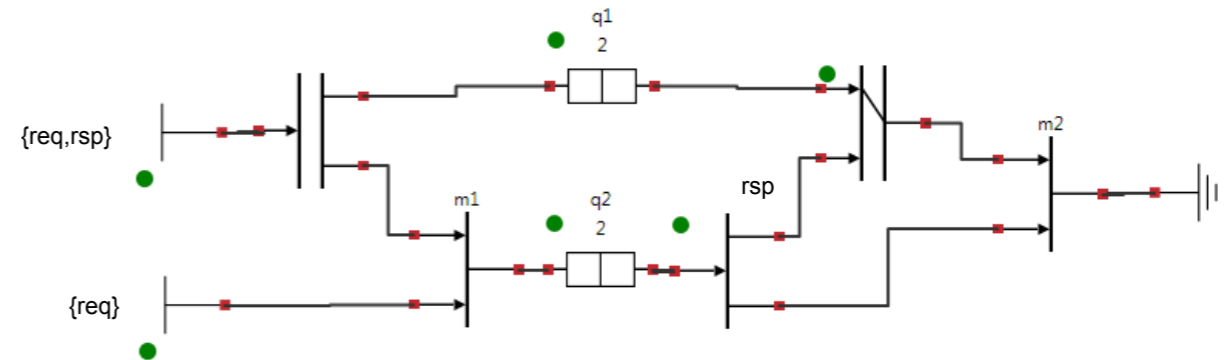
- Spillover – Travel an additional lap to avoid blocking other traffic.
- Sequence numbering – Limit the number of laps for one packet.
- Injection constraint – Limit number of packets in a ring.
- Inflation mechanism - Avoid protocol deadlock and starvation.



MaDL basic principles - Originates from Intel's xMAS



Notion of a "dead" channel: $F(c.irdy \ \& \ G \ ! \ c.trdy)$

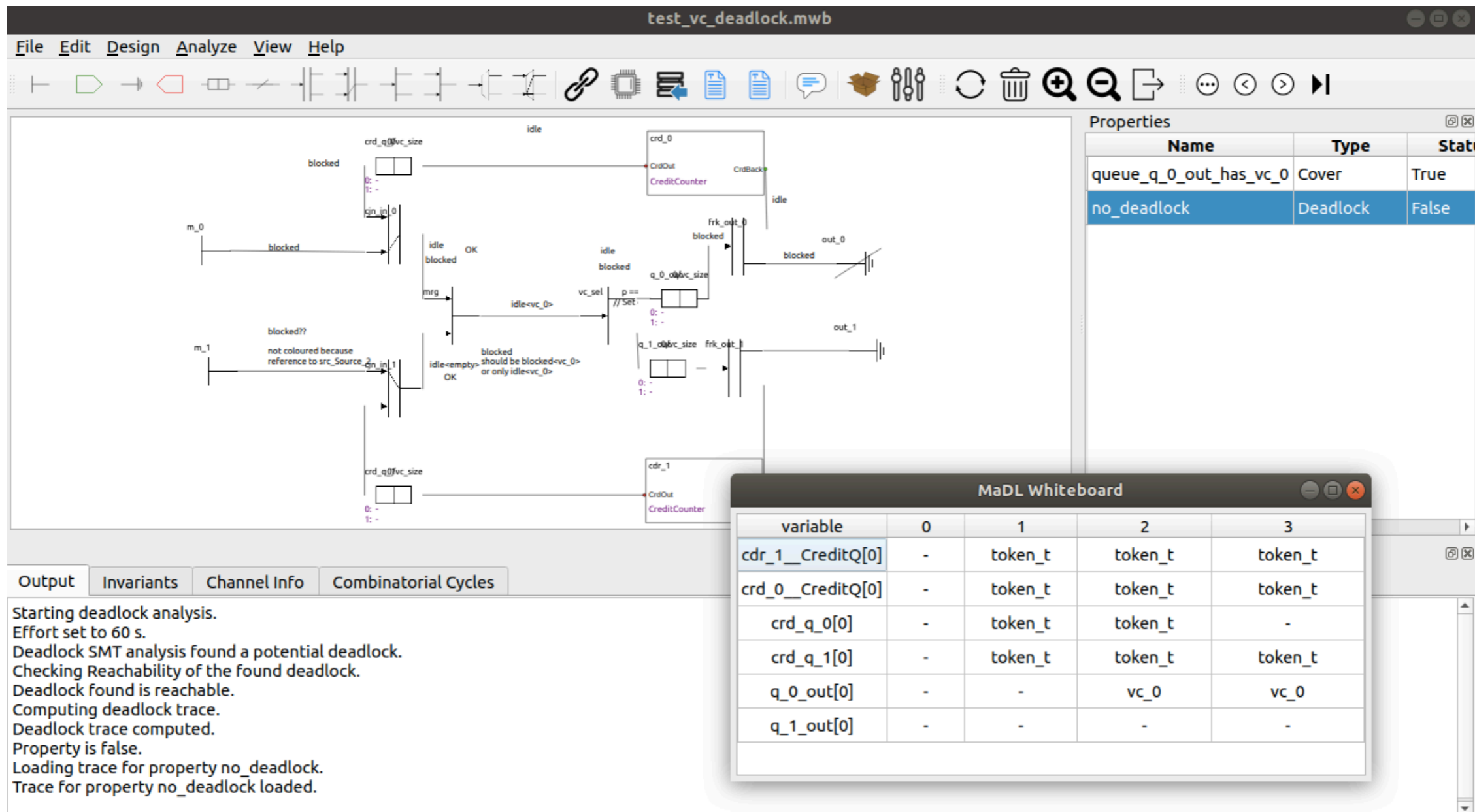


MaDL Design and Verification Environment

```

param int QSIZE;
const pkt;
chan src := Source(pkt);
chan one, two := Fork(src);
chan long := Queue(QSIZE, Queue(QSIZE, one));
chan short := Queue(QSIZE, two);
Sink(CtrlJoin(long, short));
    
```

<https://github.com/MaDL-DVT/madl-dvt>



test_vc_deadlock.mwb

File Edit Design Analyze View Help

Properties

Name	Type	Status
queue_q_0_out_has_vc_0	Cover	True
no_deadlock	Deadlock	False

MaDL Whiteboard

variable	0	1	2	3
cdr_1__CreditQ[0]	-	token_t	token_t	token_t
crd_0__CreditQ[0]	-	token_t	token_t	token_t
crd_q_0[0]	-	token_t	token_t	-
crd_q_1[0]	-	token_t	token_t	token_t
q_0_out[0]	-	-	vc_0	vc_0
q_1_out[0]	-	-	-	-

Output Invariants Channel Info Combinatorial Cycles

Starting deadlock analysis.
 Effort set to 60 s.
 Deadlock SMT analysis found a potential deadlock.
 Checking Reachability of the found deadlock.
 Deadlock found is reachable.
 Computing deadlock trace.
 Deadlock trace computed.
 Property is false.
 Loading trace for property no_deadlock.
 Trace for property no_deadlock loaded.

MaDL Ring Extension - GuardQueue primitive

Modelling the injection constraint with the GuardQueue:

‘Only inject if the local buffer is empty’

$$i_b.trdy = \neg Full(gq) \wedge sel == 0$$

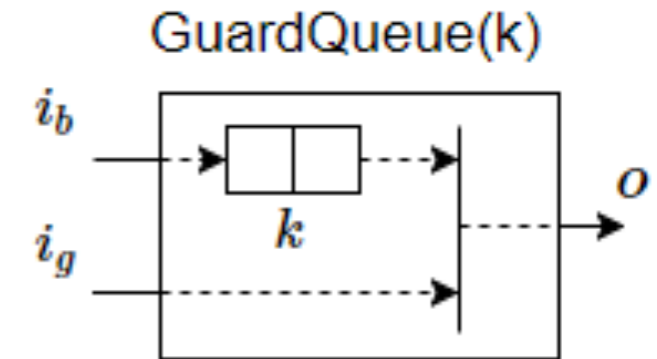
$$i_g.trdy = o.trdy \wedge Empty(gq) \wedge sel == 1$$

$$o.irdy = (sel == 0 \wedge \neg Empty(gq)) \vee (Empty(gq) \wedge i_g.irdy \wedge sel == 1)$$

$$block(i_b, c) = Full(gq) \wedge block(o, gq.head)$$

$$block(i_g, c) = block(o, c) \vee (sel == 0 \wedge Full(gq) \wedge block(o, gq.head)) \\ \vee never\ empty(gq)$$

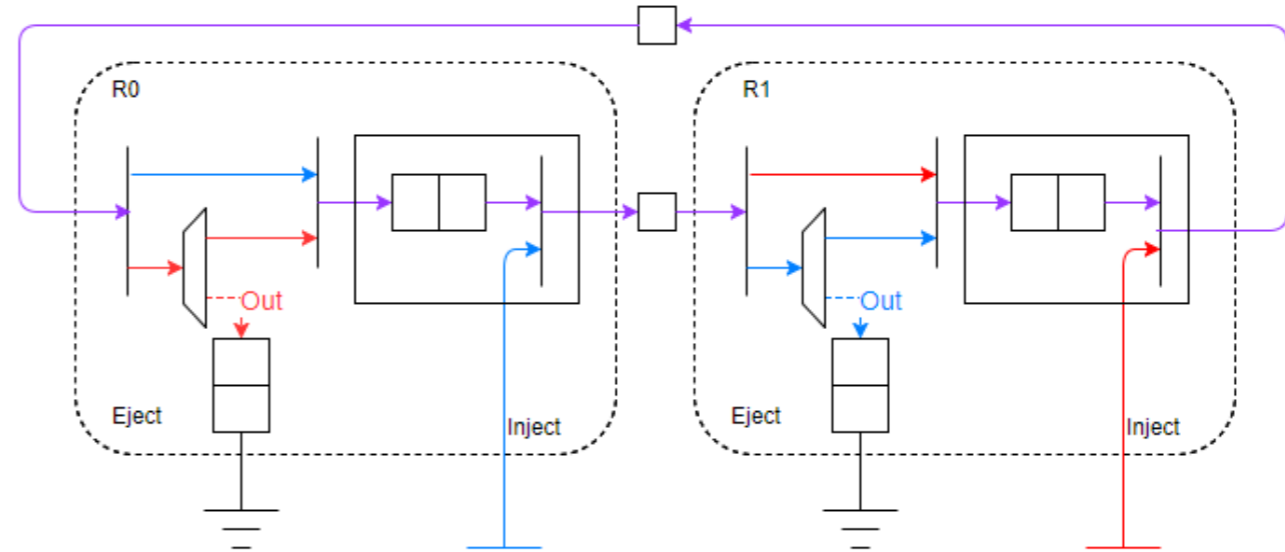
$$idle(o, c) = (idle(i_b, c) \wedge idle(i_g, c)) \vee (idle(i_b, c) \wedge never\ empty(gq)) \\ \vee \exists_{c' \in C \setminus c} block(o, c')$$



MaDL Ring Extension - Ring invariants

Ring $R = (D, X, I, O)$

- D: data colours
- X: Channels
- I: Inputs
- O: Outputs



Ring invariant for ring R:

$$\text{occ}(R) \leq \text{cap}(R) - x$$

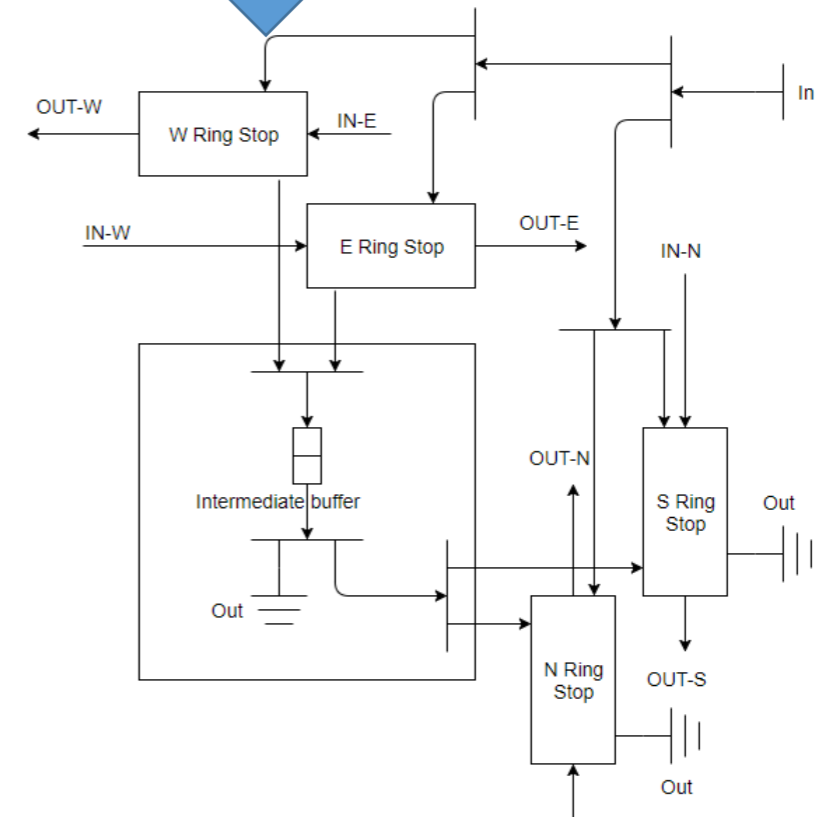
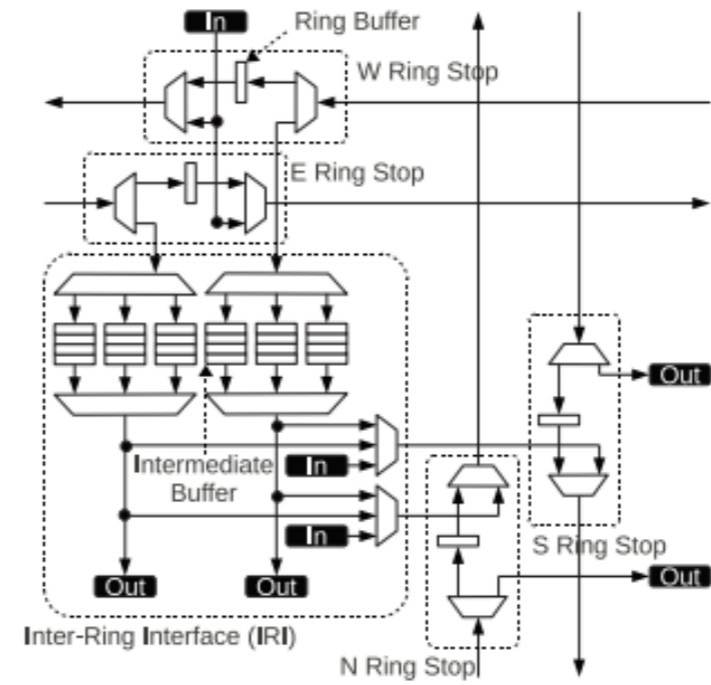
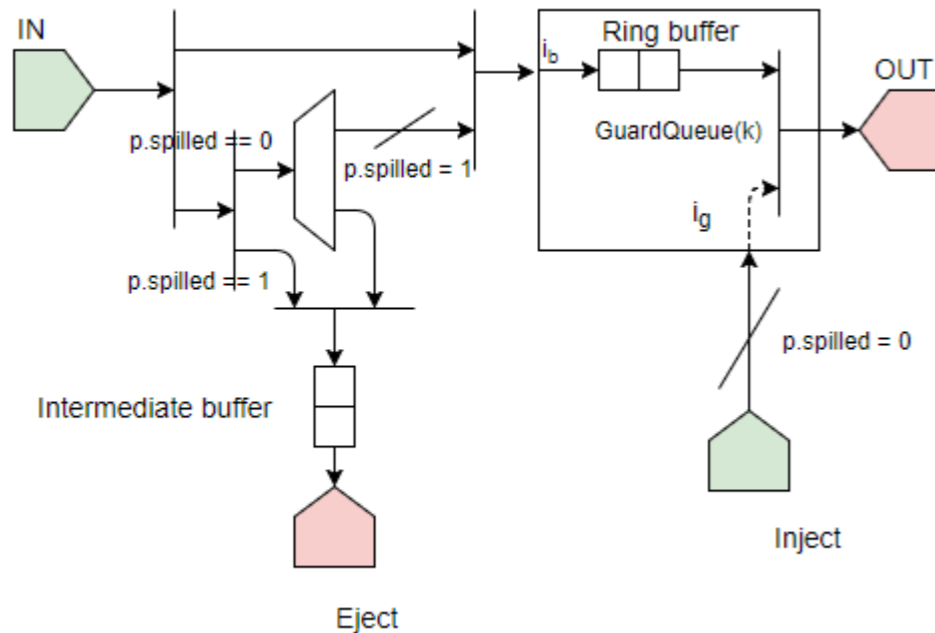
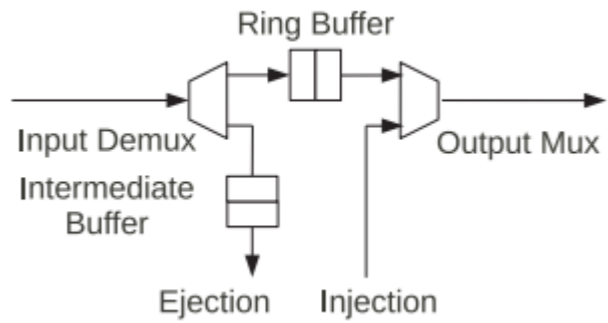
where x is the smallest capacity over all guard queues in the ring.

$(\{\text{red}\}, \{*\text{U}*\}, \{\text{R1_Inject}\}, \{\text{R0_Out}\})$
 $(\{\text{blue}\}, \{*\text{U}*\}, \{\text{R0_Inject}\}, \{\text{R1_Out}\})$

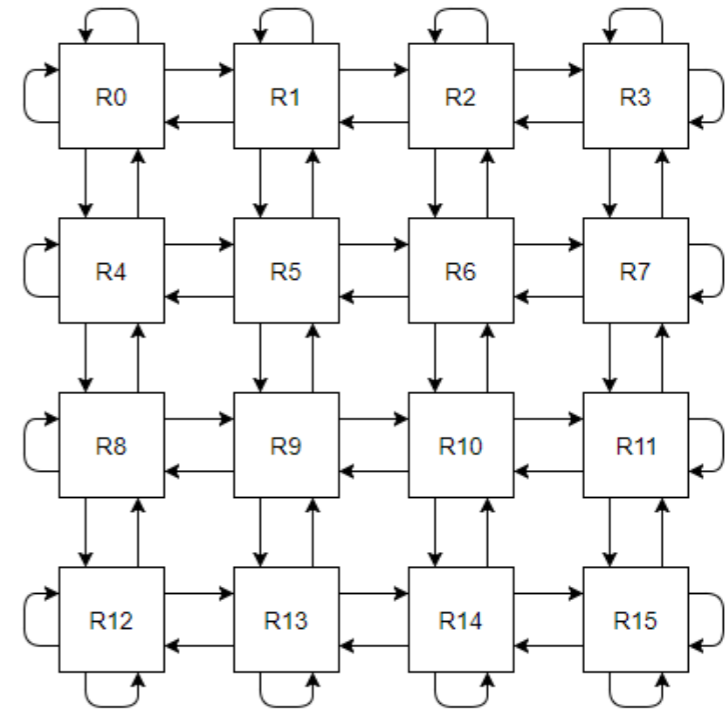
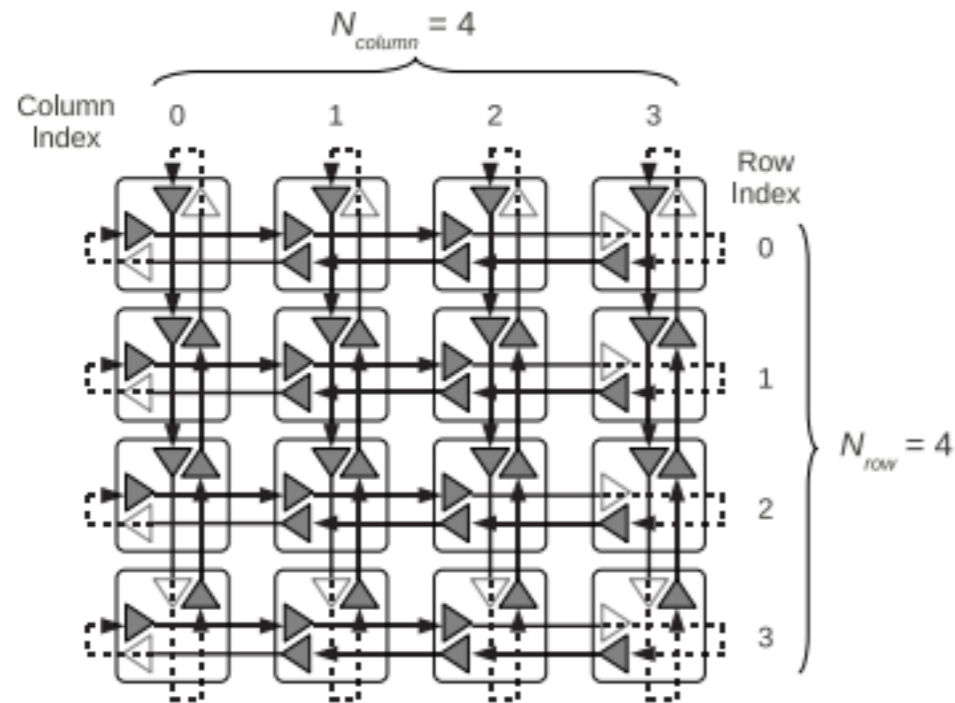


$(\{\text{red,blue}\}, \{*\text{U}*\text{U}*\}, \{\text{R0_Inject}, \text{R1_Inject}\}, \{\text{R0_Out}, \text{R1_Out}\})$

MaDL model of the TornadoNoC blocks

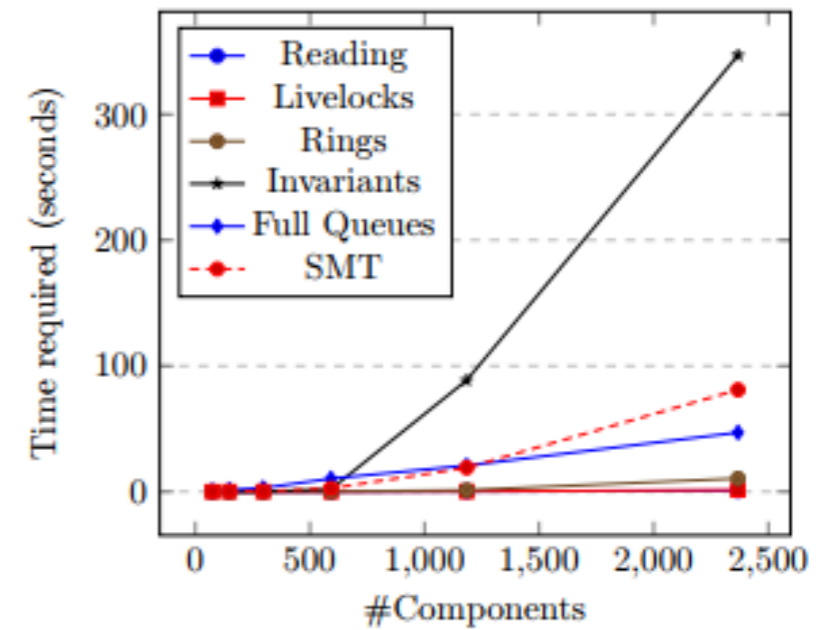


MaDL model and analysis results



Layout	#Components	Rings	Deadlock	Verification time
2×1	98	1	No	1.4s
2×2	196	4	No	2.8s
4×2	392	6	No	8.0s
4×4	784	8	No	59.7s
4×8	1568	12	No	970s
8×8	3136	16	No	3691s

Individual MaDL steps



MaDL model and analysis results - Discussion

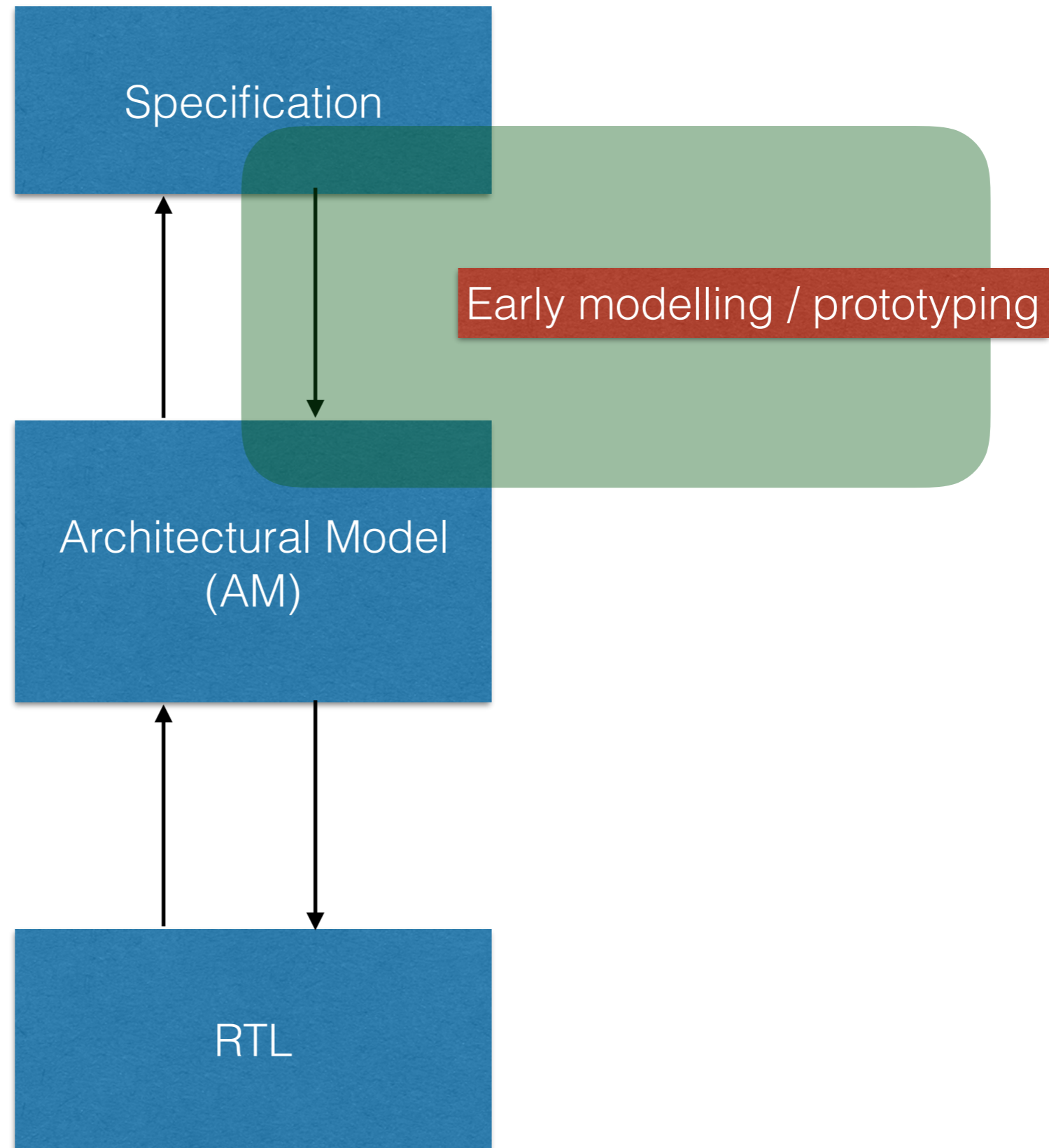
Conclusion:

- Ring networks can now be analysed without finding the trivial all-queues-are-full deadlock.
- TornadoNoC contains a potential deadlock when using credit-flow control
- The MaDL GuardQueue avoids this deadlock.

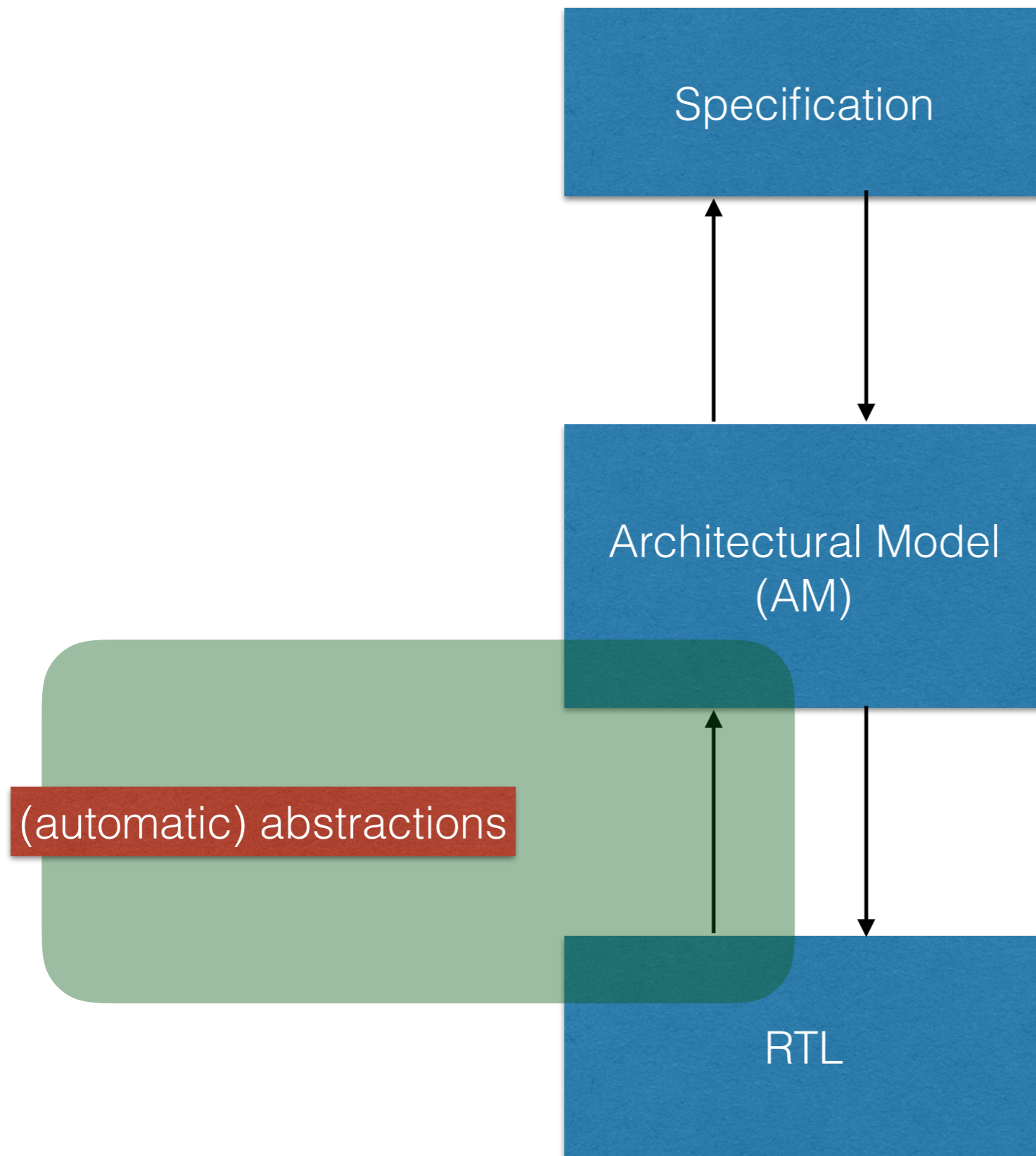
Future Work

- More detailed model of TornadoNOC, including Inflation Mechanism
- Proof of other properties like message ordering, starvation and livelock freedom, etc.

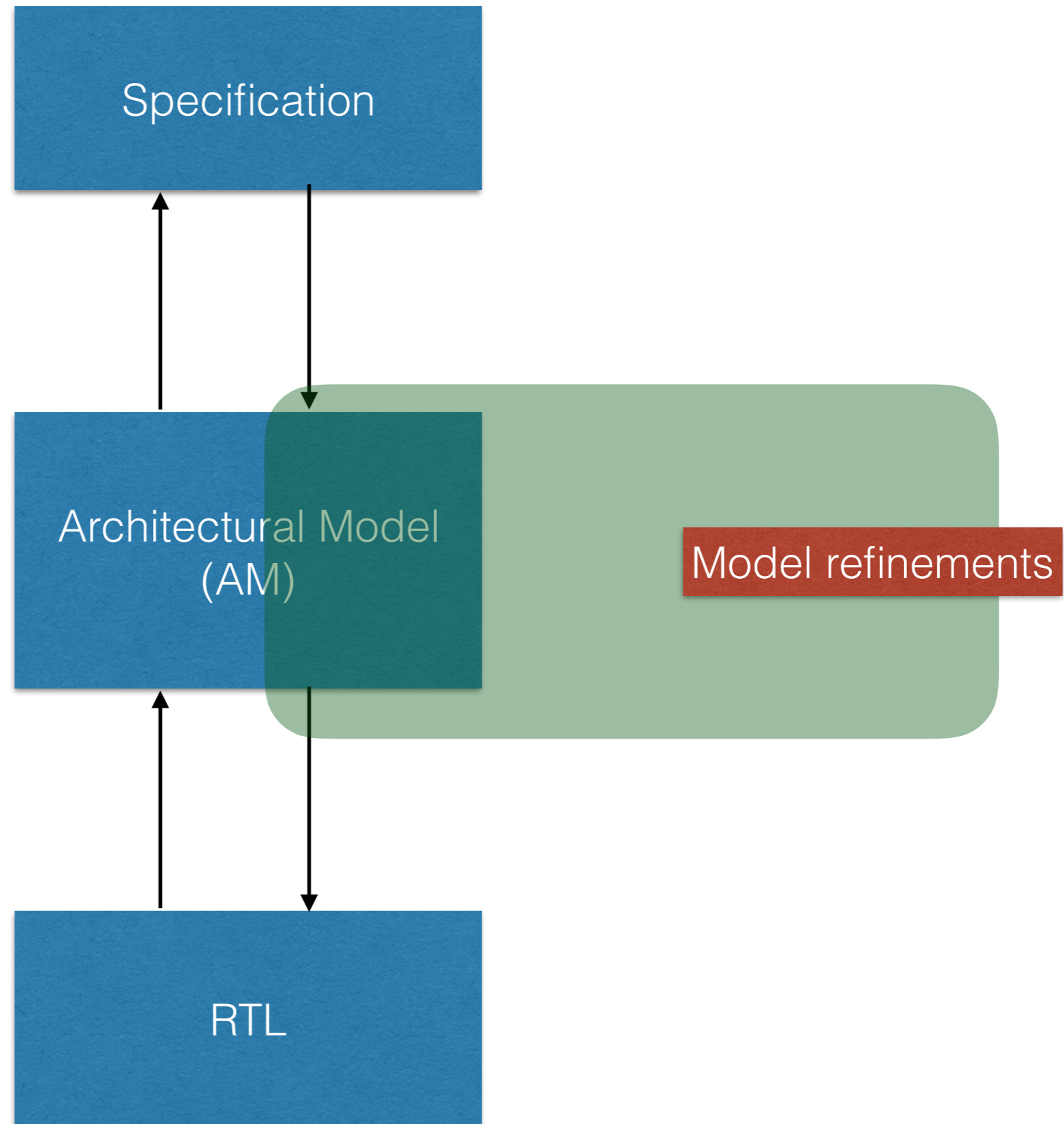
Architectural modelling and analysis - Reflection



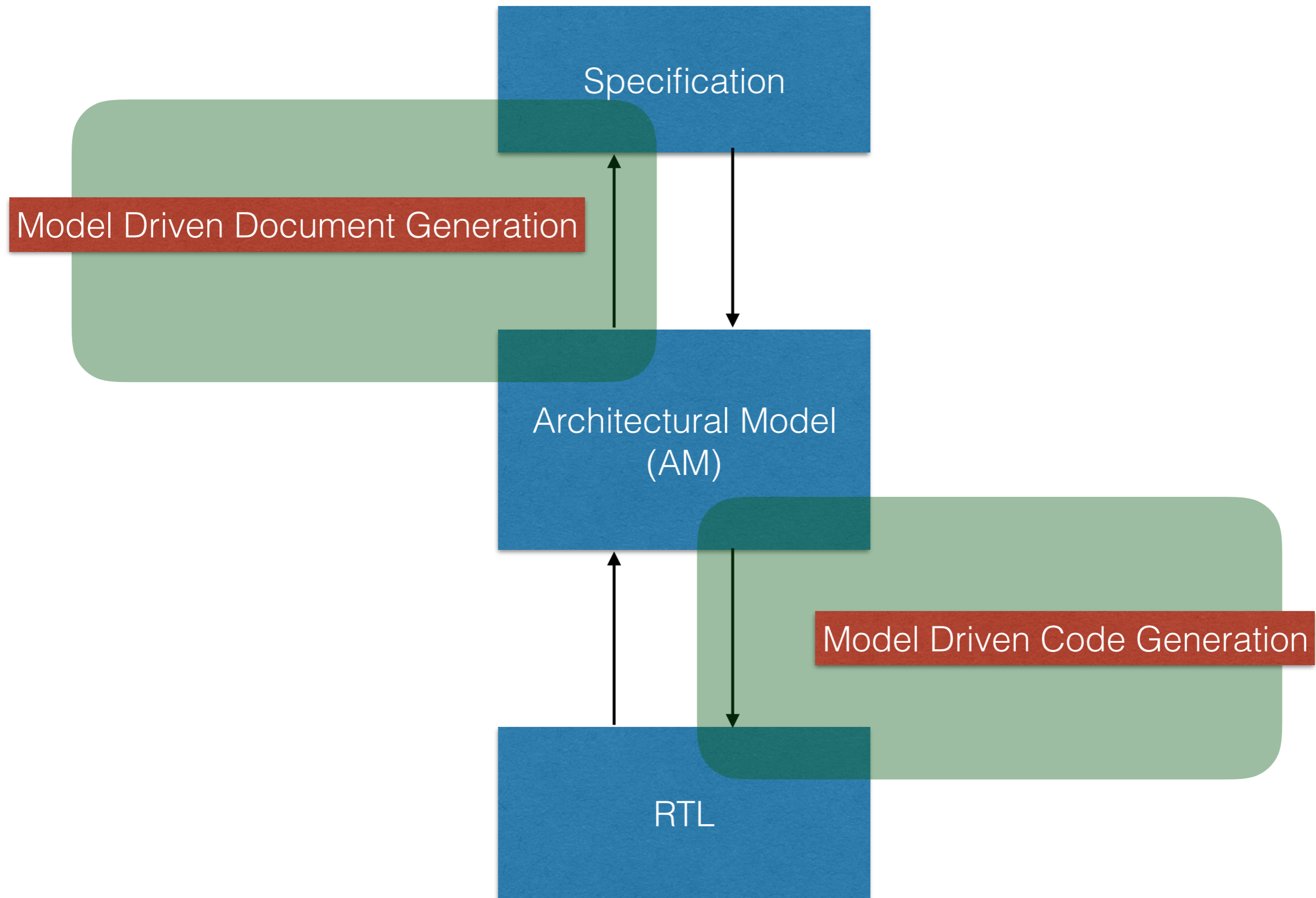
Architectural modelling and analysis - Reflection



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Architectural modelling and analysis - Reflection



Thanks!