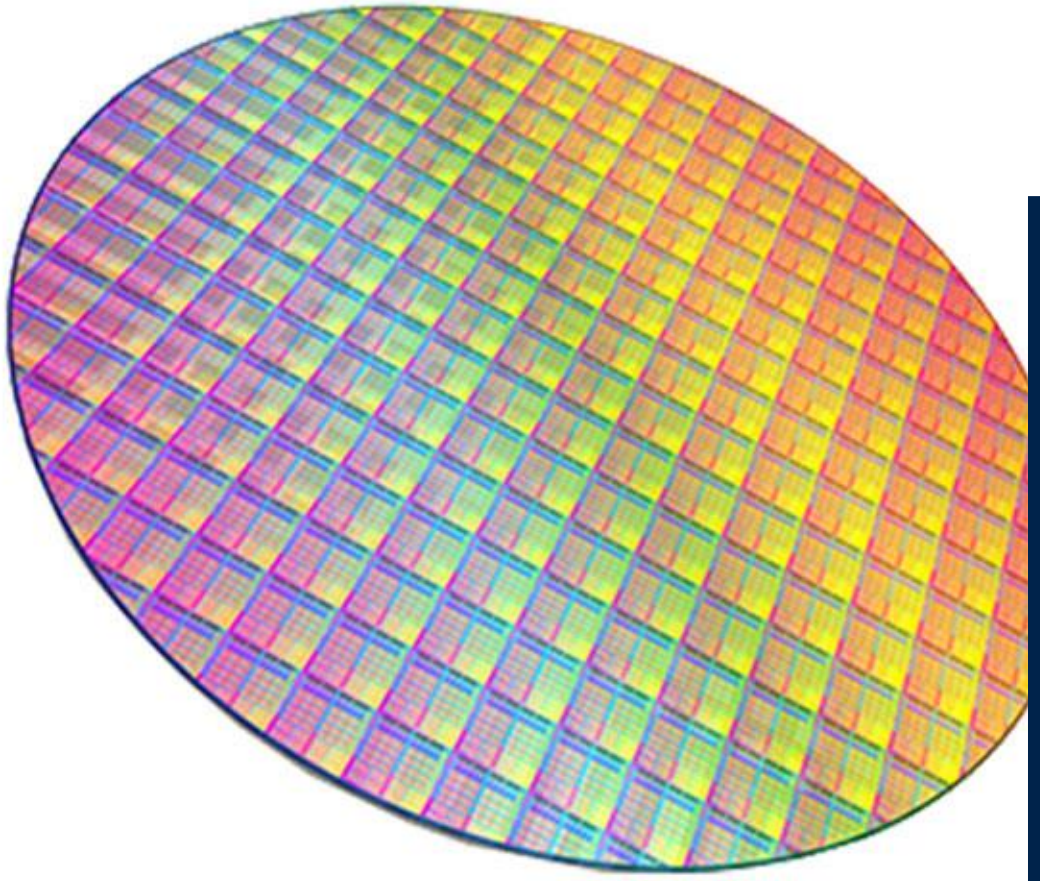

Physical Design & Signoff

FDP University Program 2023

Sanjay Kumar

Supported by

Let me introduce myself

- With 13+ years of experience in semiconductor industry.
- Graduated from NIT Calicut in Electronics and Communication Engineering.
- Currently managing the SoC Physical Design team for General Purpose Micro (GPM) products in ST, Greater Noida.
- Contributed to multiple successful tape-outs of products ranging from 180nm to 5nm technologies in consumer, automotive and industrial application.
- As part of SoC Physical Design, I have driven key initiatives in implementation of high-speed complex subsystems, and critical IPs for best-in-class power, performance, and area.
- In addition, have multiple publications / presentations and tech poster in various forums.

Agenda

- # ASIC Design Flow
- # Physical Design Introduction
- # Synthesis
- # Floorplan (IO-Ring)
- # Placement and Routing
- # Physical Signoff
- # Timing Signoff
- # Power & IR Drop Analysis

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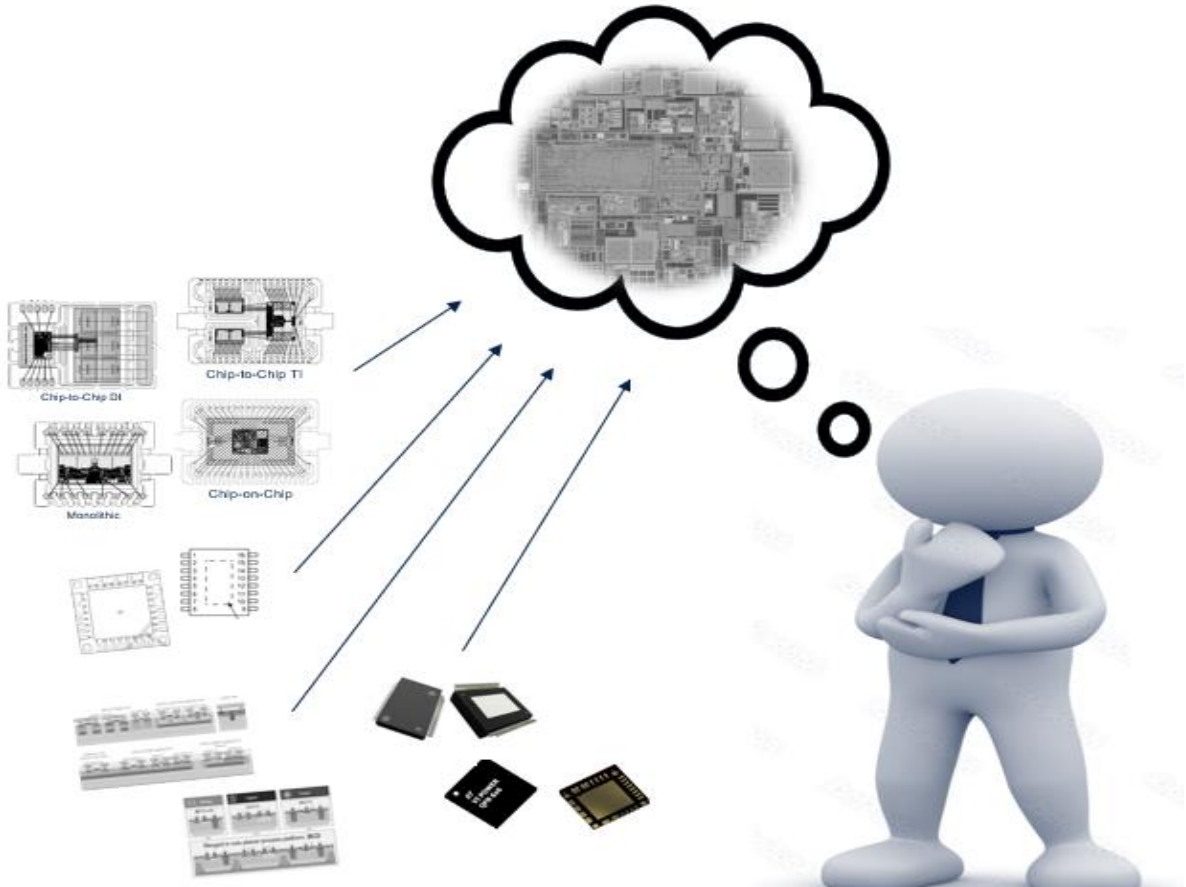
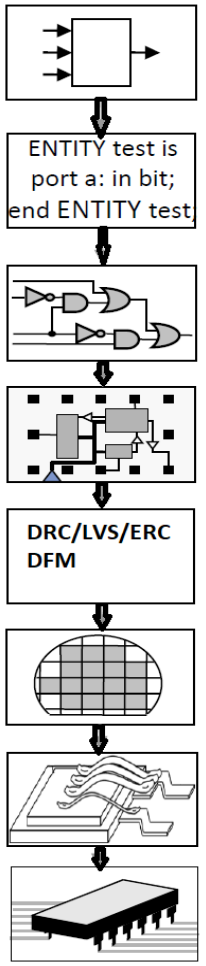
ASIC Design Flow





System Specification
Architectural Design
RTL Design & Verification
Synthesize the Design
Placement & Routing
Timing & Physical Signoff
Mask Preparation
Fabrication
Packaging & testing
Chip

Physical Design

Partitioning
Floor Planning
Placement
CTS
Routing

Parasitic Extractions
Physical Verification
Formal Verification
Static Timing Analysis
IR Drop & Power Analysis

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Physical **D**esign Team Mission

Physically implement most optimized system-on-chip designs while meeting project schedule, high level Power Performance Area targets/budgets and package constraints.

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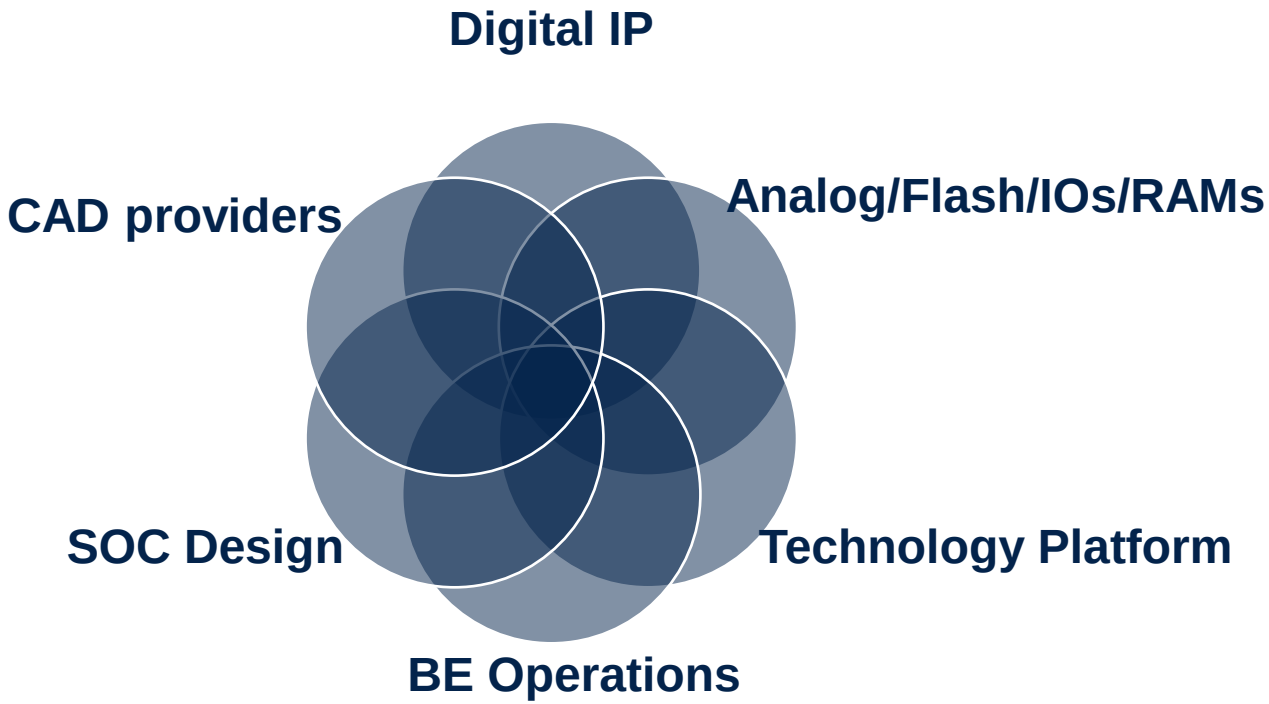
Physical **D**esign Team Engagements

- Interface with…
  - SOC FE team to define PPA budgets
  - Technology providers (ST or external)
  - Package solution team
- Define & optimize implementation methodologies
- Define the right toolset to support these methodologies
- Define & deliver the SOC implementation schedule & resource plan
- Propose IP/SOC changes for better and most optimized SOC
- Top level planning/pad-ring construction/Analog integration
- Physical signoff checks
- Packaging assessment



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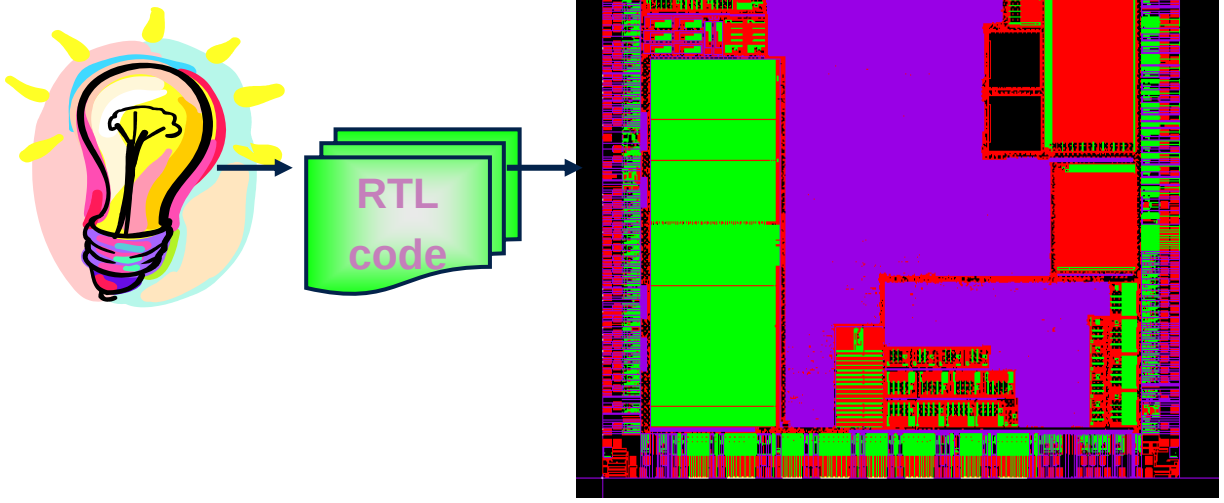
Physical Design flow - scope

***Front End* Design must guarantee:**

- Functionality
- Testability
- Reliability



***Back End* Design needs:**

- Chip architecture understanding
- Front end know how
- Technology information
- Implementation and Production steps know how
- Knowledge of testability requirements
- Backend CAD tools deep knowledge

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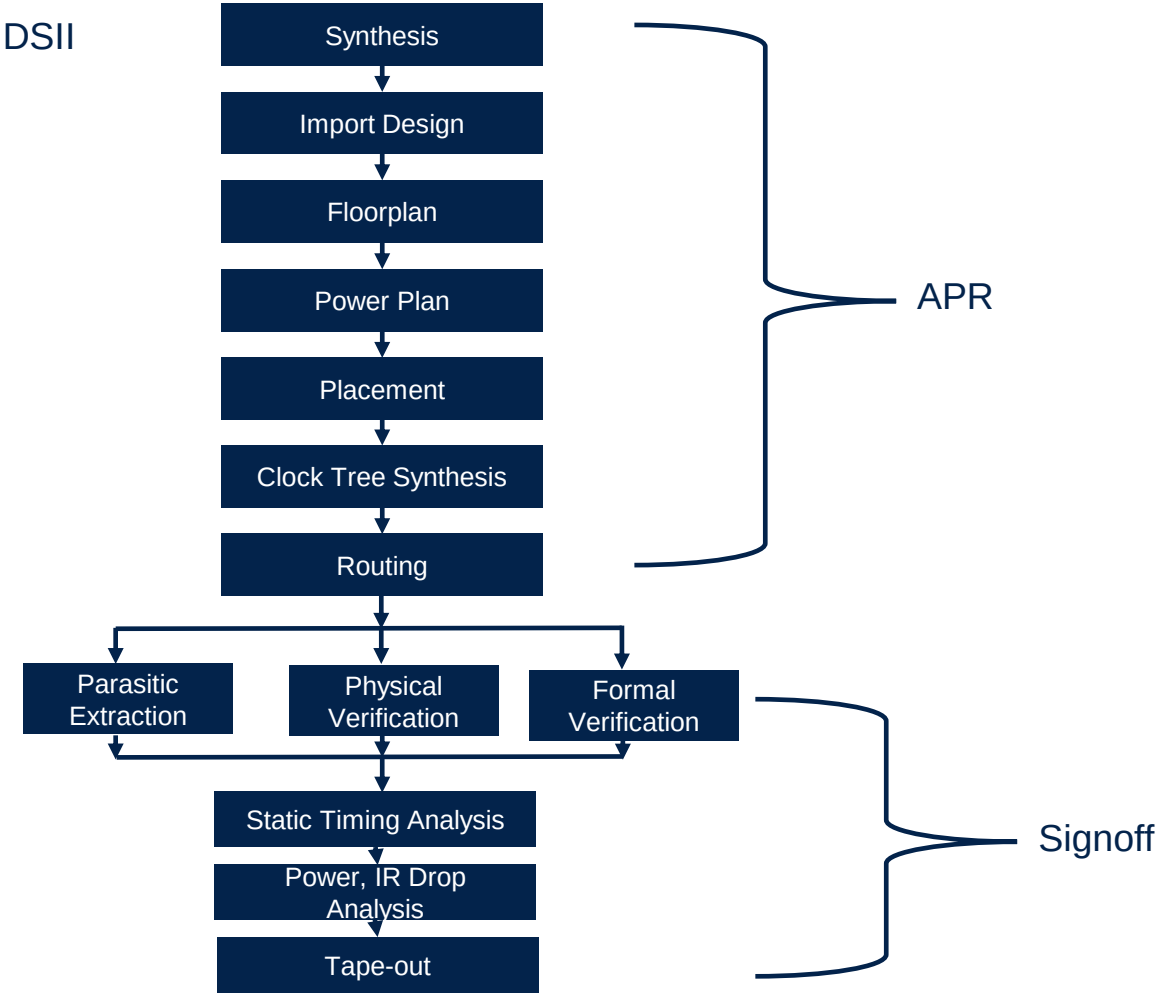
Physical Design Introduction

- Structural representation to Physical Design i.e., RTL to GDSII
- Stages:
  - Synthesis
  - Placement and Routing (PnR)
  - Signoff
- Objectives:
  - Timing
  - Congestion
  - Area
  - Power
- Possible Issues:
  - Timing Violations
  - Congestion Issues
  - Design Rule Violations



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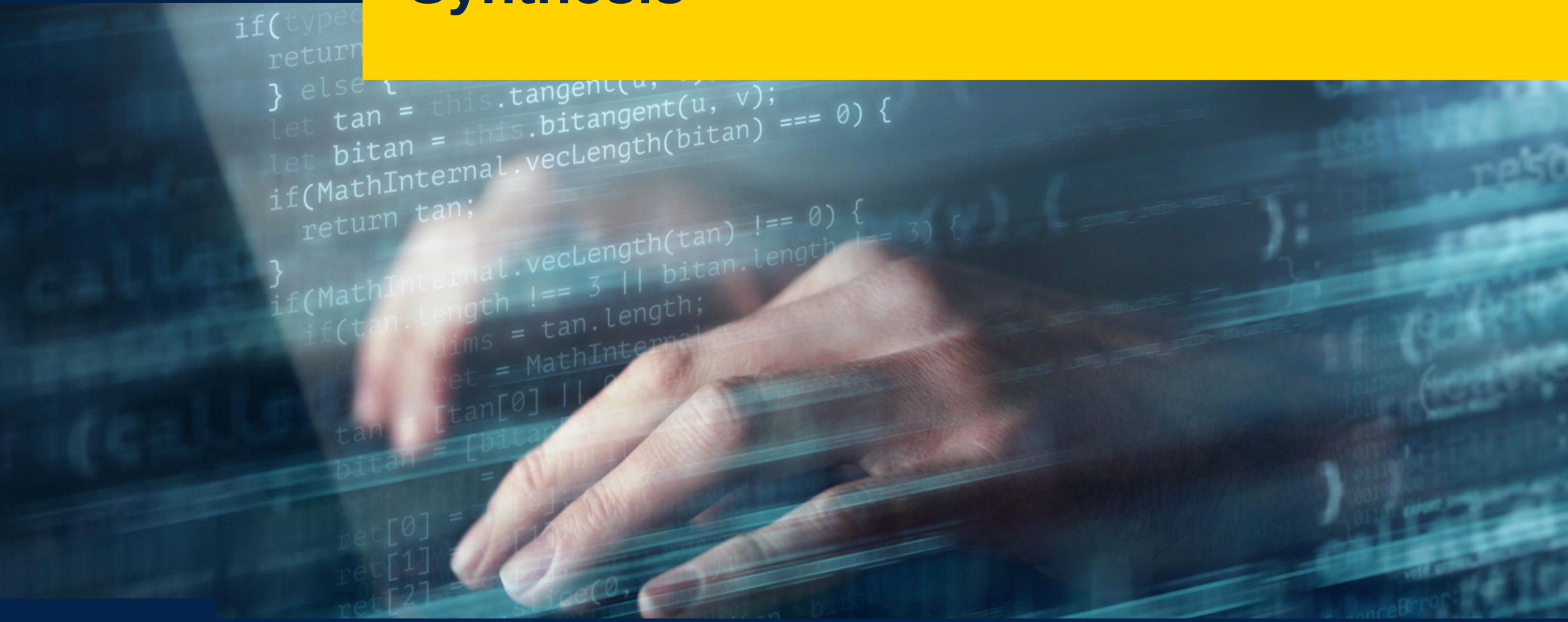
Synthesis



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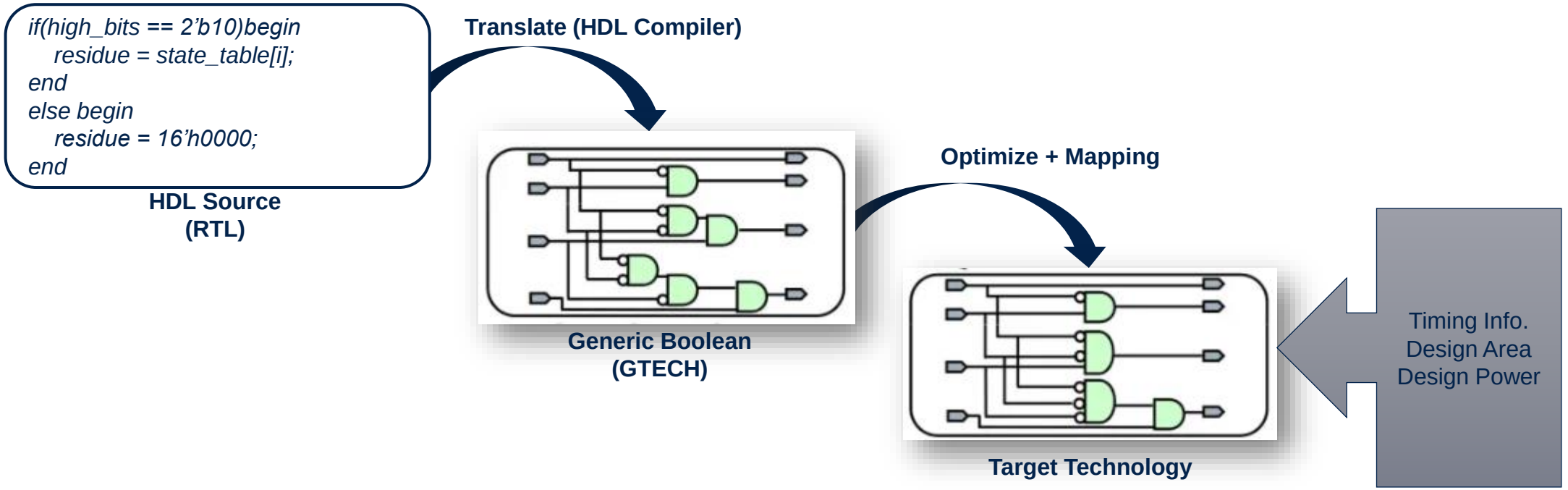
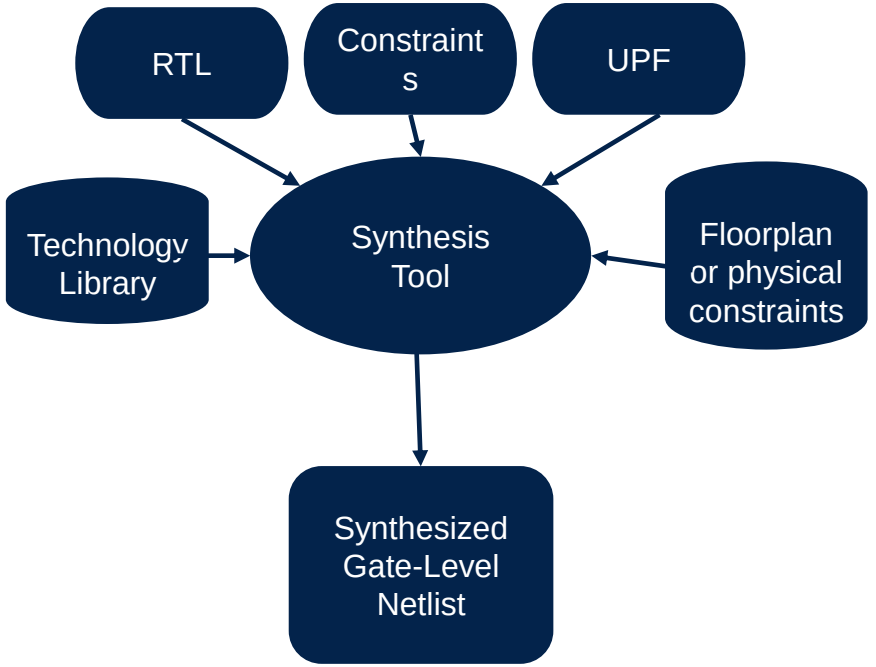
Synthesis (1/2)

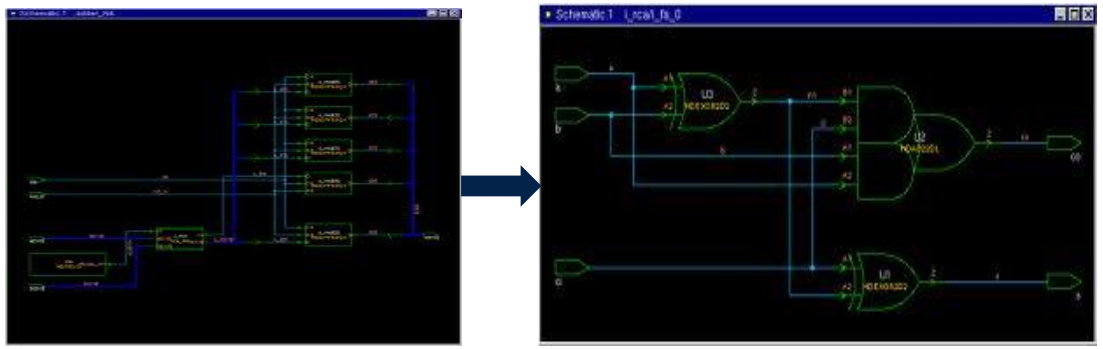
- Process of transferring HDL to Gate-level netlist and described as
  - Synthesis = Translation + Logic Optimization + Mapping
- HDL => Generic Boolean Logic => Optimization => Mapping => Netlist



Synthesis (2/2)

- Goal of Synthesis
  - To get a Gate-level Netlist
  - Logic Optimization
  - Inserting DFT Logic
  - Logic Equivalence between RTL and Netlist should be maintained.
- Inputs of Synthesis
  - RTL: HDL files
  - Library views
  - Constraints
  - Floorplan DEF (for physical synthesis)
  - UPF (Power intent for power aware synthesis)
- Outputs of Synthesis
  - Netlist
  - QoR Reports (timings, area, cell count etc.)
  - UPF





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Library Views (1/2)

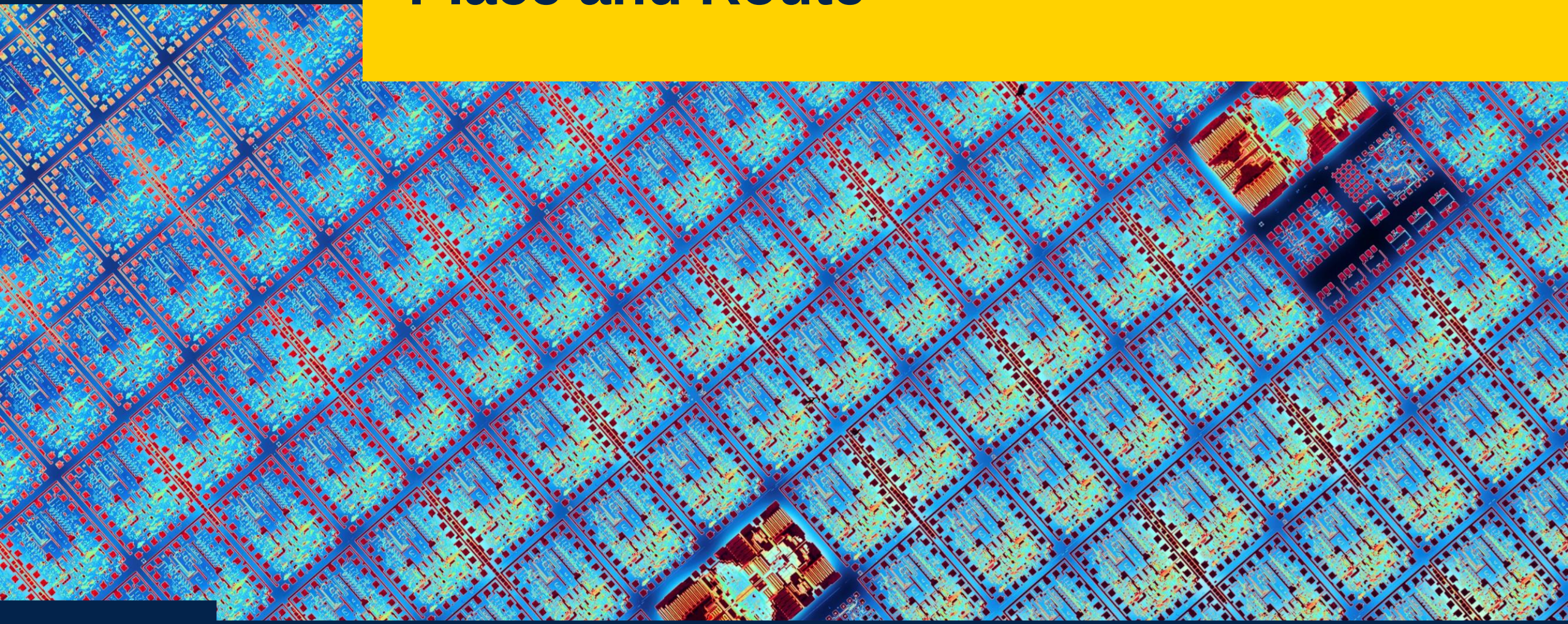
- LIBRARY: Consolidated Data for Use in Designing a System On Chip.
- Various Types of Libraries:
  - CORE Libraries
  - IO Libraries
  - Memories
  - Analog and Mixed Signal

- CORE Libraries:
  - Group of basic logic functional cells, called std cells.
  - Type of cells: AND, OR, Flops, Latch etc.
  - Physical/logic/timing/electric models are present
- IO Libraries:
  - IO buffers are designed for specific process technology.
  - Power/Ground IOs for chip supply
  - IOs are with protection of ESD events.

- Memories:
  - Memories like SRAM, DRAM, ROM etc.
  - Implemented as generator and configure various size of memory.
  - Supports many features like redundancy, masking etc.
- Analog and Mixed Signal Libraries:
  - These IPs provides unique functions
  - Examples are PLL, ADC, DAC, USB, SATA etc

- Types of Views:
  - HDL models
  - Timing Libs
  - Schematic
  - Symbol
  - Layout (LEF/GDSII)
  - Abstract and more …

Place and Route



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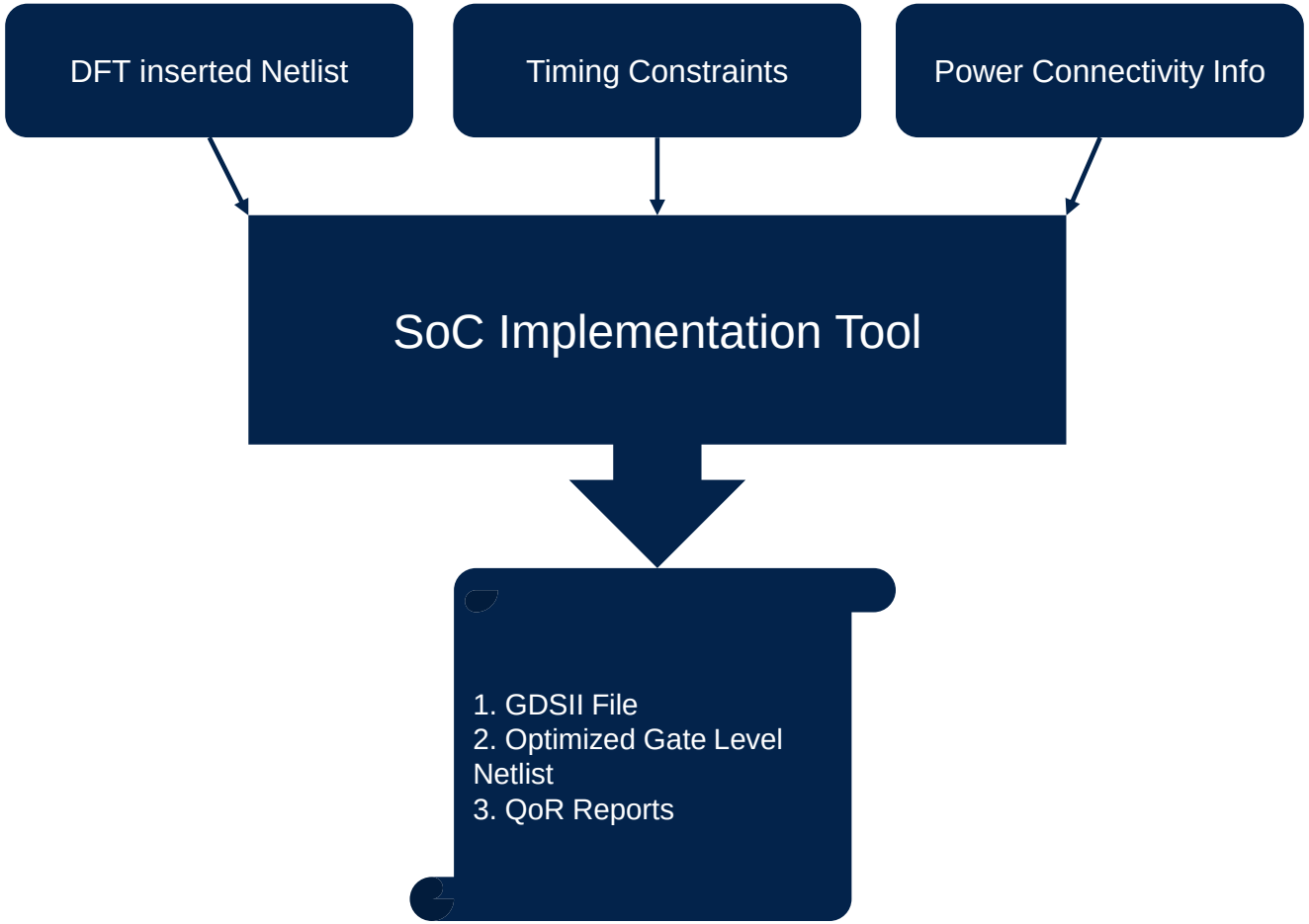
PnR Inputs (1/2)

- Netlist/Verilog
  - Std. cell instance name & drive strength
  - Macros & memories instances
  - Design module definitions
  - Interconnection details
- Constraints
  - Timing Constraints like Clock Definitions (clock period, duty cycle) and uncertainties.
  - Timing Exceptions (False Paths, Asynchronous Paths).
  - Delay Constraints (Latency, Input Delay, Input Transition, Output Load and Output Transition)
  - Design rule constraints like Max. Cap / Transition / Fanout.
- Liberty Timing Files
  - Cell Logical View / The timing Library
  - Std Cell Lib, Macro Lib, IO lib
  - Gate Delay
- Liberty Exchange Format (LEF)
  - Cell Abstract View / The Physical Library
  - Std Cell LEF
  - Macro LEF
  - IO LEF
- Technology File
  - Defines Units, Design Rules for Layers and VIAS as per technology
  - Physical and Electrical Parameters
  - Metal direction/pitch/width/offset/thickness/resistance/capacitance etc.
  - Site/Unit Tile definition
- Interconnect Parasitic File
  - Used for layer parasitic extraction
  - Contains layer/via cap and resistance values in lookup table
- Map file
  - Useful if is there is 2 different naming convections in Technology file, LEF or Interconnect Parasitic file

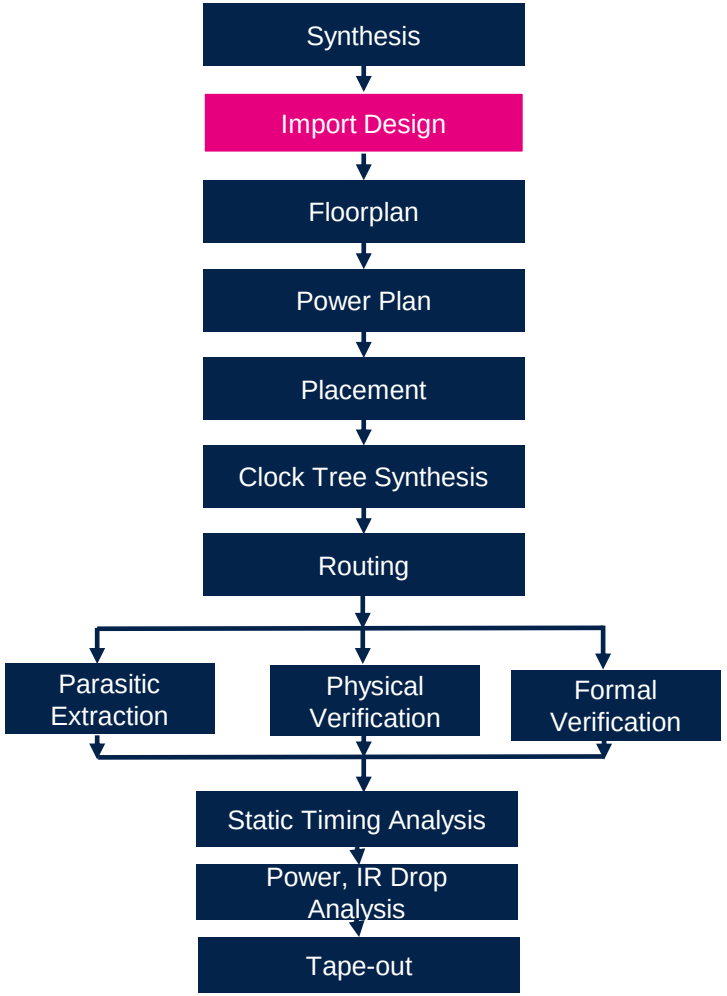
PnR Inputs (2/2)

- Power Specification File
  - Power Modes & Power Domains
  - Tie Up supply & Tie Low supply
  - Power Nets & GND Nets
- Optimization Directives
  - Don’t Use Cells
  - Don’t Touch
  - Size only
- Clock Tree Constraints
  - Root Pin Definition
  - Insertion delay and skew targets
  - Max Cap/Tran limits (DRVs)
  - List of Buffers/Inverters for CTS
  - NDRs for Clock Routes
  - Macro Models if applicable.



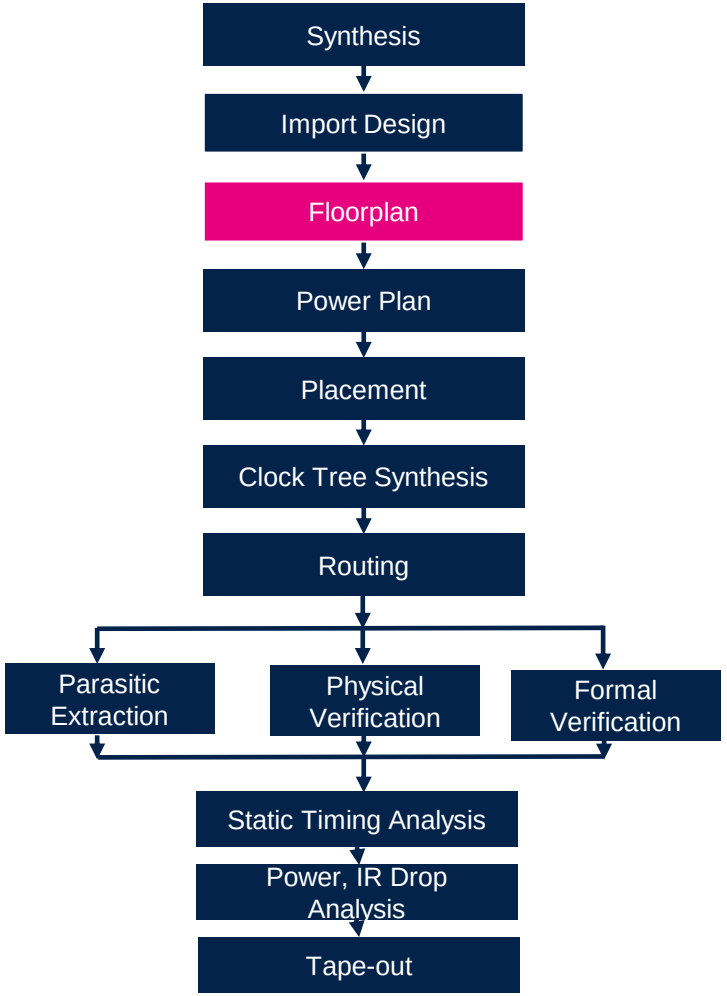
Import Design

- **The following input files information are loaded to the PnR tool**
  - Netlist (.v/ .vhd/ .edif)
  - Physical Libraries (.lef)
  - Timing Libraries (.lib)
  - Technology Files
  - Constraints (.sdc)
  - IO Info. File (optional)
  - Power Spec. File (optional)
  - Optimization Directives (optional)
  - Clock Tree Spec. File (optional at floorplan stage)
  - DEF/ FP (optional if floorplan is not done)
- **Sanity Checks**
  - Sanity Checks mainly checks the quality of netlist in terms of timing
  - It also consists of checking the issues related to Library files, Timing Constraints, IOs and Optimization Directives.
  - Netlist Sanity Checks like floating pins, un-driven i/p ports, unloaded o/p ports multiple drivers etc.



Floorplan

- To achieve best PPA
- To minimize issues like placement density, congestion, timing challenges
- To Reduce wire length and making routing easy.
- To reduce Si cost



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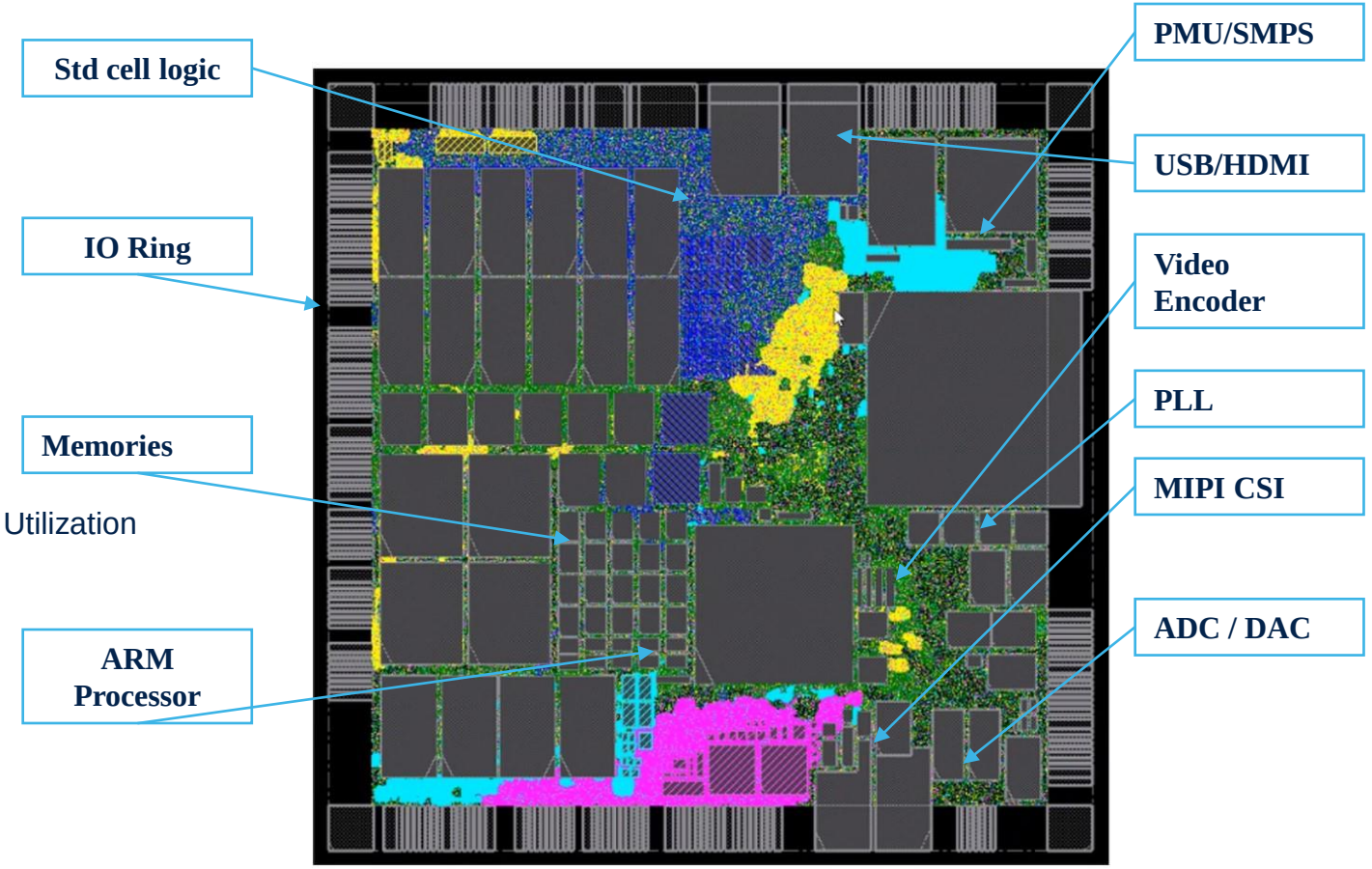
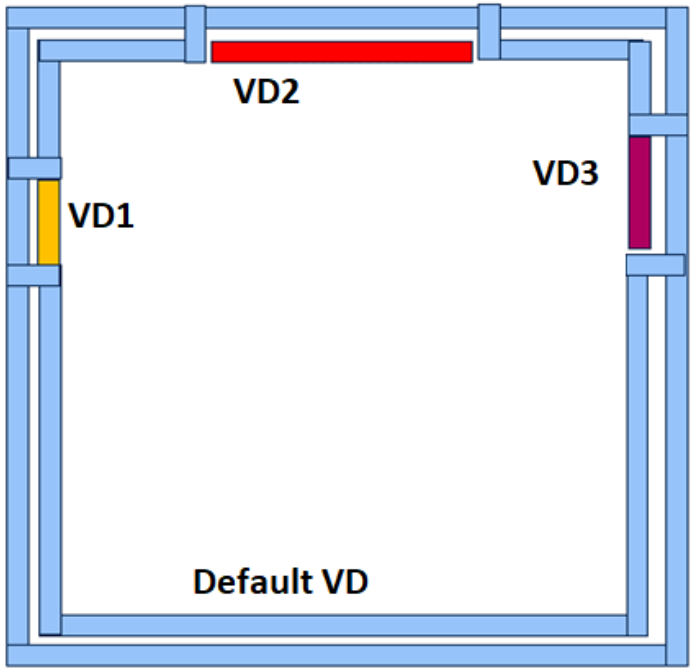
Floorplan

- Important Terminologies in Floorplan
  - Utilization
  - Manufacturing Grid
  - Std Cells Site / Placement Tile / Unit Tile
  - Std Cell Rows
  - Placement Grid
  - Routing Grid and Routing Track
  - Flight-Line / Fly-Line
  - Macros
- Steps in Floorplan
  - Initialize fp with Chip & Core Aspect Ratio (AR) and with Core Utilization
  - Initialize fp Row Configuration & Cell Orientation
  - Provide the Core to Pad/ IO spacing (Core to IO clearance)
  - Pins/ Pads Placement
  - Macro Placement by Fly-line Analysis
  - Blockage Management (Placement/ Routing)



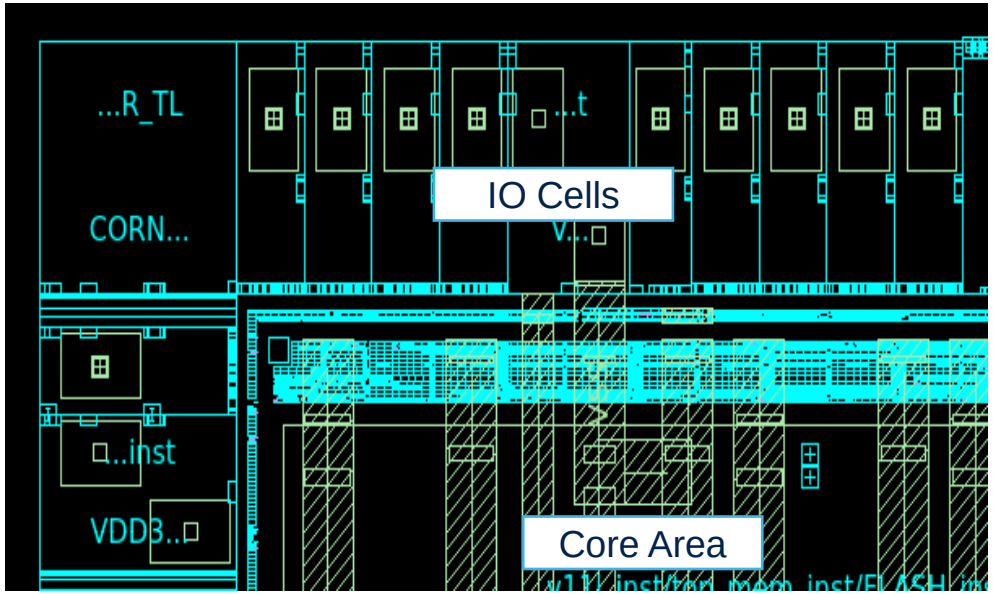
IO-Ring Introduction

- Interface between the package and the chip
- Type of IOs
  - IO and core Power Pads
  - Signal Pads
  - Corner PADs
  - Protection from outside aggression (ESD)
- IOs are abutted to create PAD Ring
- Multi Voltage Design support
- Multi Package Compatibility



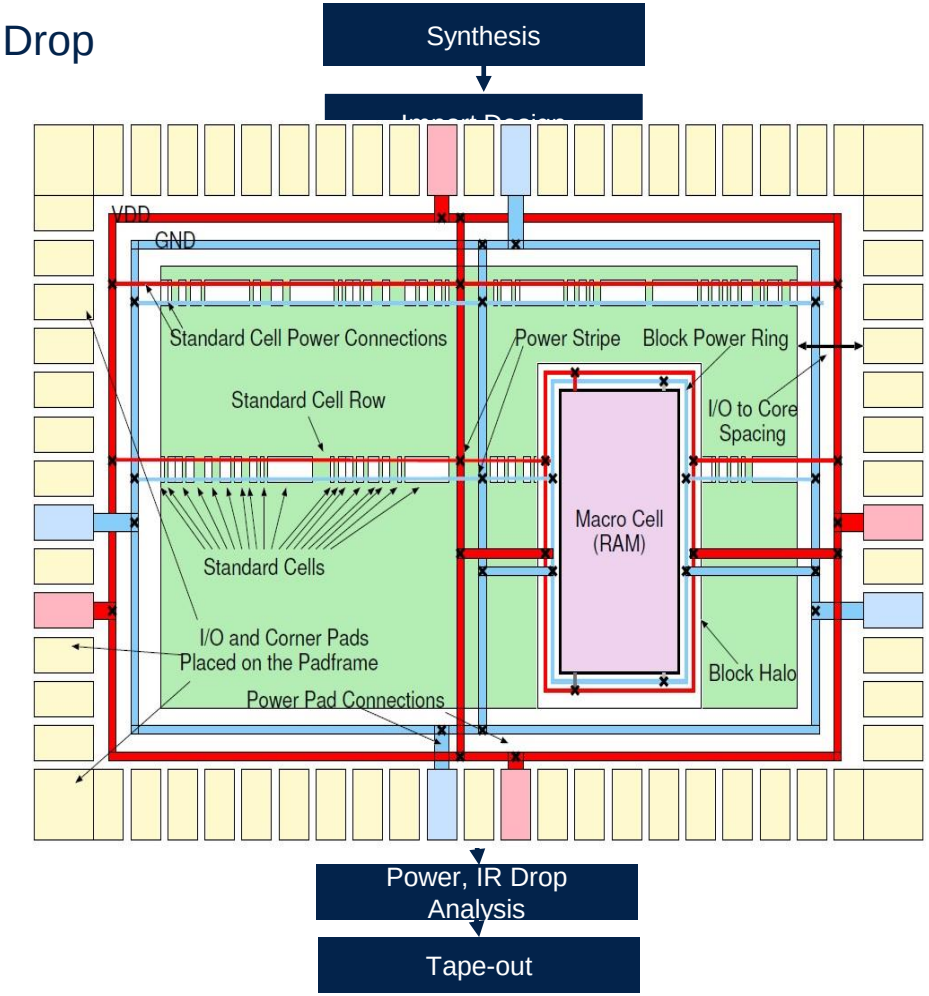
IO-Ring

- **IO Placement**
  - Chip Level => IO Pads and Block Level => IO Pins
  - Pin is a logical entity and is a property of a Port and Port is a physical entity and only 1 Pin associated with it.
  - Netlist will have Pins and Layout will have Ports
  - Different types of IO PADs
    - Signal Pads/Pins
    - Core Power Pads/Pins
    - IO Power Pads/Pins
    - Corner Pads
    - Filler Pads (Fill the gaps between IO pads to get the Ring Connectivity)
  - Physical-only pads that are not part of the input Gate level Netlist need to be inserted prior to reading IO constraints.
  - IO Pads enables the design to operate at different voltages with the help of Level Shifters, Pre-Drivers (at Core Voltage) Post-Drivers (at IO Voltage)



Power Plan

- To connect power to the chip by considering issues like EM and IR Drop
- Levels of Power Distribution
  - Rings : V_{DD} & V_{SS} Rings are created around the core and Macro
  - Stripes: V_{DD} & V_{SS} Power Stripes are created in the core area
- Special Route (Rails)
  - Connect V_{DD} & V_{SS} to the std cells
- Power Vias
  - Insert Visa between ring/grid, and horizontal and vertical grid
- Trunks
  - Connects ring to Power Pad
  - Trunk is a piece of metal that connects IO Pad and Core Ring



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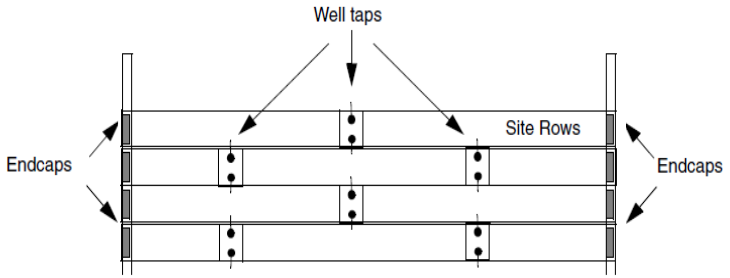
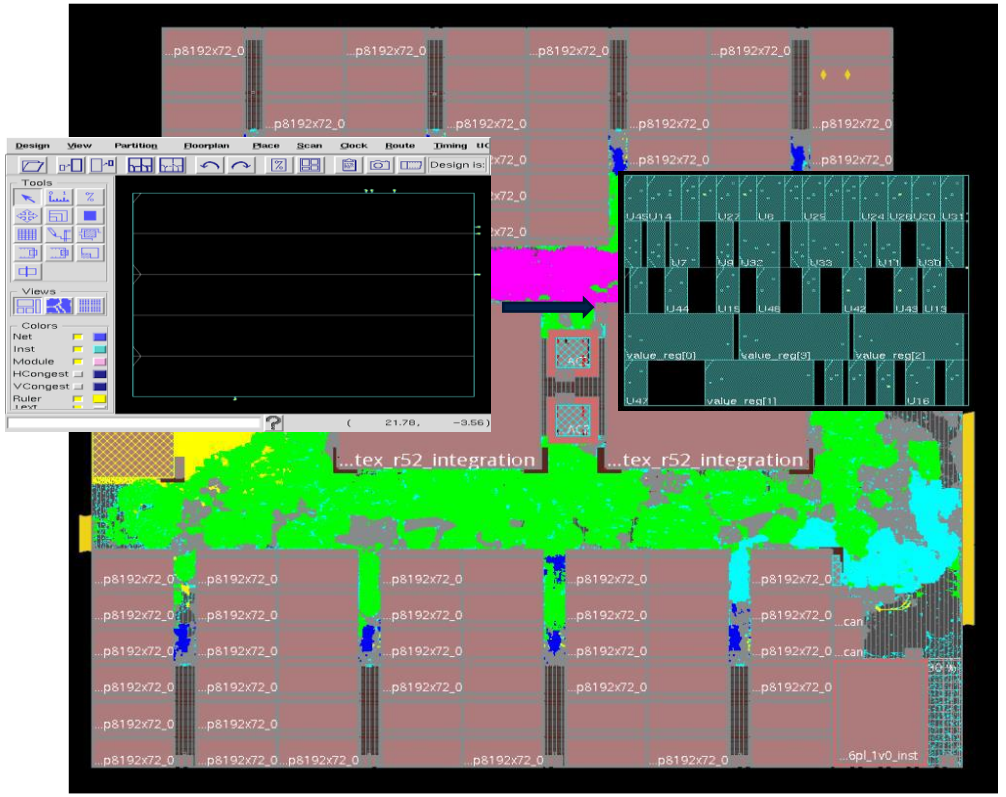
Pre-Placement

- Physical Only Cells (Well Taps, End Caps)
  - These cells do not have signal connectivity and connect only to the power and ground rails
  - End Caps ensure that gaps do not occur between the Well and Implant Layers and prevents DRC violations
  - Well Taps help to tie Substrate and N-wells to VDD and VSS levels and thus prevent Latch-up
- Special Cells (Spare cells, Decap Cells)
  - Spare Cells for ECO and Decaps for avoiding Instantaneous Voltage Drop (IVD)
- Cell Padding
  - Cell Padding is done to reserve space for avoiding Routing Congestion
  - Cell Padding adds Hard Constraints to Placement
  - The Constraints are honored by Cell, Legalization, CTS, and Timing Optimization.



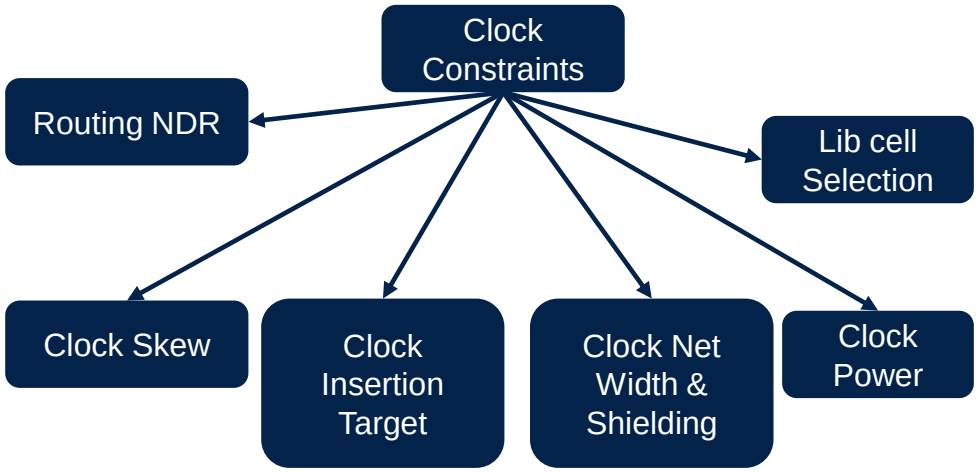
Placement

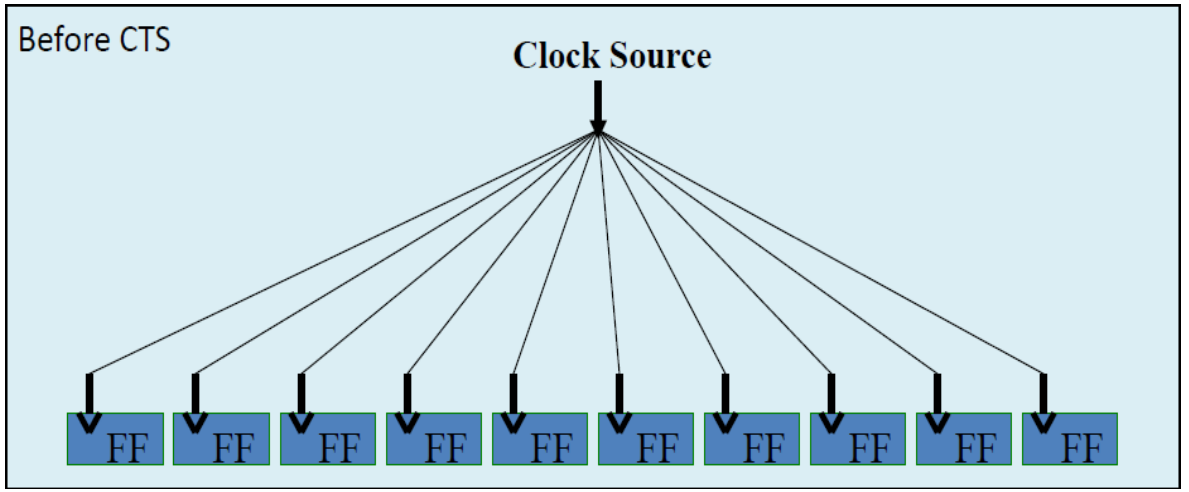
- Automated std cell placement on placement tracks.
- Placement Objectives
  - Total wire length
  - Routability
  - Performance
  - Power
  - Heat distribution
- Timing checks at Placement stage
  - Only Setup Time check, since clock is ideal at placement stage
- Placement Methods
  - Timing Driven Placement
  - Congestion Driven Placement

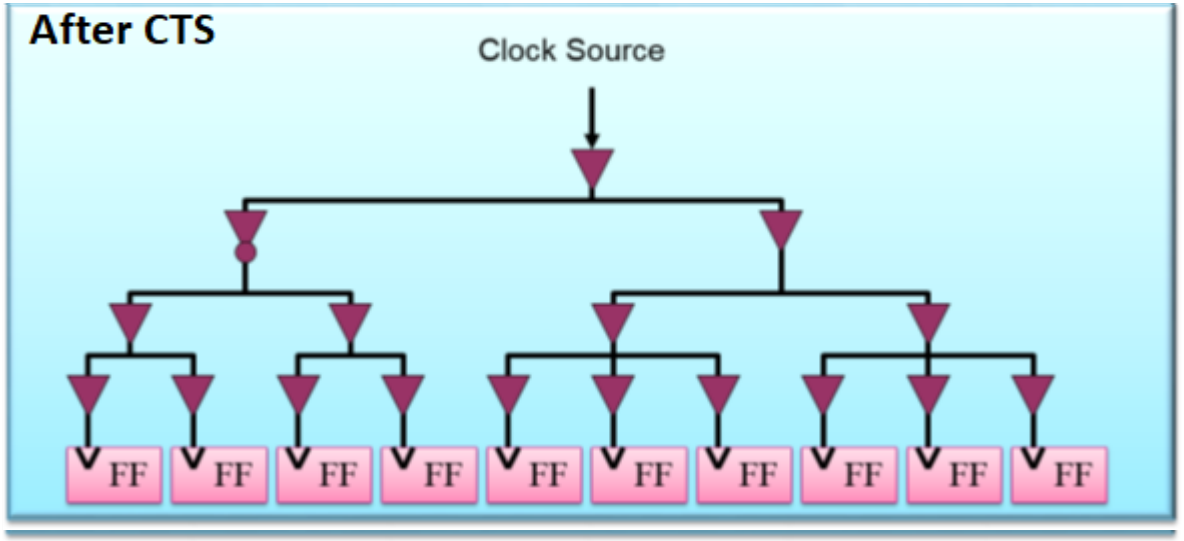


Clock Tree Synthesis (1/3)

- What is clocks Tree ?
- Clock Spec file from SDC
  - Definition of Clocks
  - Clock Balance Constraints
  - Stop & Ignore pins
  - Macro pin insertion delay
  - Exclusive Sink Groups
  - Early Clock for Dividers







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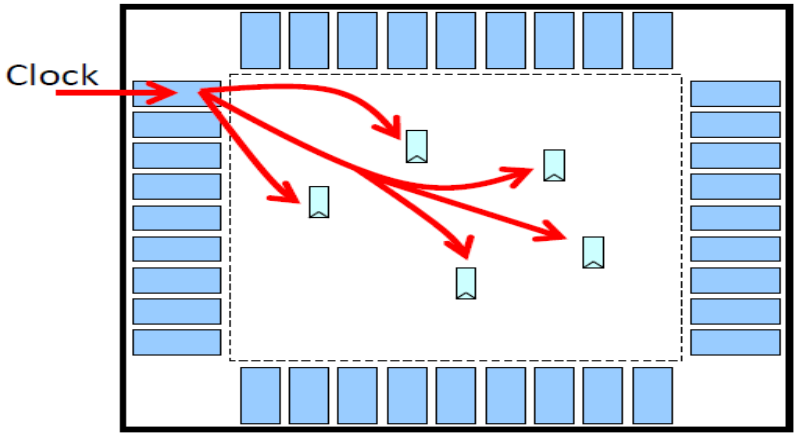
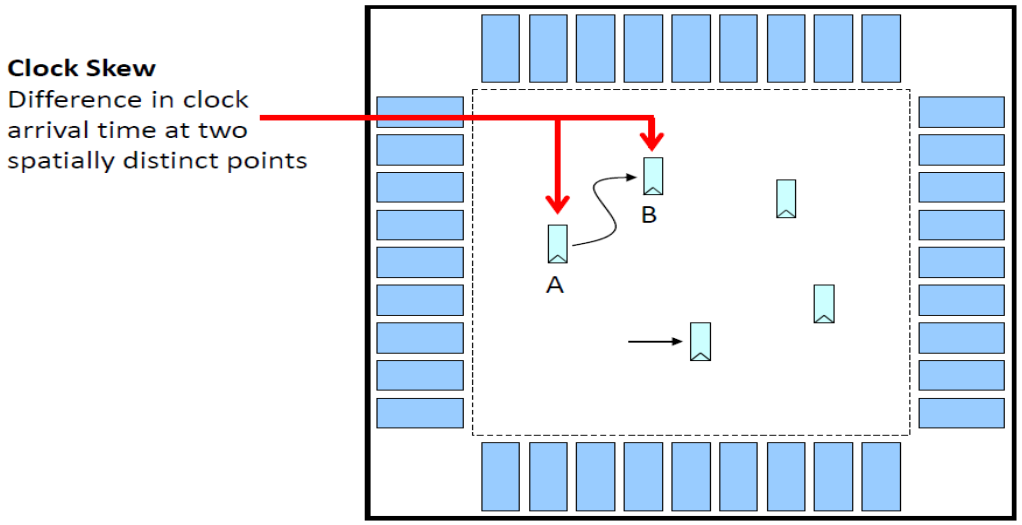
Clock Tree Synthesis (2/3)

- Skew: Most important concern for Clock Networks.
  - Due to variations in trace length, metal width and height, coupling caps.
  - Also due to variations in local clock load, local power supply, local gate length and threshold, local temperature.
- Power: Major power consumer.
  - Clock cell switches at every clock cycle.
- Noise:
  - Clock is often very strong aggressor
  - May need shielding
- Delay:
  - Clock Insertion Delay is important
  - Good transition on clock network.





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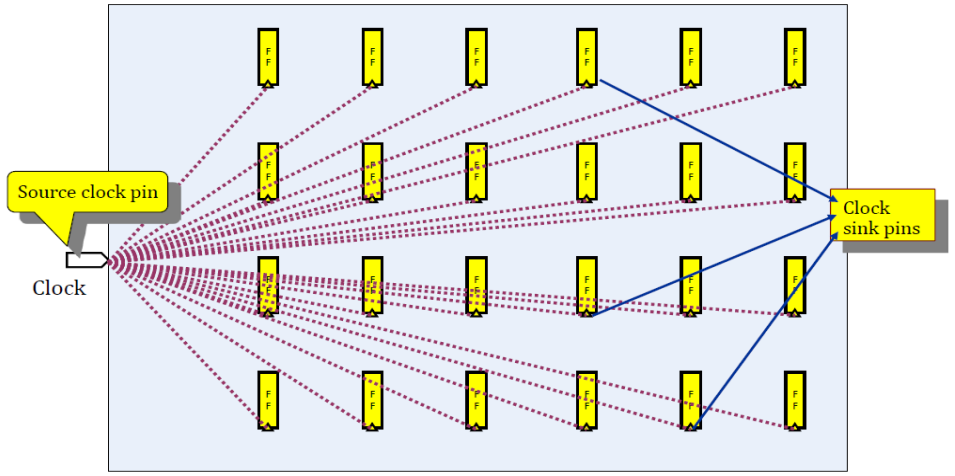
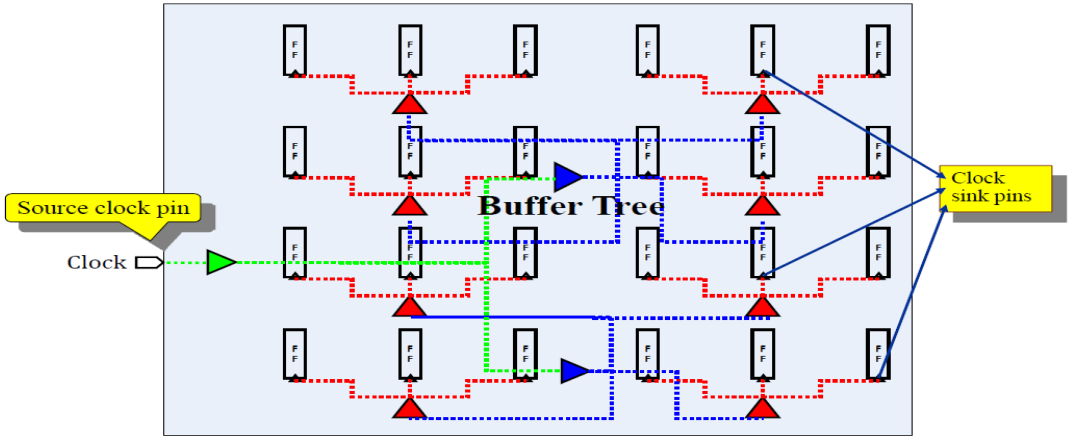
Clock Tree Synthesis (3/3)

- Before CTS, all Clock Pins are driven by a single Clock Source.



- After CTS, the buffer tree is built to balance the loads and minimize the skew.



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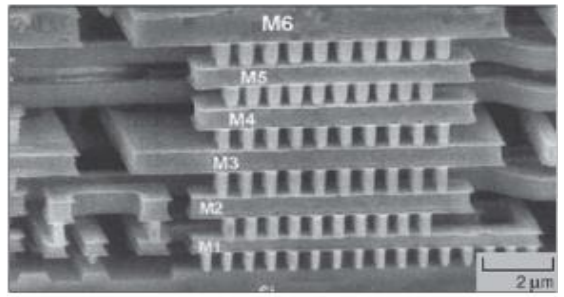
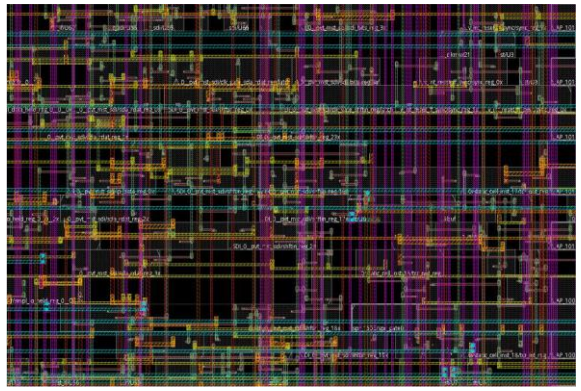
Routing (1/3)

- Routing Objectives : Connections are routed as connected logically
- Routed paths must meet setup & hold timing margin.
- DRVs max. Capacitance/ Transition must be under the limit.
- Metal traces must meet foundry physical DRC requirements.
- Layout geometries should meet Current Density specification.



Multi-level Interconnection (MLI) Technology Layer stacks



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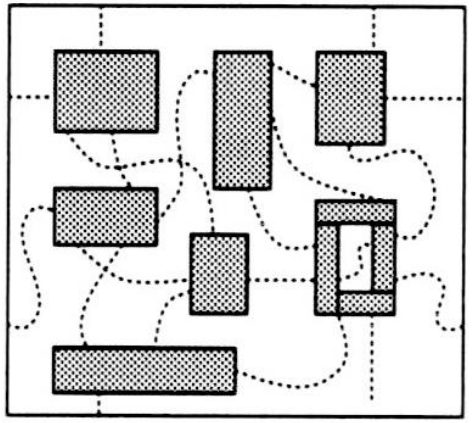
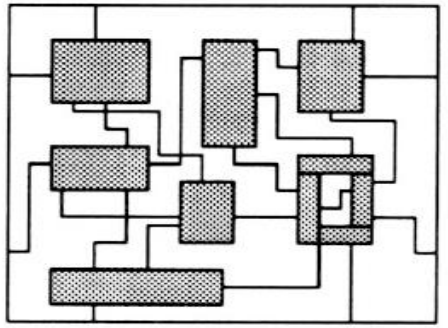
Routing (2/3)

- Trial/Global Routing:
  - Routable path for the nets driving/ driven pins in a shortest distance.
  - Does not consider DRC rules, which gives an overall view of routing and congested nets
  - Assign net to specific routable window, i.e Global Route Cell (GRC)
  - Avoid congested areas and also long detours and avoid routing over blockages
  - Avoid routing for pre-route nets such as Rings/Stripes/Rails
  - Uses Steiner Tree and Maze algorithm
- Track Assignment:
  - Takes the Global Routed Layout and assigns each nets to the specific Tracks and layer geometry
  - It does not follow the physical DRC rules but will do the timing aware Track Assignment.
- Detail/Nano Routing:
  - It follows up with the track routed net segments.
  - It Performs complete DRC aware and timing driven routing
  - Final routing for the design built after the CTS and the timing is freeze.



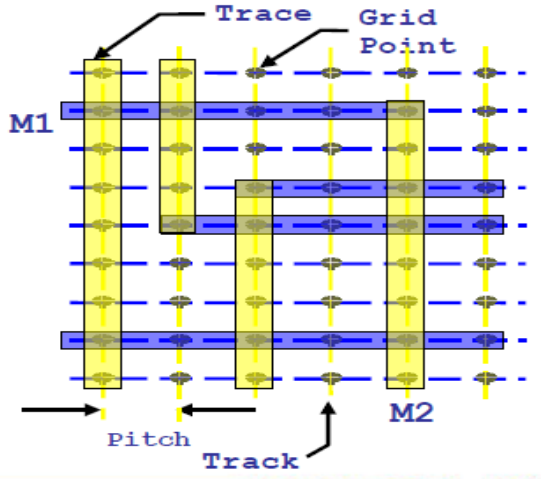
Global Routing

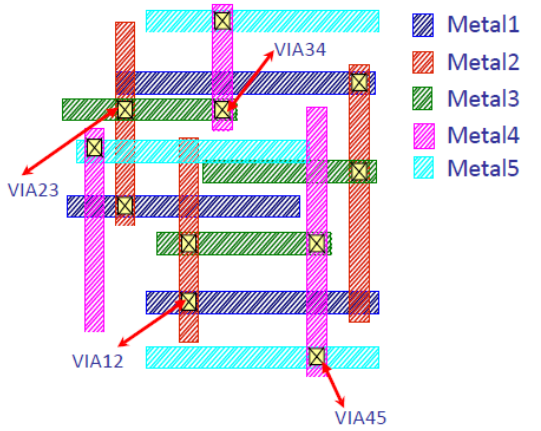


Detailed Routing

Routing (3/3)

- Grid Based Routing:
  - Metal traces (routes) are built along and centered upon routing tracks.
  - Various types of grids are Manufacturing Grid, Routing Grid (Pitch) and Placement Grid.
  - Grid dimension should be multiple of Manufacturing Grid.
- Routing Preferences:
  - Typically Routing only in “Manhattan” N/S E/W directions.
  - Spacing checks with the adjacent layers.
  - Width check for all layers and via dimension rules.
- Layer Routing directions:
  - Each metal layer has its own preferred routing direction and are defined in a technology rule file.
  - M1: Horizontal, M2: Vertical , M3: Horizontal, M4: Vertical and so on…
  - In some cases, we can avoid following preferred routing direction for smart routing (Non-preferred direction)





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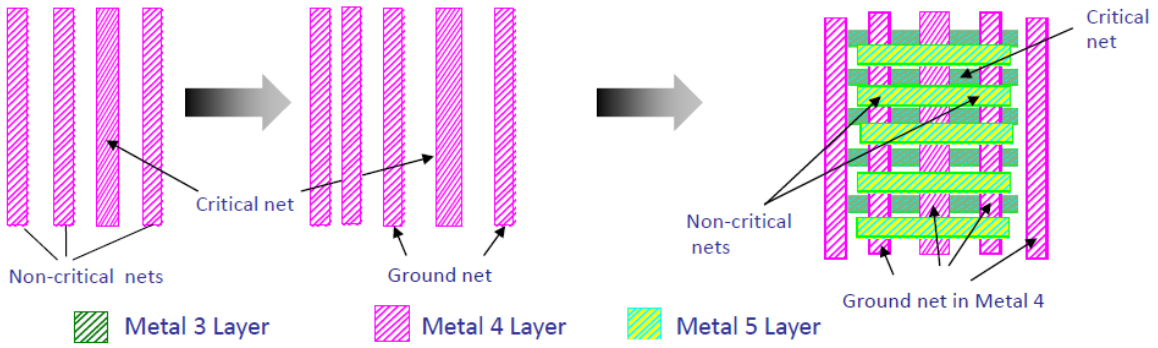
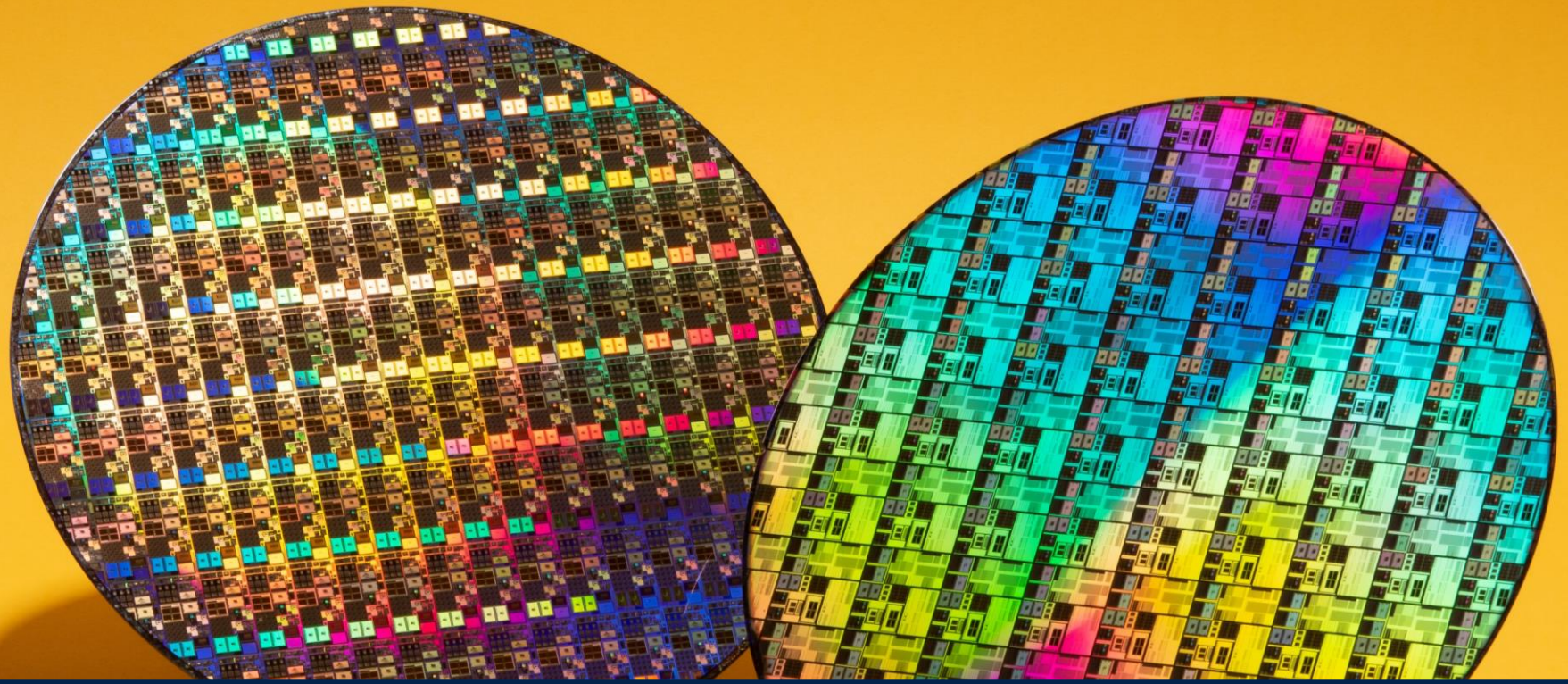
Post Routing Optimization

- Signal Integrity (SI) Optimization by NDRs and Shielding for the sensitive nets
- Types of Shielding for sensitive nets
  - Same layer shielding
  - Adjacent layer/ Coaxial shielding
- Metal Fill: Filling up empty metal tracks.
  - Floating Metal Fills
  - Grounded Metal Fills



Signoff



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Signoff

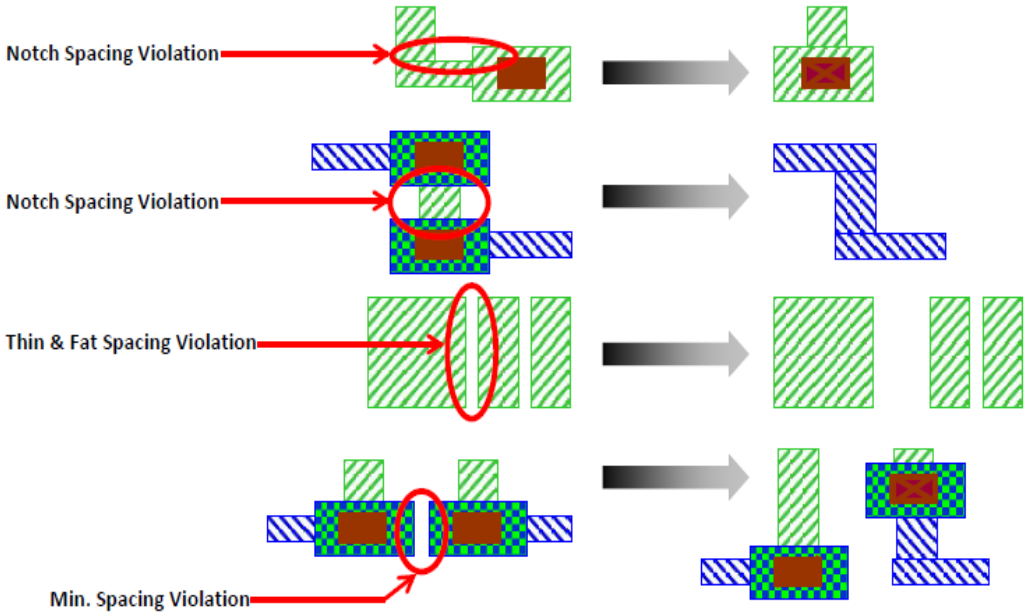
- Physical Verification: DRC and LVS
  - DRC: Fabrication related rules : Spacing and Notch etc
  - LVS: layout versus schematic : GDSII versus CDL.
- Timing Signoff
  - Design meets frequency specs
  - No setup – hold violations
  - All DRVs met (max-capacitance, max-transition, fan-out)
- Power Signoff
  - Static: IR Drop Analysis
  - Dynamic: IR Drop Analysis

Physical Verification (DRC)

- Design Rule Check (DRC) is the process of checking physical layout data against fabrication-specific rules specified by the foundry to ensure successful fabrication.
- Process specific design rules must be followed by drawing layouts to avoid any manufacturing defects during the fabrication of an IC.
- As Technology Shrinks
  - Number of Design Rules are increasing
  - Complexity of Routing Rules is increasing
  - Increasing the number of objects involved
  - More Design Rules depending on Width, Halo, Parallel Length
- Violating a design rule might result in a non-functional circuit or low Yield.

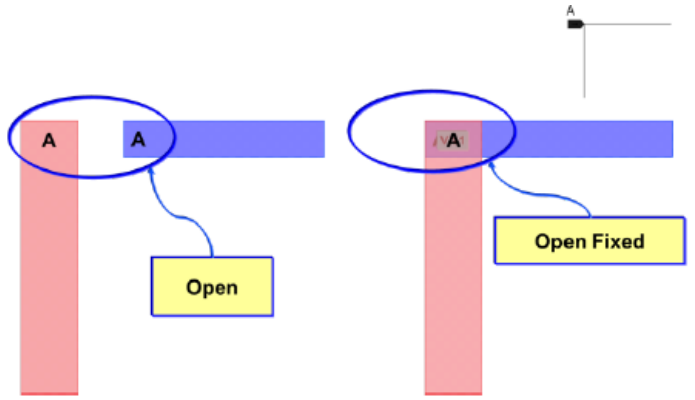
Physical Verification (DRC)

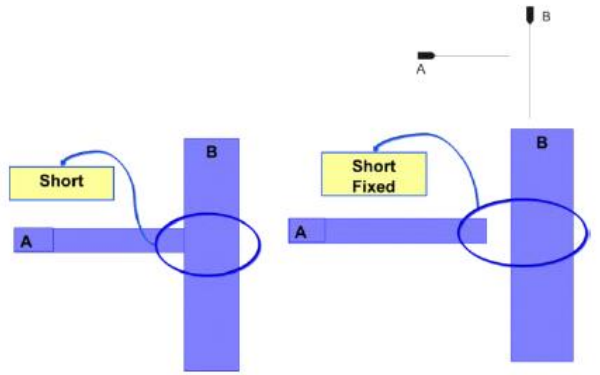
- Design Rule examples:
  - Maximum Rules: Manufacturing of large continuous regions can lead to stress cracks. So ‘wide metal’ must be ‘slotted’ (holes)
  - Grid: All corner points must lie on a minimal grid, otherwise an “off grid error” is produced
  - Minimum Spacing: The minimum spacing between objects on a single layer
  - Minimum Width: The min width rule specifies the minimum width of individual shapes on a single layer
  - Minimum Enclosure/ Overlap: Implies that the second layer is fully enclosed by the first one
  - Notch: The rule specifies the minimum spacing rule for objects on the same net, including defining the minimum notch on a single-layer, merged object
  - Minimum Cut: the minimum number of cuts a via must have when it is on a wide wire



Physical Verification (LVS)

- Layout Versus Schematic (LVS) verifies the connectivity of a Verilog Netlist and Layout Netlist (Extracted Netlist from GDS)
- Tool extracts circuit devices and interconnects from the layout and saved as Layout Netlist (SPICE format)
- As LVS performs comparison between 2 Netlist, it does not compare the functionalities of both the Netlist
- Input Requirements
  - LVS Rule deck
  - Verilog Netlist
  - Physical layout database (GDS)
  - Spice Netlist (Extracted by the tool from GDS)
- LVS checks examples
  - Short Net Error, Open Net Error, Extract errors, Compare errors





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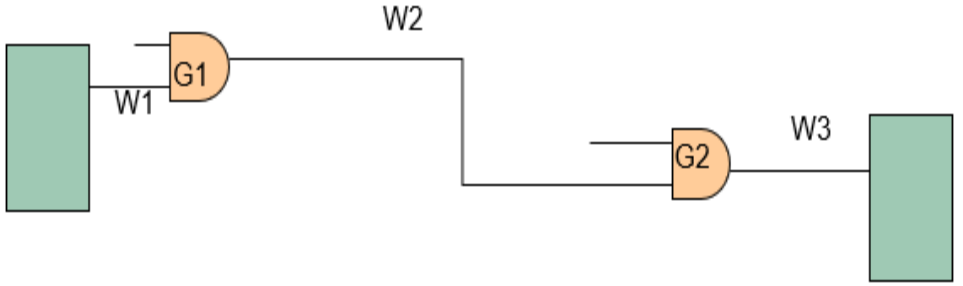
Timing Signoff

- To check if the design meets timing constraints in all situations.
- Static Timing Analysis : Computes both minimum and well as maximum range of delay values of all possible combination of inputs
- First stage STA done at gate level netlist.
- Where does timing come from ?
  - Gates: PVT (operating conditions)
  - Connections: (load Cap, and input tran).
  - Wire: parasitic (resistance, Capacitance)

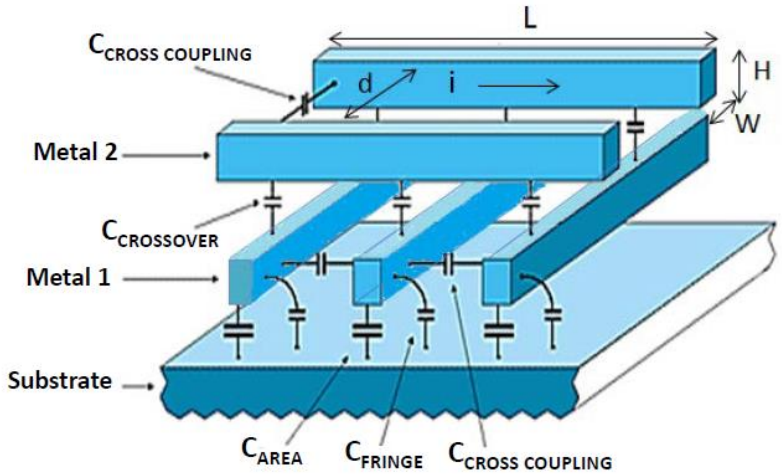
- STA: Principle…
  - To time any and every single gate & wire
  - Sum up these delays on any timing path
  - Check versus the constraints if timing is met

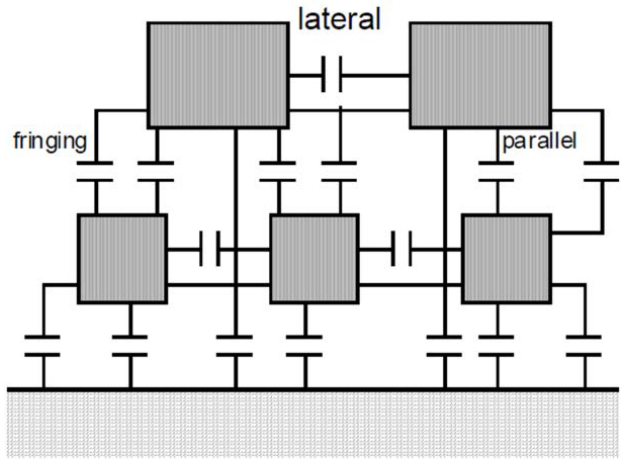


Delay in Gates (G1, G2) + Delay in wires (W1, W2, W3) < Expected delay on the path

Parasitic Extraction

- Capacitance : C = εo*W*H / d
  - Transistors: Depends on area of transistor gate, physical of materials, thickness of insulator, diffusion to substrate
  - Poly to Substrate: Parallel plate and fringing.
- Capacitance between conductors: Coupling cap, Area cap, Fringing cap and Crossover cap.
- Coupling Cap / Lateral Cap
- Fringing Cap
- Parallel/Crossover Cap
- Area Cap





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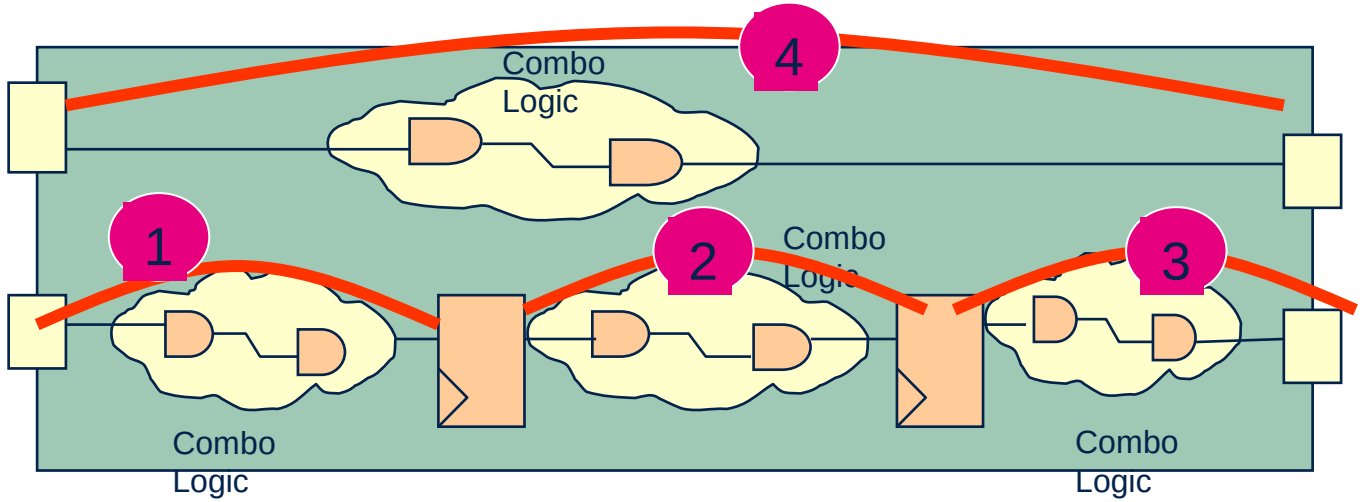
Static Timing Analysis

- Default #4 types of timing paths:
  - In2Reg
  - Reg2Out
  - Reg2Reg
  - In2Out
- Setup and Hold check
- Max Transition and Max Capacitance check



1 Input to Register Paths

2 Register to Register Paths

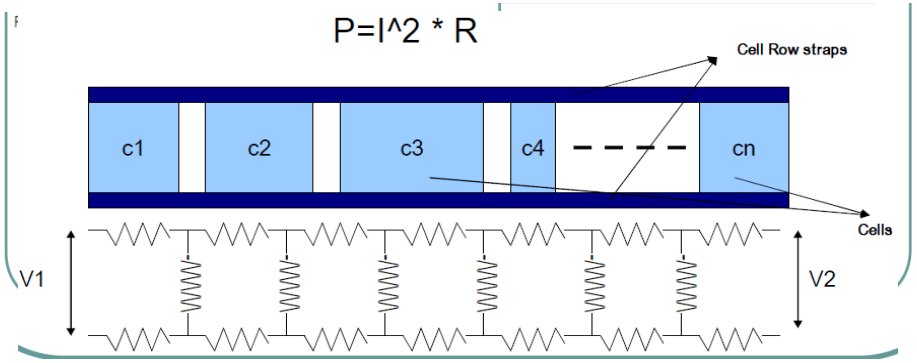
3 Register to Output Paths

4 Input To Output Paths

IR Drop Analysis

- Why worry about IR drop analysis ?
  - Poor-floor planning
  - Problems in power routing such as: Unconnected contact arrays, Power grid discontinuities.
  - Insufficient power pins
  - Incorrect power-pin placement
  - Faster clocks => higher power consumption, need to offset by scaling C and Vdd
  - Shrinking wire cross-sections => higher wire and via resistances values
- Power dissipation on the silicon will happen because of following reasons.
  - Static components
  - Dynamic components
  - Power distributions

- Static Components
  - Subthreshold Leakage
  - Tunneling Current
  - Reverse Biased diode leakage
- Dynamic Components
  - Switching and Short circuit analysis
  - Charging and discharging of the load capacitances.
  - Short circuit current through PMOS and NMOS transistors when they are partially on.
- Power Distribution : Ohm’s law applicable



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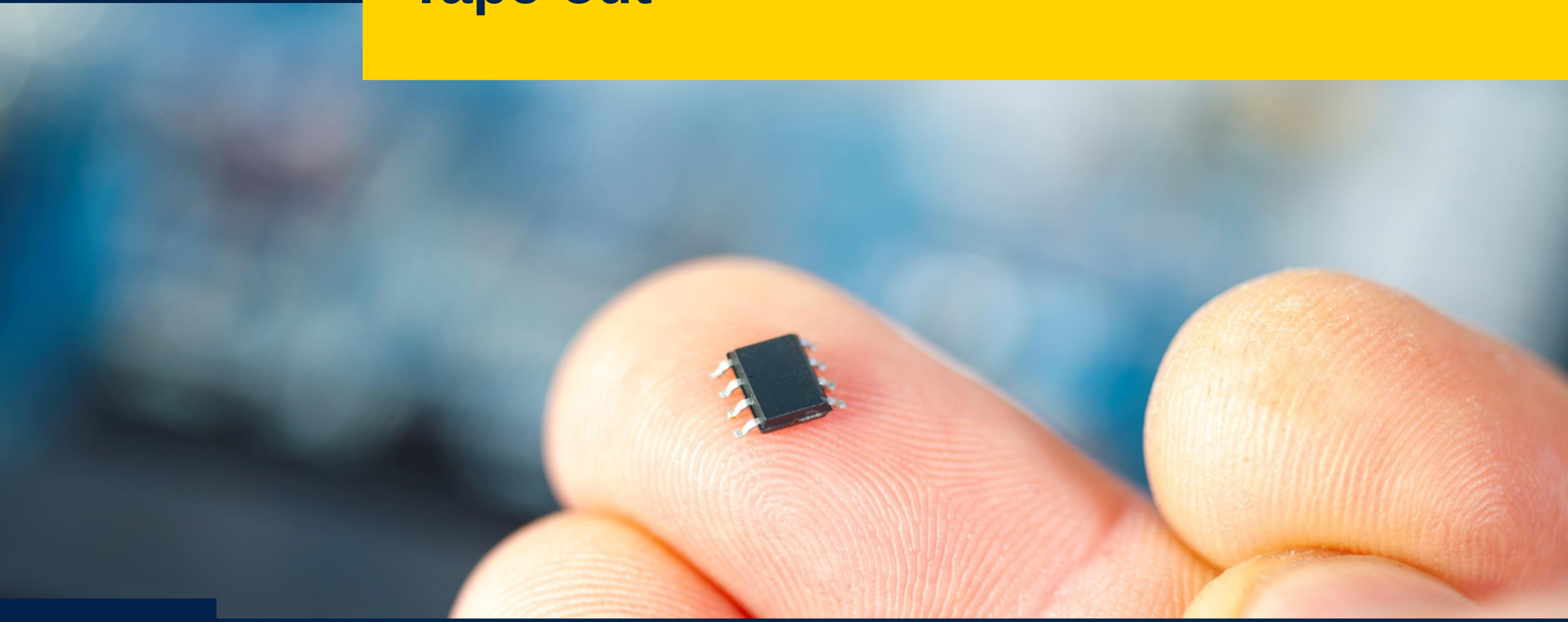
Tape-out



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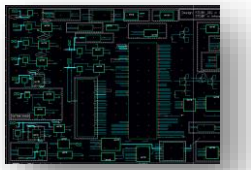
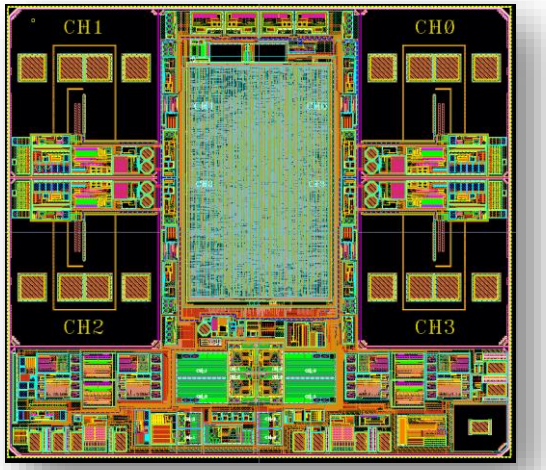
Tape-out

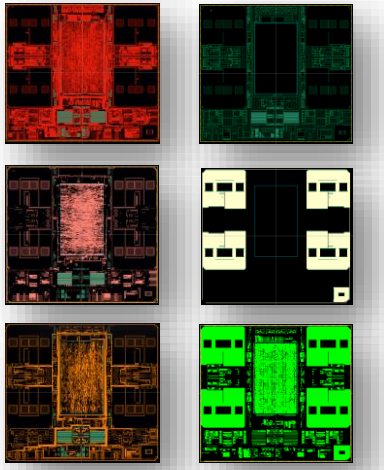
- Chip is ready to be manufactured ☺



SCHEMATIC

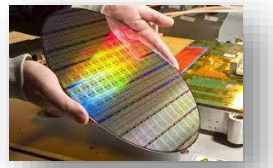


LAYOUT



MASK LAYERS

PHOTOLITHOGRAPHY MASK



CHIP ON WAFER

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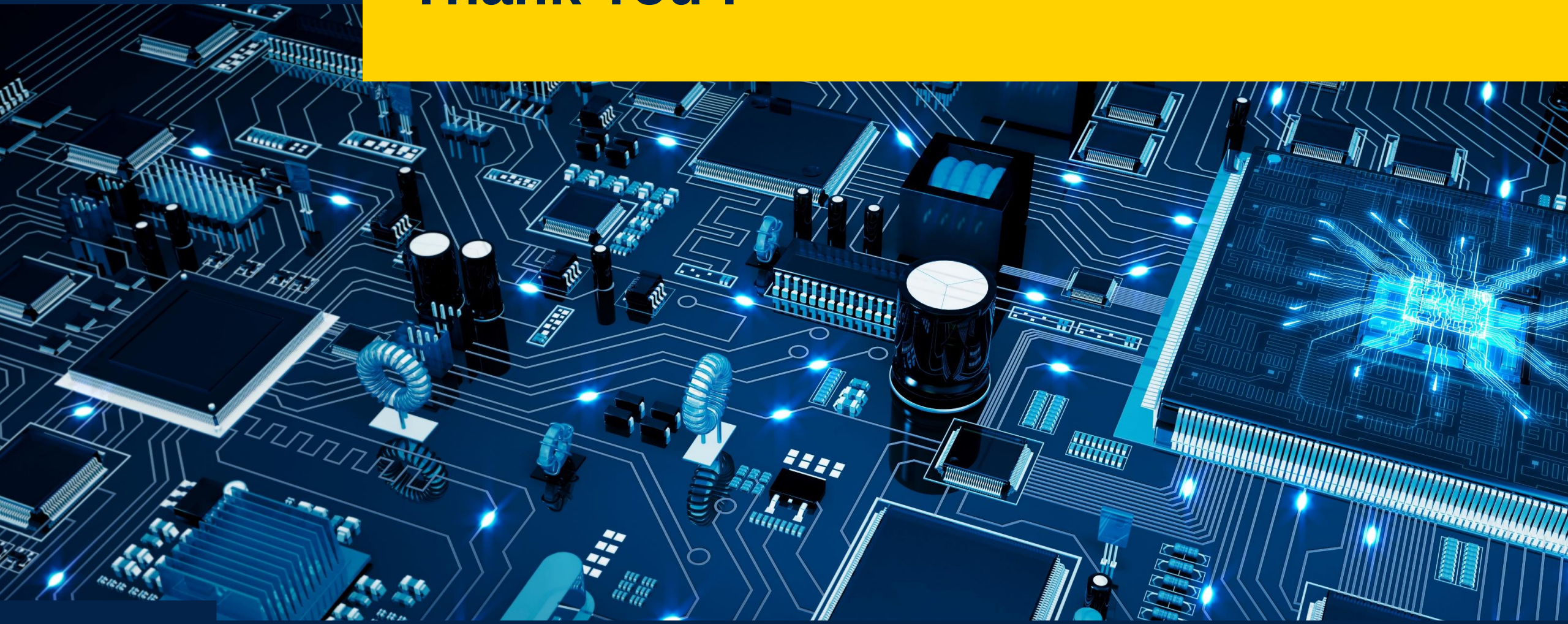
Thank You !



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