VLSI Introduction: Idea to product flow

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Presenters

- **Mukesh Chopra** – Director, Microcontroller & Discrete ICs Group (MDG) R&D India STMicroelectronics
- With 20+ years in semiconductor industry (VLSI & Software), Mukesh has strong Leadership acumen having a rich experience across SOC development cycle including SOC design & verification, Subsystem/IP development, System level design, Design methodology & Foundation library development.
- He has contributed to products ranging from 0.18um to 5nm technologies in consumer, automotive, industrial & storage domains. In addition, he has actively participated in International Standardizing bodies.
- Led several cross-functional and global task forces, driven EDA partnerships to solve complex organizational and technical challenges.

- **Ashish Kumar Sharma** – IP Sourcing – MDG GPM IDC, STMicroelectronics
- Ashish is managing IP Sourcing for General Purpose Micro (GPM) products in ST, Greater Noida. With 22+ years of experience, he has experience doing things in verification, design, architecture domain from scratch.
- Has deep expertise in architecture definition, planning, execution, resource management, risk mitigation, strategy loop development and deployment, cross functional working with various stakeholders, customer interaction, managing teams across different sites.
- A recognized leader is a pro on cross vertical coherence, diversity, collaborative leadership and deploying processes to attain reliability-repeatability-consistency and sustainability.

Agenda

1 VLSI Industry Overview

2 Building Blocks

3 Beyond Moor’s

4 Let's see product design flow

5 How to be part of semiconductor industry

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VLSI Industry overview

Semiconductors industry is an industry built on sand

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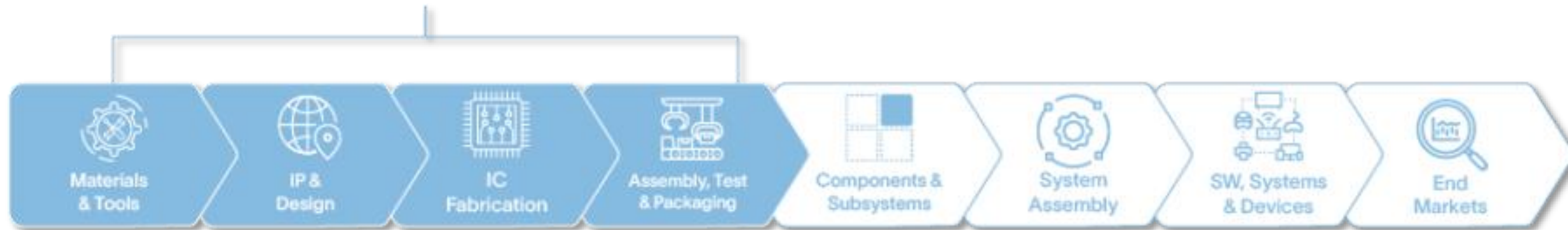
Semiconductor Ecosystem



Materials
Showa Denko, UCT, BASF

Capital Equipment
ASML, Applied Materials, Lam Research, KLA, TEL

EDA Tools
cadence, Ansys, KEYSIGHT TECHNOLOGIES, SYNOPSYS, XILINX

Integrated Device Manufacturer (IDM)
ANALOG DEVICES, intel, SK hynix, MICROCHIP, ON Semiconductor, TOSHIBA, maxim integrated, qorvo, FUJITSU, freescale, CYPRESS, MITSUBISHI, infineon, ST, TI, IBM, NXP, Micron

Sensors/ Passives
AVX, BOSCH, KEMET, Panasonic, VISHAY

Fabless
Qualcomm, BROADCOM, AMD, NVIDIA, MARVELL

Core IP
arm, FARADAY, LATTICE, Rambus

Foundry
intel, Micron, SAMSUNG, tsmc

OSAT/ATMP
ASE Technology Holding Co., Ltd., JCET, Amkor, Powertech Technology Inc.

PCB
AT&S, COMPEQ, ELTEK, flex, Mektec, SMTC, Unimicron 欣興電子

OEMs
Canon, NOKIA, Motorola, LG, Apple, Juniper, cisco, SEAGATE, SAMSUNG, ASUS, DELL, HITACHI

EMS
Benchmark, FOXCONN, SANMINA, wistron, JABIL, Inventec

SW
aws, Linux

CoSPs
AT&T, BT, CenturyLink, Charter, COMCAST, T, verizon

CSPs
aws, Azure

Healthcare
GE, SIEMENS, PHILIPS

Automotive
Ford, BMW, HONDA, VW

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Semiconductor and *Geopolitics*

FORBES > INNOVATION > AI

The Geopolitics Of AI Chips Wil[l] Define The Future Of AI

Tech Today Congress: India needs to build an in-house semiconductor supply chain, says panel

Various aspects of India's semiconductor ... n were extensively deliberated upon during the panel discussion on 'The World on a Chip' at today's Tech Today C... zed by Business Today in Bengaluru.

INTERVIEW

Why semiconductors are central to world economy, geopolitics

Geopolitics Distorting Chip Market, Locating Fabs Locally No Guarantee[e] Competitive Edge: TMSC CEO On 'D[e-]Taiwanification' Of Semiconductor Industry

Analysis

From chip shortages to global chess: Geopolitical struggles are reshaping the [se]miconductor industry

Japan revamps semiconductor strategy as competition and geopolitical tensions heightens

Technology

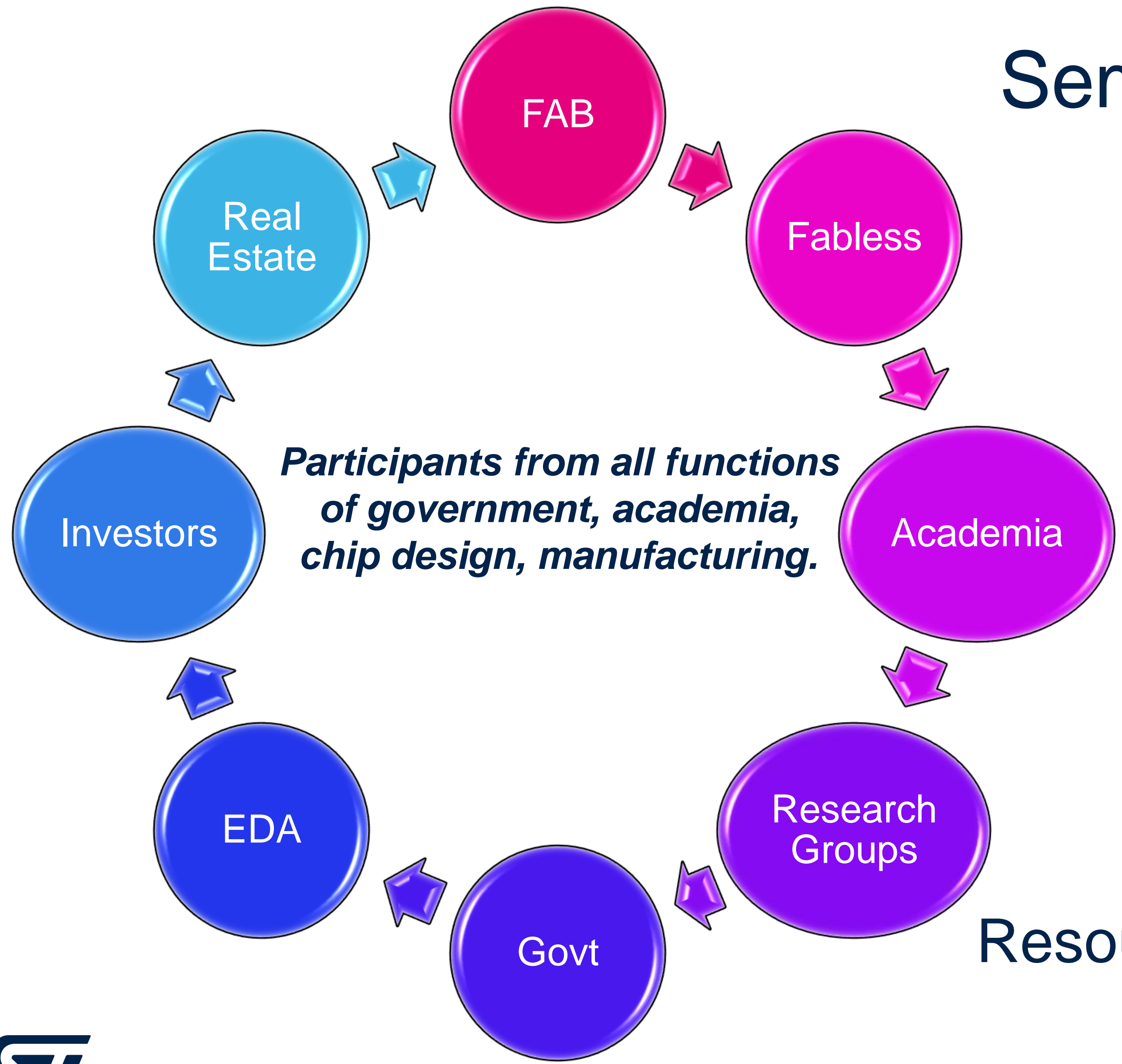
Buffett says geopolitics a factor in Berkshire sale of TSMC stake

Reuters

Global politics to be dominated by semiconductor supply chain, says Intel boss

Chiplet Innovation Will Extend Moore's Law & Emerge As Crucial Component In US-China Tech Dominance Rivalry

Semiconductor Ecosystem



SemiconIndia 2023
Catalyzing India's Semiconductor Ecosystem
Gandhinagar, Gujarat | July 28 - July 30

Chip act !!

Resources (water, energy, material)

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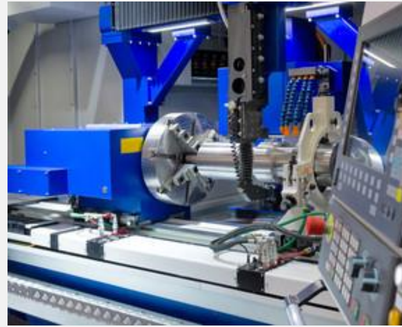
Applications

Appliances

Metering

Robotics & Automation



Healthcare

Power Tools

Secure Locks

Surveillance

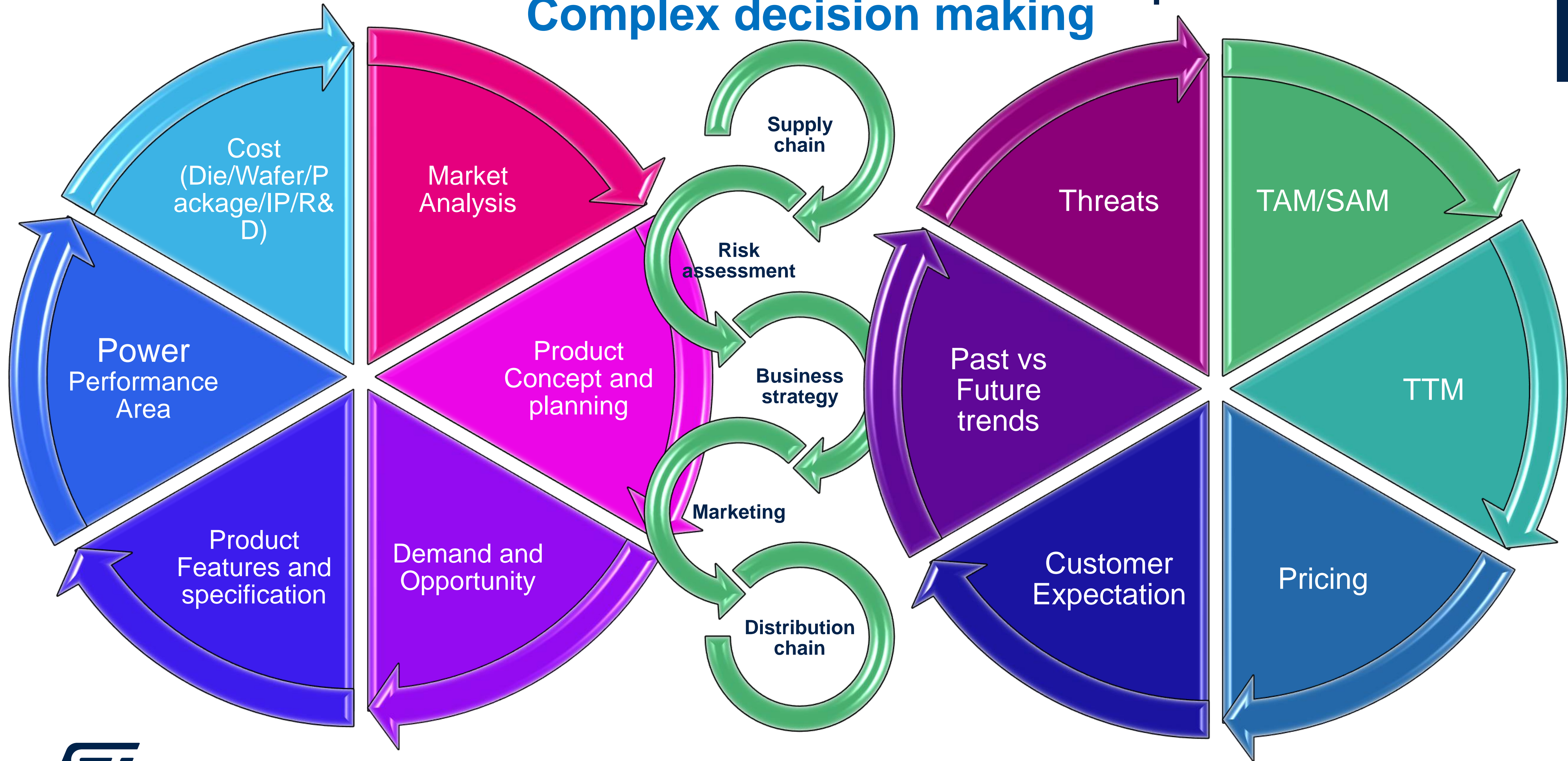
Smart Homes & Buildings

Drives, Pumps, Compressors

Lighting

How a product is built

Complex decision making



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Product Type

Digital

- Detect the presence (1) or absence (0) of a voltage
- Boolean Logic
- Manipulated and processed
- Real world signal get converted to Digital by quantization

Mixed Signal

- Complex design
- Have benefits of both analog and digital processing

Analog

- Deals with voltages, frequency, current, or charge
- Measure, process, manipulate
- Well suited to processing real-world signals
- Theoretically infinite resolution

Building Blocks

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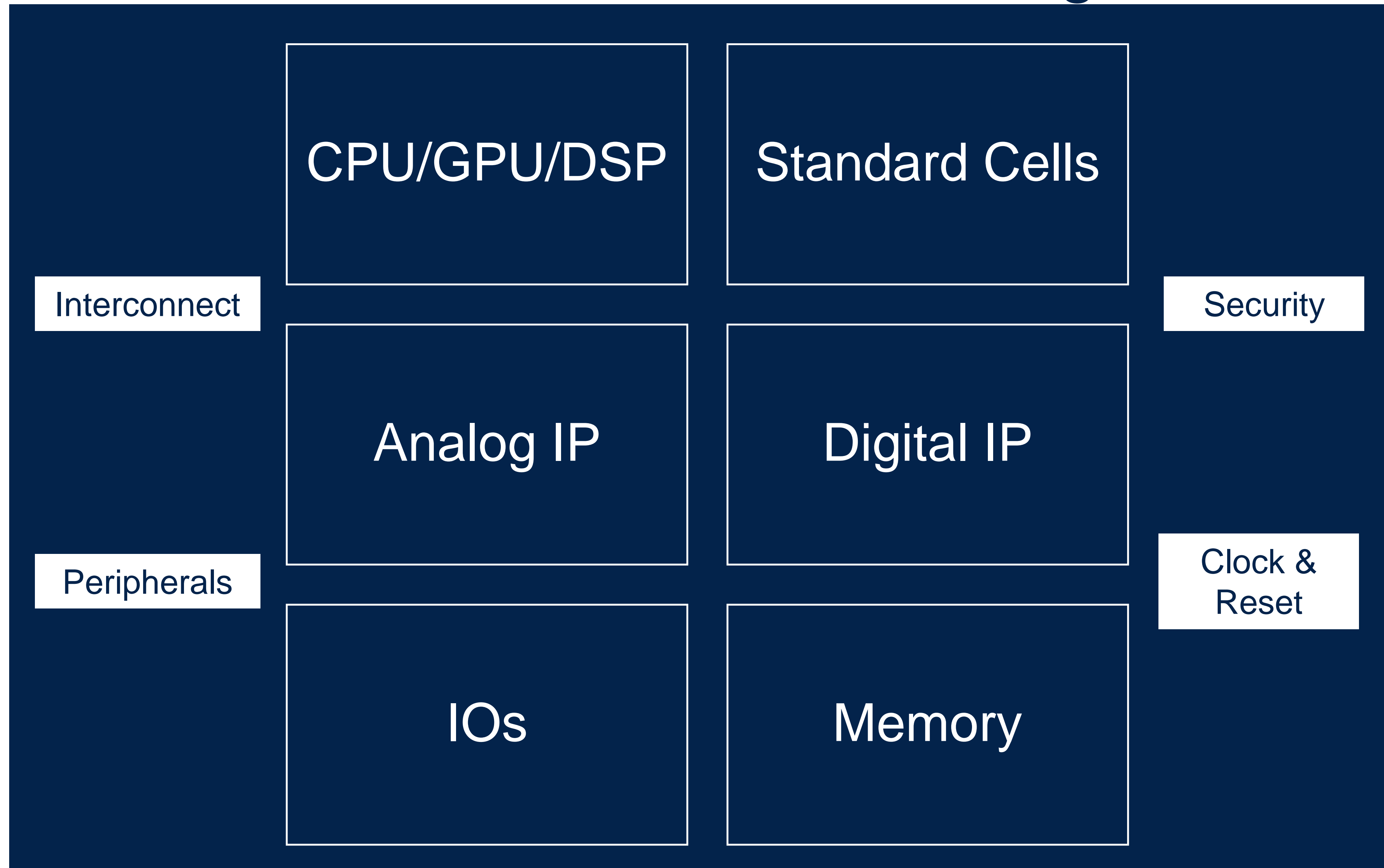
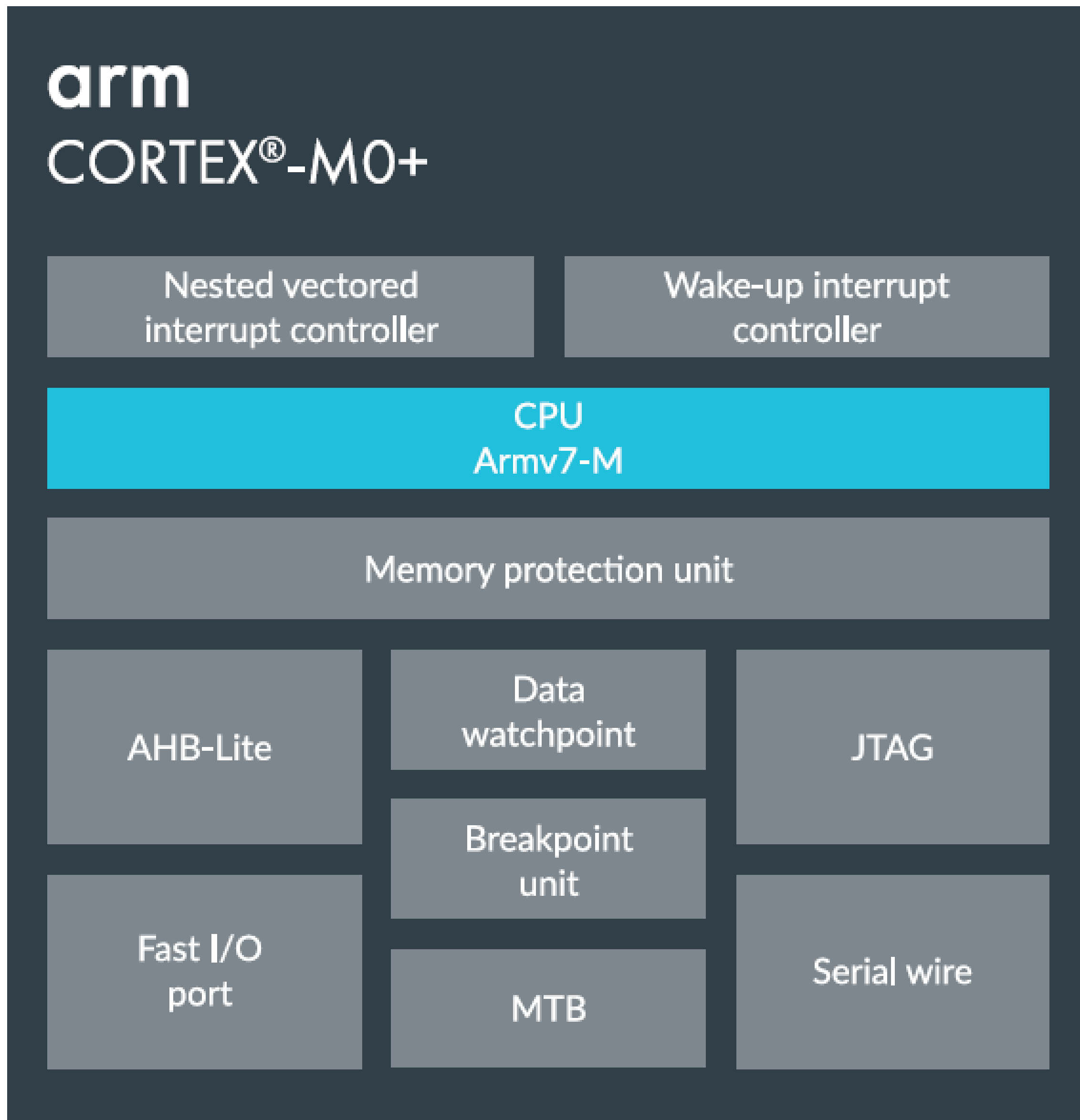
Building blocks of SOC



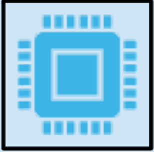


Processor

- Three-stage pipeline based on a von Neumann bus architecture
- Privilege-level separation
- Memory protection unit
- Small and inexpensive processor
- MTB: Micro Trace Buffer, its low-cost instruction-trace feature
- Optional single-cycle I/O interface for connecting peripherals that need low-latency access
- 32 bit instructions

Content courtesy: Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers

Choice between MPU/MCU



Microcontroller uses on-chip embedded memory (FLASH, PCM, MRAM, ReRAM etc.), to store and execute its program.

Fast but size constraint

Microprocessor uses external memory for program and data storage

Large storage comes at cost

Deciding factors

Real time application

Power consumption

BOM cost

Processing power required

Microprocessor vs Microcontroller

Processor frequency/performance/capabilities	*****	***
Rich open operating system support	*****	*
Security support flexibility	*****	***
External memory size/performance	*****	**
External mass storage support	*****	***
Peripheral set	*****	*****
Real time predictibility	*	*****
Boot time	***	*****
Wakeup time	*	*****
System power consumption	***	*****
Overall ease of system conception and bring up	**	*****

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IP: Integrated circuit Intellectual Property, also known as IP block or IP core

- These are *reusable block of logic*
  - Pre-designed and Pre-verified functional blocks
  - *IP can be Generic or Fixed*
    - *Parameterized* to cater wider use cases (flexible design, may not be area optimized) also known as generic IP. CAN, Ethernet, I2C, MIPI, USB, Memory controller etc.
    - *Fixed functionality* (area optimized, context specific), SOC specific IPs like Reset and Clock control, power controller

- ***Digital***: Standard interface for configuring its register. Ex CAN, ETHERNET, GPU, CPU.
- **Analog**: crucial for handling real-world signals. (ADC, DAC, SMPS, LDO, Current Mirror, Comparators, OPAMPS)

- ***Soft***: Technology agnostic, synthesizable, delivered in RTL form (sometimes netlist, encrypted), provides flexibility and portability.
- ***Hard***: Technology specific, optimized area, optimized timing, usually delivered as a layout database (GDSII) or as a physical design database
- ***Hybrid***: combination of hard and soft

- IP helps in
  - Time and Cost *Savings*, *Reusability*, *Quality* and *Reliability*, Focus on Core Competencies

Standard Cells

- Standard cells are pre-designed and pre-characterized building blocks that can be reused to implement different logic functions. They have fixed sizes, shapes, and layouts, and are stored in libraries that can be accessed by automated tools.

- Combinational logic
  - Basic Gates: INV, BUFF, NAND, NOR, AND, OR, EXOR
  - Multiplexer: MUX, MUX-INV
  - Compound Boolean: AND-OR-INV
  - Arithmetic Operation: Full Adder, Half Adder
- Sequential logic
  - Flipflops
  - Latches

- PPA (Power Performance Area)
  - Track: 6T, 8T, 9T, 12T, 18T (Speed vs Density)
  - Vt: Low Vt, Standard Vt, High Vt (Timing vs Power)
    - Channel doping: LVT → SVT → HVT
    - O/P drive current: HVT → SVT → LVT
    - Cell Delay: HVT → SVT → LVT
    - Cell Leakage: HVT → SVT → LVT

- Library Views: layout, schematic, symbol, abstract, simulation, spice model, hdl

Memory

Memory: It's a storage entity used to store data

- Uses ***electrical***, ***magnetic***, ***optical***, *quantum* properties to store data in form of bits.
- Various parameter decide its selection: *speed-access time*, *storage capacity*, *power consumption*, *volatility*, *endurance*, *cost per bit*, *reliability*, *temp and environment condition*, *technology compatibility*, *design constraints*.

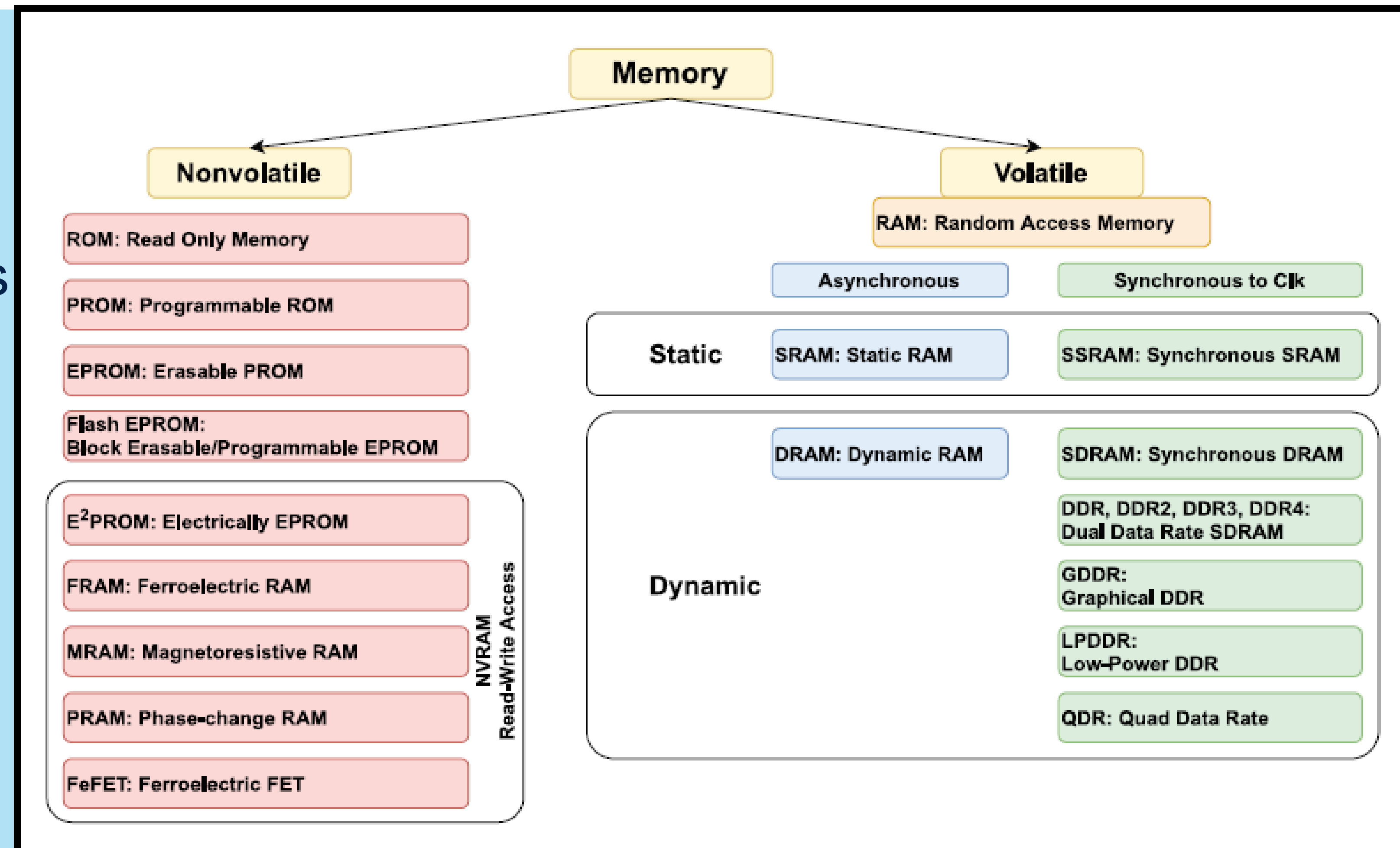


Image courtesy: Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers

IO, Bumps, Package

IO

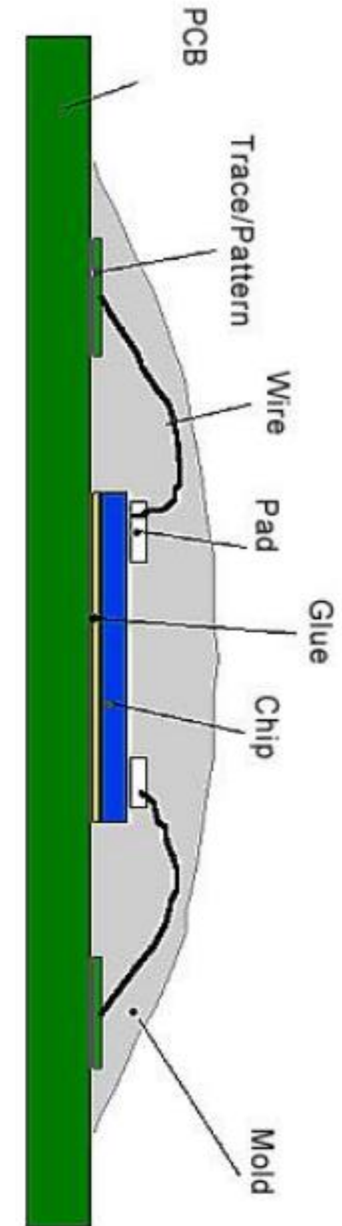
- IO refers to the interface or communication between the integrated circuit (IC) and the external world.
- IO pads or cells are located on the periphery of the IC and serve as physical connections between chip and external world. Drive large capacitance off chip
- Operate at compatible voltage levels. Provide adequate bandwidth
- Limit slew rates to control di/dt noise. Protect chip against electrostatic discharge.
- Types of IO can be Vdd/Gnd, Output, Input, Bidirectional, Analog

BUMPS

- Bumps, also known as solder bumps or micro-bumps, are small metallic connections placed on the surface of the IO pads of the chip.
- These bumps are typically made of materials like solder or copper.
- Their primary purpose is to facilitate the electrical and mechanical connection between the chip and the package.

Package

- The package, also called the semiconductor package, is the protective casing that houses the IC and provides electrical connections to the outside world.
- The package serves several essential functions, such as protecting the chip from physical damage, dissipating heat, and providing a standardized interface for connecting the chip to external devices or a printed circuit board (PCB).



Type of Integrated Circuits

Analog on TOP (AOT)

- Designed to work with continuous signals, such as sound, light, or temperature. Can measure, amplify, filter, and process continuous signals. Can process signals with high fidelity
- Require high precision in their design and manufacturing to minimize signal distortion and noise
- Can operate at lower frequencies and with lower voltages than digital circuits. Consume less power and generate less heat
- More complex to design and manufacture than digital circuits, sensitive to temperature changes, noise, and interference.
- Less flexible than digital circuits, as they can only process continuous signals and cannot perform logical operations.
- They typically use components such as resistors, capacitors, and inductors to manipulate these signals.
- Examples: amplifiers, filters, oscillators, and voltage regulators.

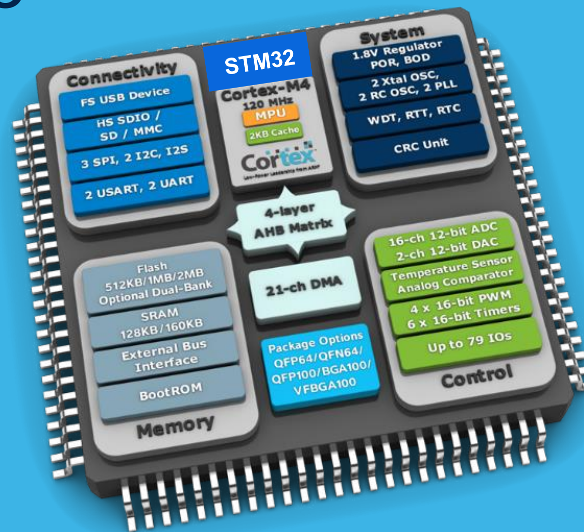
Digital on TOP (DOT)

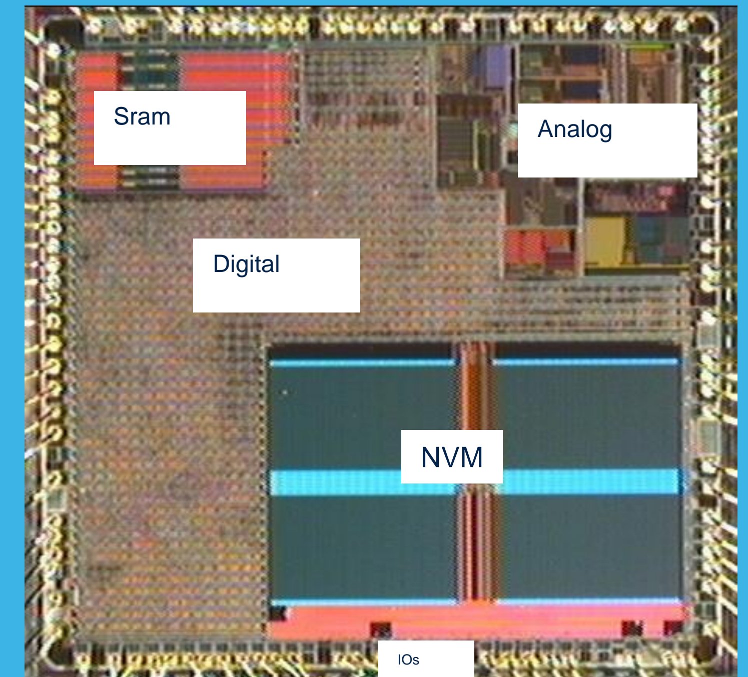
- Designed to work with digital signals, which can only have two states, typically represented as 0 or 1
- Digital signals are discrete and have specific voltage levels that correspond to each state
- Can process and manipulate these signals using logic gates and flip-flops, which are components that can store and manipulate digital signals
- Can perform logical operations on digital signals, which makes them suitable for a wide range of applications, from simple calculators to complex computer systems.
- Can also be easily reprogrammed to perform different tasks.
- Less sensitive to noise and interference. Less susceptible to analog effects due to discrete nature
- Consume more power, require higher voltages and operate at higher frequencies.
- Less accurate can introduce errors and noise in the digital signal.
- Examples: microprocessors, memory chips, and digital signal processors

Source: https://asicslearning.info/posts/analog-vs-digital-on-top

Microcontroller SOC

- ARM Cortex M CPU
  - NVM for Code Storage
  - SRAM
  - Digital peripherals
  - Analog Ips
  - Ios



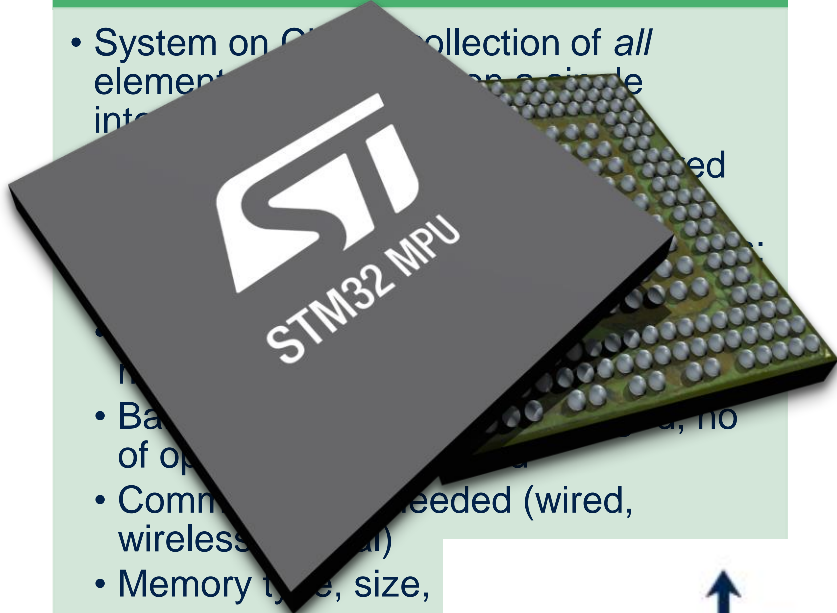


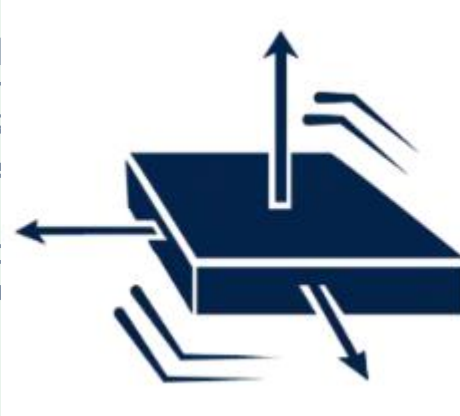
- **Designed in eNVM technology**

SOC, ASIC, FPGA

SOC

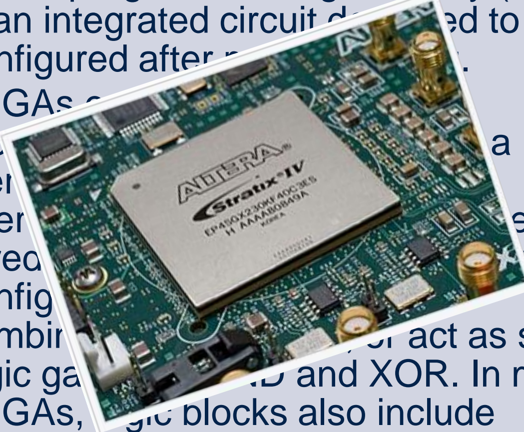
- System on C... collection of *all* element... on a single int...
- ...ed
- Ba... of op...
- Comm... eeded (wired, wireless...al)
- Memory ty...e, size, ...
- Extensions: standar... PCI(x)), Serial (UAR... I3C), proprietary, de... SWD)
- Device connectivity:... (temp, voltage, curr... (current, process)
- Testing/monitoring





FPGA

- A field-programmable gate array (FPGA) is an integrated circuit d...ed to be configured after ...
- FPGAs c... pro... a hier... inter... e wired... e config... combin... act as simple logic ga...D and XOR. In most FPGAs, ...gic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.
- FPGAs h... n embedde... nt, it allow various s... gn iterations ... system architect...
- FPGAs c... in comparis... n speed.

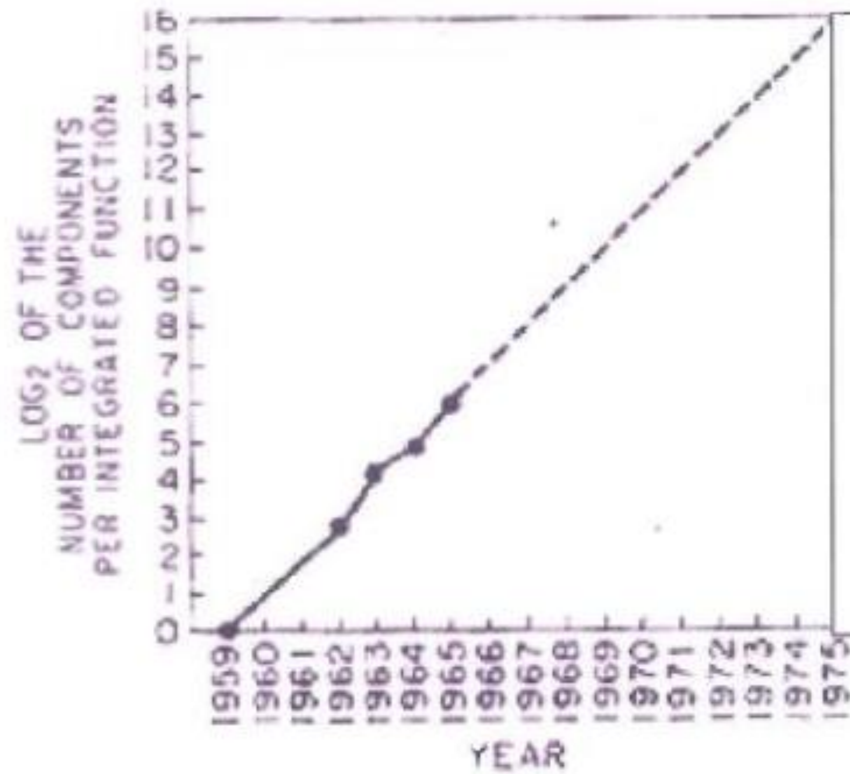


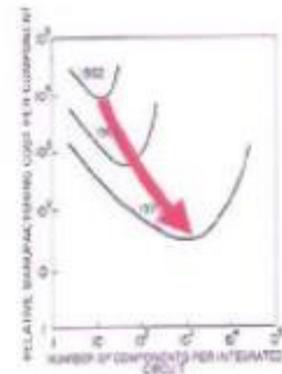
ASIC

- When a SOC is Application specific it becomes ASIC
- It can have a processor... depending on app...
- Optimized ...

Beyond Moor’s

Moor's Law - 1965

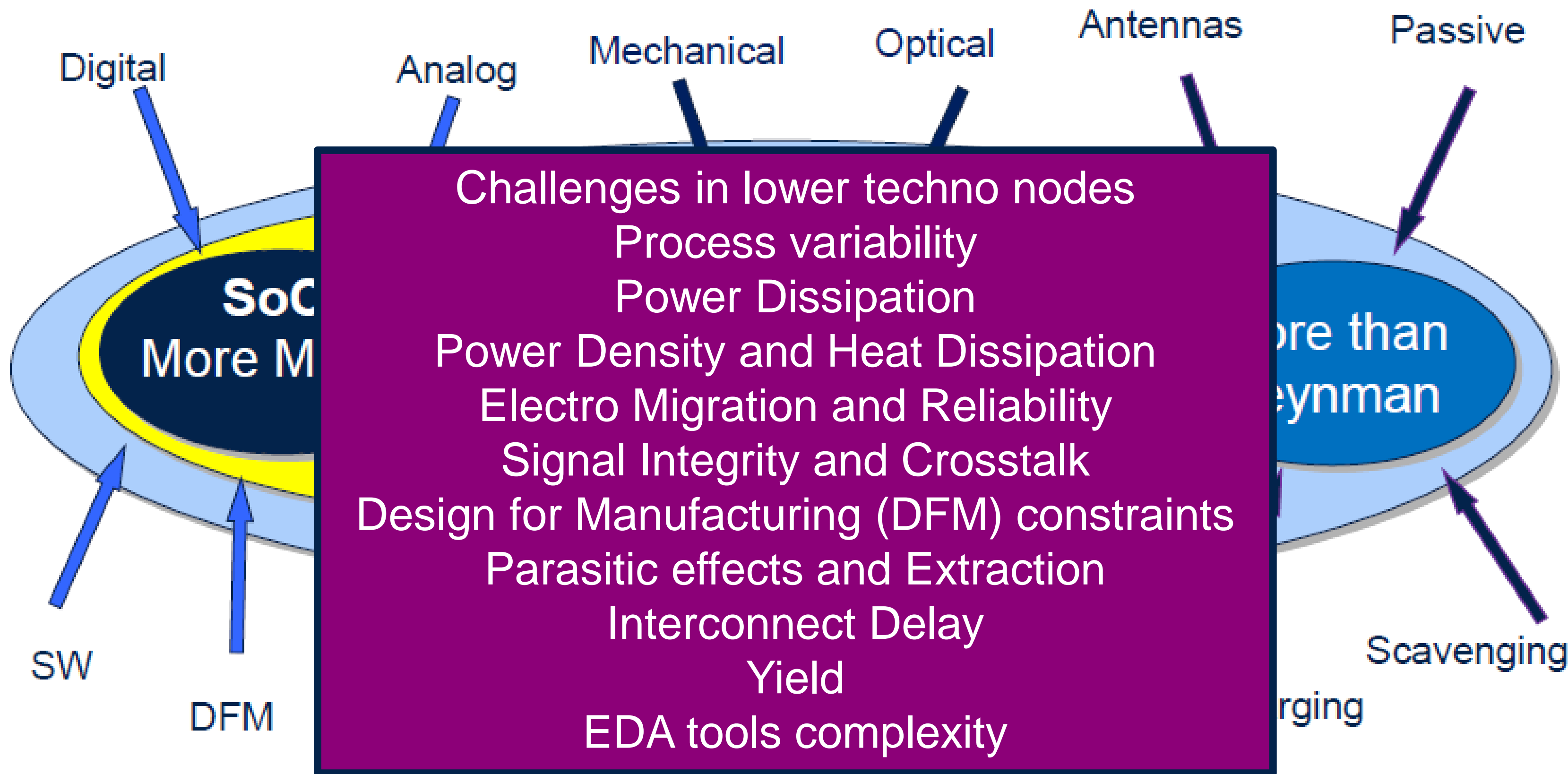




"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38, Number 8, April 19, 1965

Technology Evolution

Number of transistors in an integrated circuit (IC) doubles about every two years – Gordan Moore 1965



There's Plenty of Room at the Bottom: An Invitation to Enter a New Field of Physics - Richard Feynman (29/12/1959 – Caltech) ***arrange the atoms the way we want***

Courtesy: Bruno Murari, Scientific Advisor, STMicroelectronics

SIP, Chiplets

SIP

- SiP: System in a package are like systems on a chip (SoCs) but less tightly integrated and not on a single semiconductor die. SiP solutions may require multiple packaging technologies, such as flip chip, wire bonding, wafer-level packaging and more

Chiplets

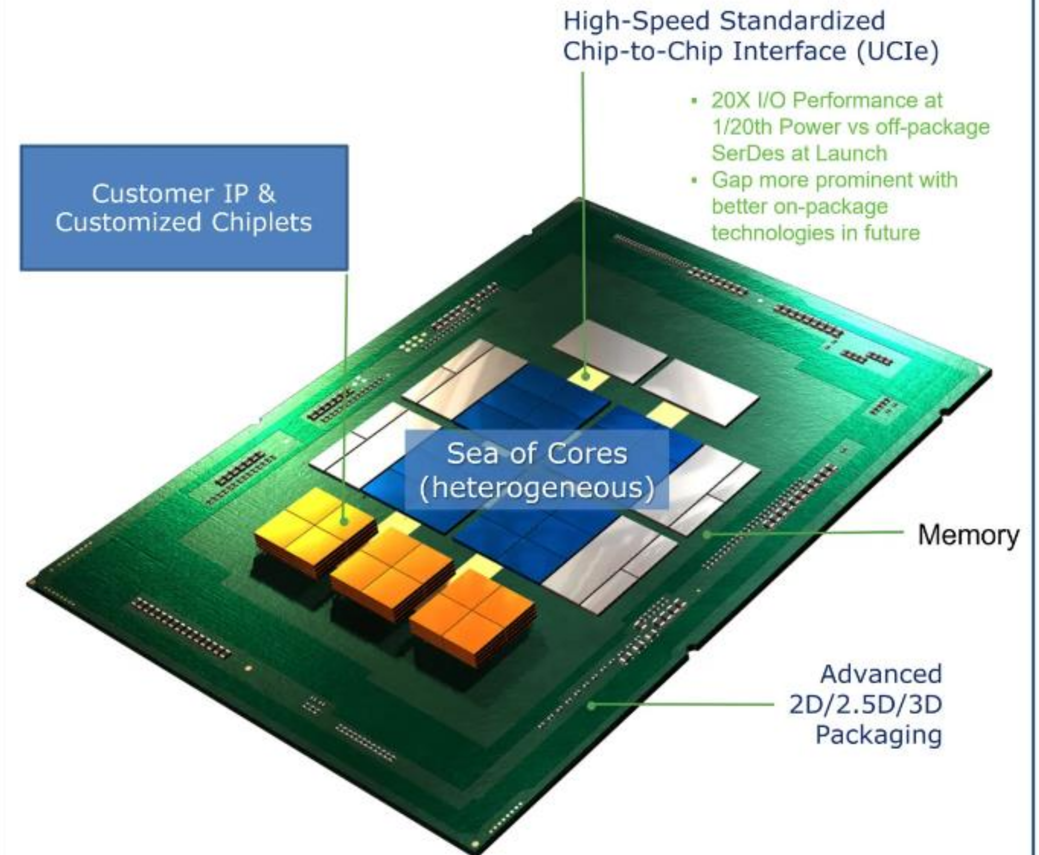


Image: UCIe

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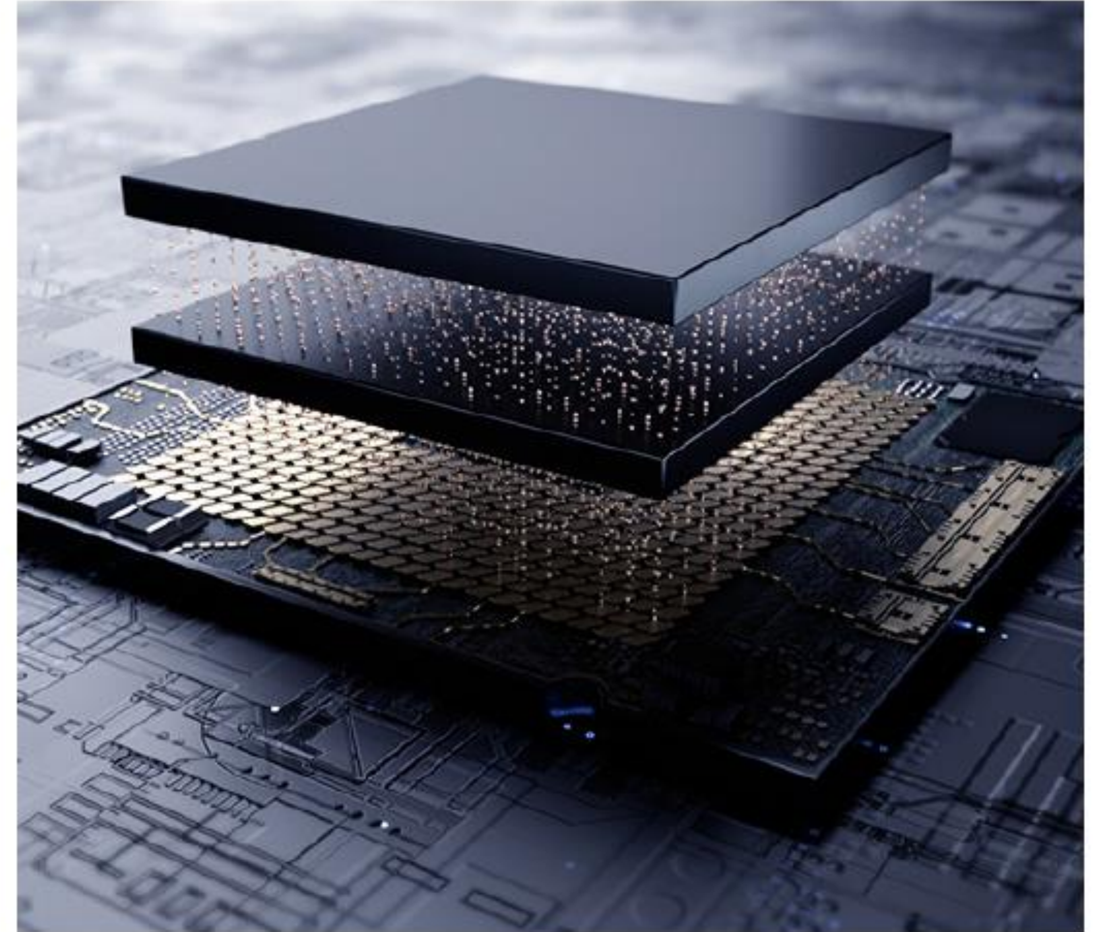
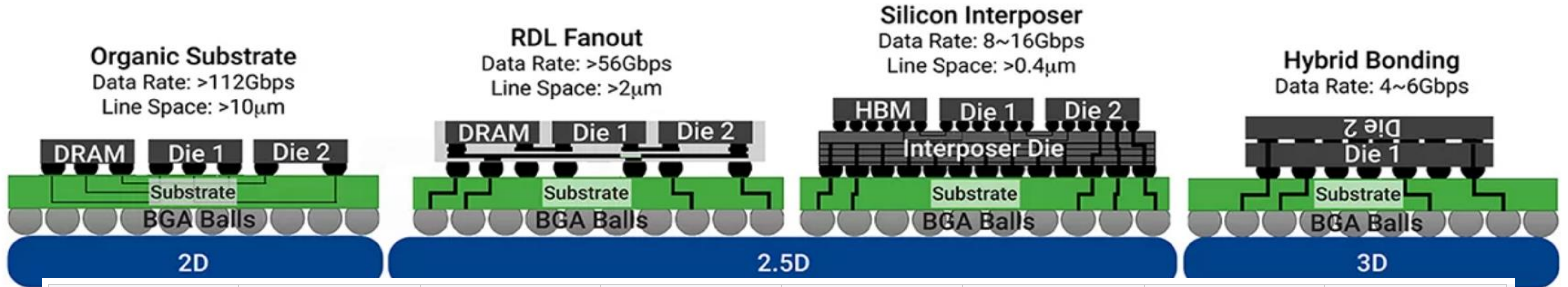
Multi die

- 3D IC packages save
  - Save Area: Stacking components vertically, reducing surface area and bumping
  - Increase performance: by shortening the space between chips.
  - Reduce risks: in comparison to big die implementation
  - Low costs: retaining high bandwidth and low power performance.



2D, 2.5D, 3D Packaging Options



Standard	Data Rate [Gbps]	Bump Space [um]	Power Efficiency [pJ/bit]	Edge Density [Tbps/mm]	Area Density [Tbps/mm2]	FOM-1 [Tbps/mm / pJ/bit] *Larger is better*	FOM-2 [pJ/bit / mm] *Smaller is better*
AIB 2.0	6.4	55	0.5	1.64	-	3.28	0.1
OpenHBI 1.0	8	40	0.4	2.29	2.04	5.71	0.1
OpenHBI 2.0	12~16	40	0.5	3.34	3.06	6.86	0.06
BoW – Basic	8	40	0.5	1.78	1.07	3.56	0.1

Parallel die-to-die interface standards for advanced packaging

Image courtesy: Synopsys, OCP Tech Week, Nov 2020)

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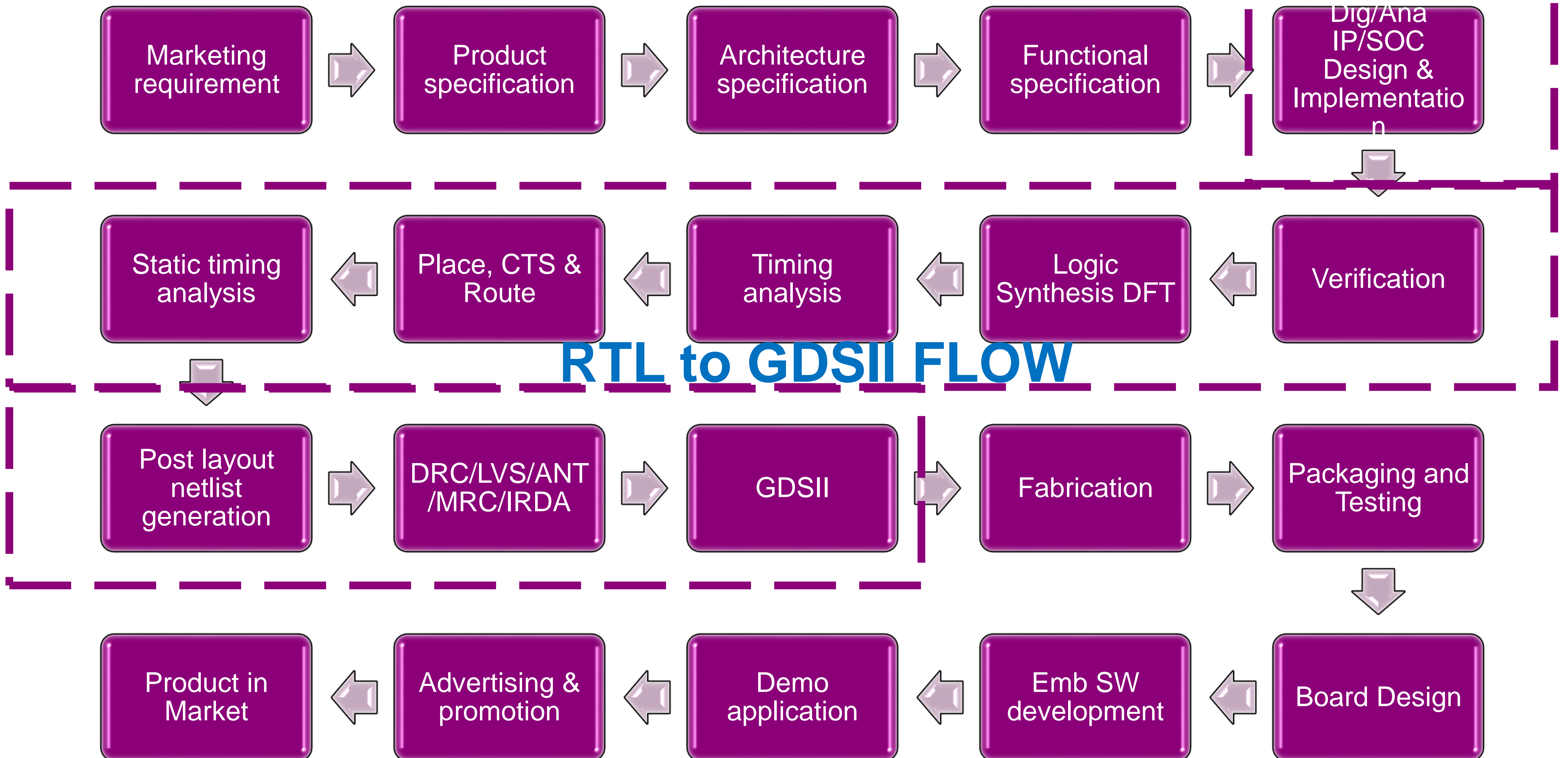
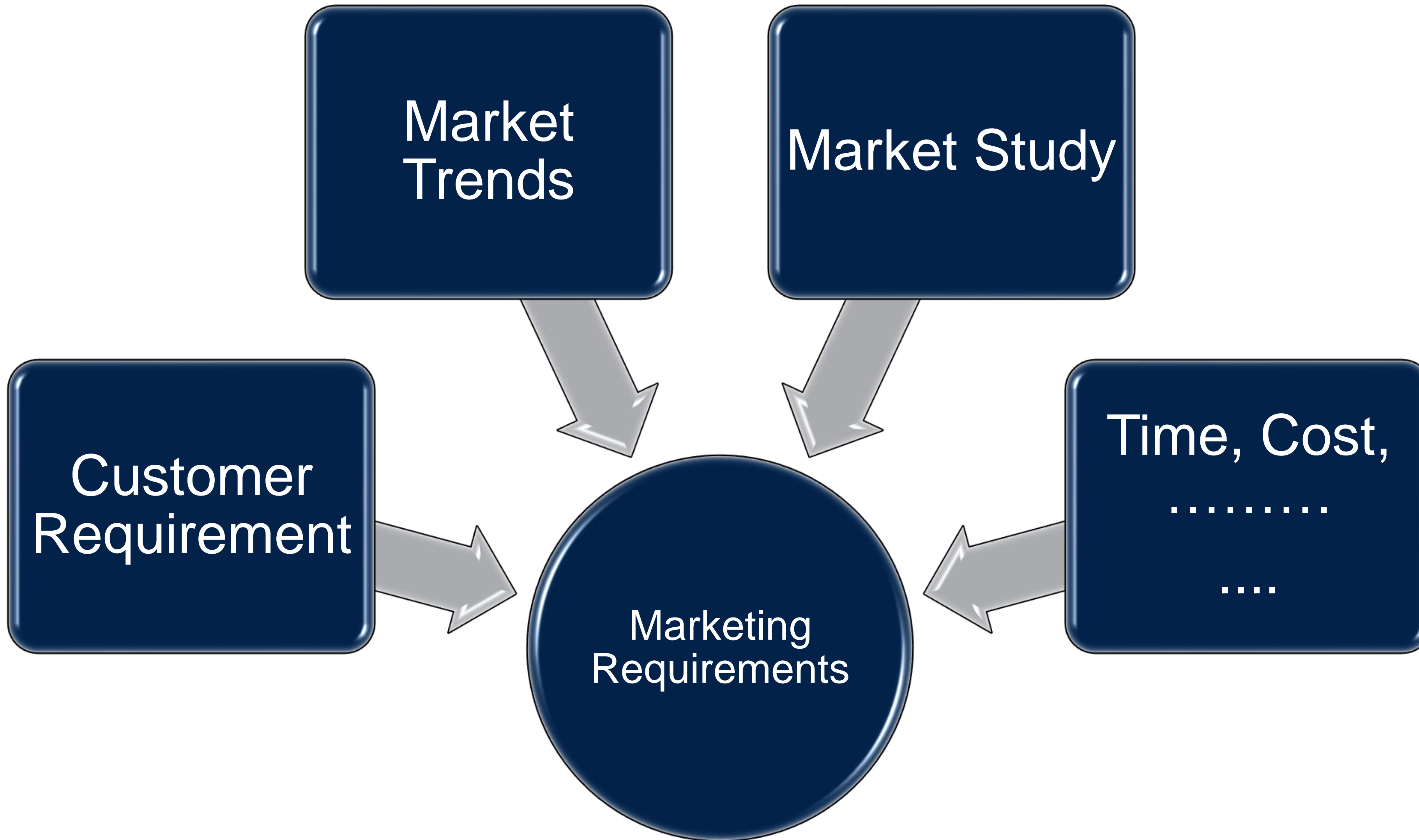
Let's see product design flow

Product design flow



Marketing

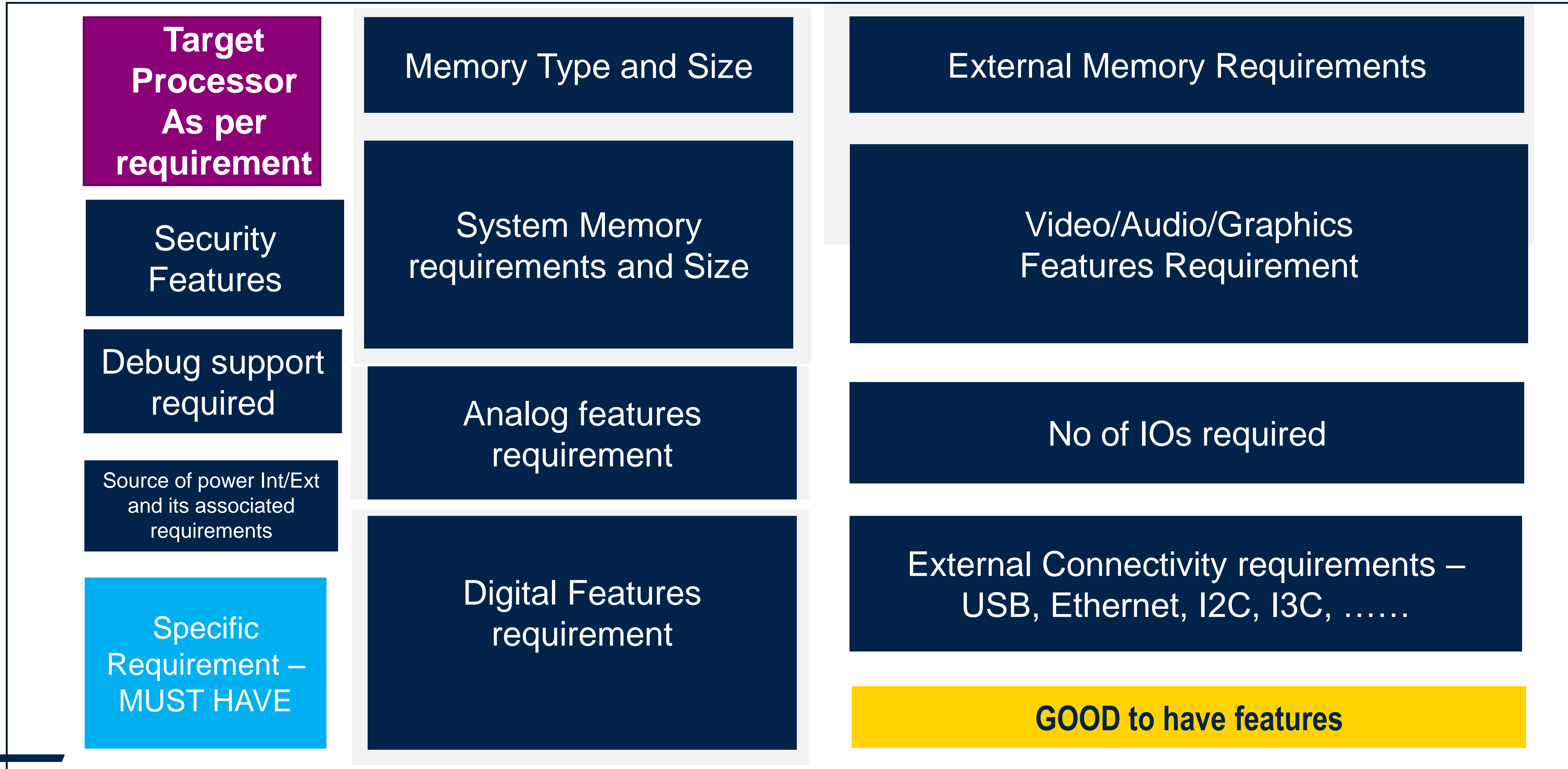


Brings to table Customer/Market expectations:

- Product name
- Business case
- Target market
- Features superset
- Variants proposal
- Road Map
- Technology
- SWOT
- …

Product Specification - Superset of requirements

Required Embedded Memory, Required performance, Required power management, Required connectivity



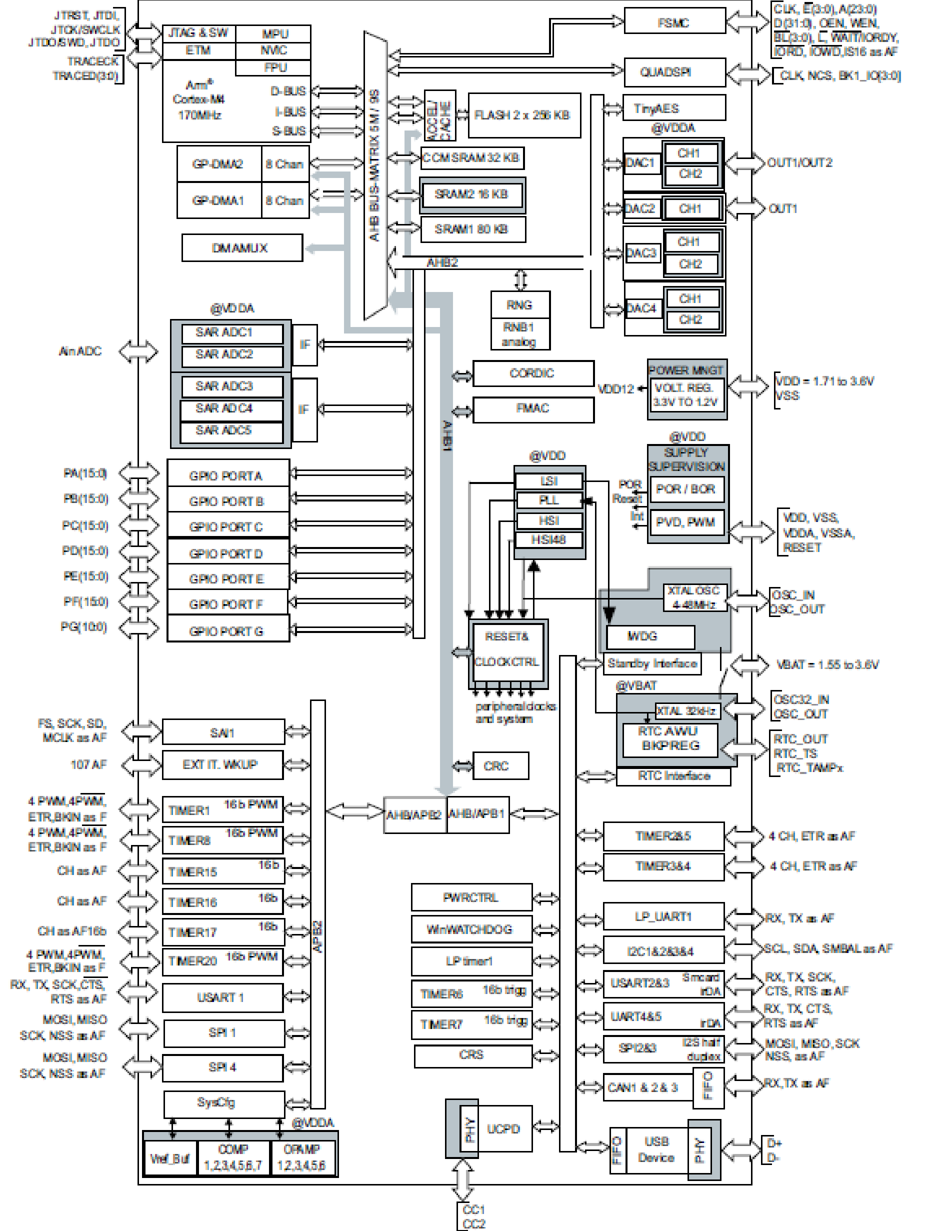
Architecture – translating market expectation to specification

- Architecture specification
  - IP(s) required, no of instances of IP, configuration of each IP
    - Generic IP or SoC IP decision is taken
  - Memory Map
  - Interrupt Map
  - DMA requirements
  - Memory cuts requirements
  - Frequency requirements
  - Security Requirements

Datasheet

STM32G473xB STM32G473xC STM32G473xE

Arm® Cortex®-M4 32-bit MCU+FPU, up to 512 KB Flash, 170 MHz / 213 DMIPS, 128 KB SRAM, rich analog, math accelerator



- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from Flash memory, frequency up to 170 MHz with 213 DMIPS, MPU, DSP instructions
- 7 x 12-bit DAC channels
- 16-channel DMA controller
- 5 x 12-bit ADCs 0.25 µs, up to 42 channels. Resolution up to 16-bit with hardware oversampling, 0 to 3.6 V conversion range
- 7 x ultra-fast rail-to-rail analog comparators
- 6 x operational amplifiers that can be used in PGA mode
- 14 timers
- Calendar RTC with alarm, periodic wakeup from stop/standby
- 3 x FDCAN, 4 x I2C , 5 x USART/UARTs, 1 x LPUART, 4 x SPIs, 1 x SAI, USB 2.0, USB Type-C, IRTIM

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Chip/SOC Lead/Management

- *A product is design under collaborative effort of various teams, people and individuals.*
- *Role of Chip Lead or SOC Lead or Project Lead is to act as bridge between various stakeholders.*

Product Marketing

Security Architect

Embedded SW

Application

Digital IP design

Digital IP Verification

Analog IP design and Verification

IO Design

Product Engineering

Test Engineering

BE Implementation

DFT

Quality

FPGA Integration and Board

Emulation

Packaging

Analog Mixed Signal Verification

Activity Leads

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Design and implementation

Processor
Analog IP
Verification
SOC IP
Verification
Compile
Elaborate
Sanity Check
Constraints
Specification
IP 1,2,3….100 ..120..150..200
SOC Integration
Synthesis
Digital IP
Verification
Memory
IO
LINT
CDC
SOC Verification
RDC
UPF
Netlist

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CDC/Lint/RDC

Metastability

- How do you ensure that you have handled metastability across clock domains, so it does not affect design functionality?

Reconvergence

- How do you ensure that a group of converging synchronized control signals are in sync at a particular clock cycle?

Data hold (data loss)

- How do you ensure that data from one clock domain is held long enough to be captured by the other clock domain? (Fast to slow clock, data enable sequencing)

Design intent across clock domains

- How do you ensure that more sophisticated synchronization schemes (such as handshake, FIFO) behave according to your specifications?

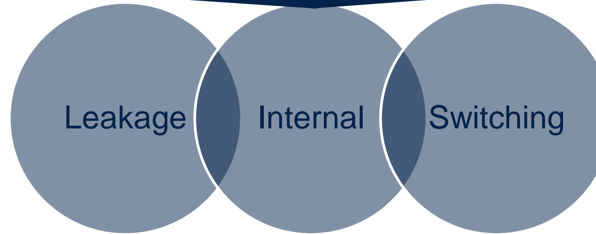
Reset Synchronization

- How do you ensure that an asynchronous set/reset is properly synchronized for a set of flops and the reset is asynchronously asserted and synchronously de-asserted

- Different flows available for SoC CDC analysis.
  - Grey box (ip_block) approach.
  - Full flat approach.
  - Abstraction based approach.
- There are pros and cons of each approach

Criteria	Full Chip in normal flow	IP_BLOCK	Full chip with abstraction flow
Synthesis required for blocks ?	Yes	Yes	No
Run-time	High	Medium	Low
Noise	High	Medium	Low
IP validation checks	No	No	Yes
Convergence checks	Yes	No	Yes
Functional checks	Yes	Yes	No
SGDC complexity /Setup Effort	High	Medium	Low
SDC complexity	High	Medium	Low

Low Power



	Leakage	Switching	Internal	Total
Sequential	2.368	40.475	160.38	203.223
Clock_cell	0.188	26.52	24.531	51.239
Memory	5.53	19.38	177.28	202.19
Combinational	28.7336	490.38	350.86	869.9736
IO	45.35	0.155	0	45.505
PLL				16
Total	82.1696	576.91	713.051	1388.131

SAMPLE

What can be done ?

Architecture Level

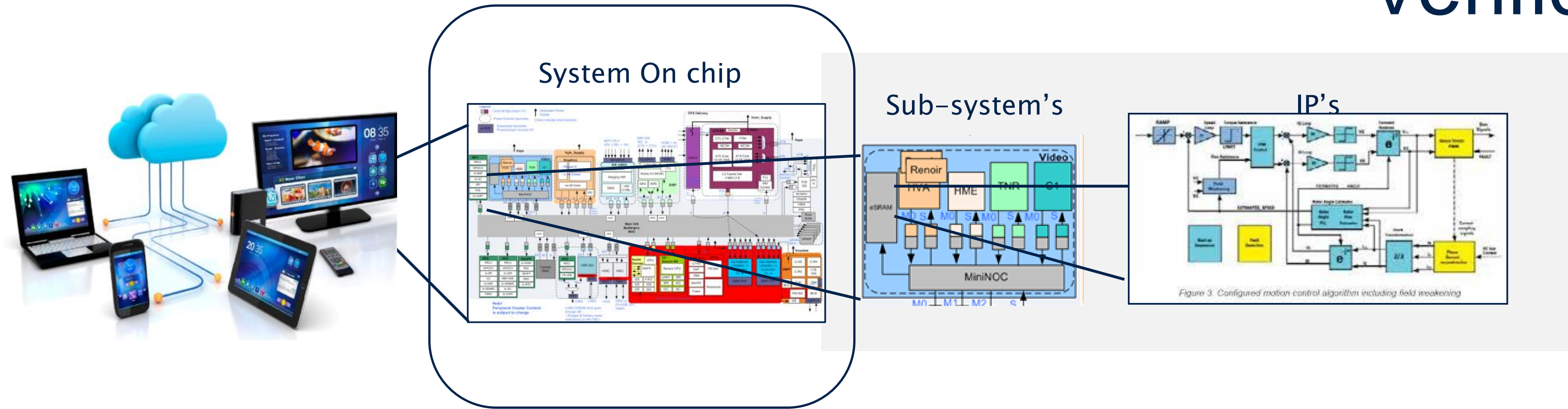
- Module level clock gating. Frequency scaling
- Voltage scaling

Implementation Level

- Automatic clock gating. Multi-vt design
- Data pipelining

RTL Level

- Clock gating, managing clock enable in data. Shift registers, grey pointers, state machine optimization., IDLE bus management
- Memory optimization: slicing, throughput, SP vs DP
- Split big counters. Out of BOX



SoC Verification

- Connectivity
- Interoperability
- Performance - Application Scenarios

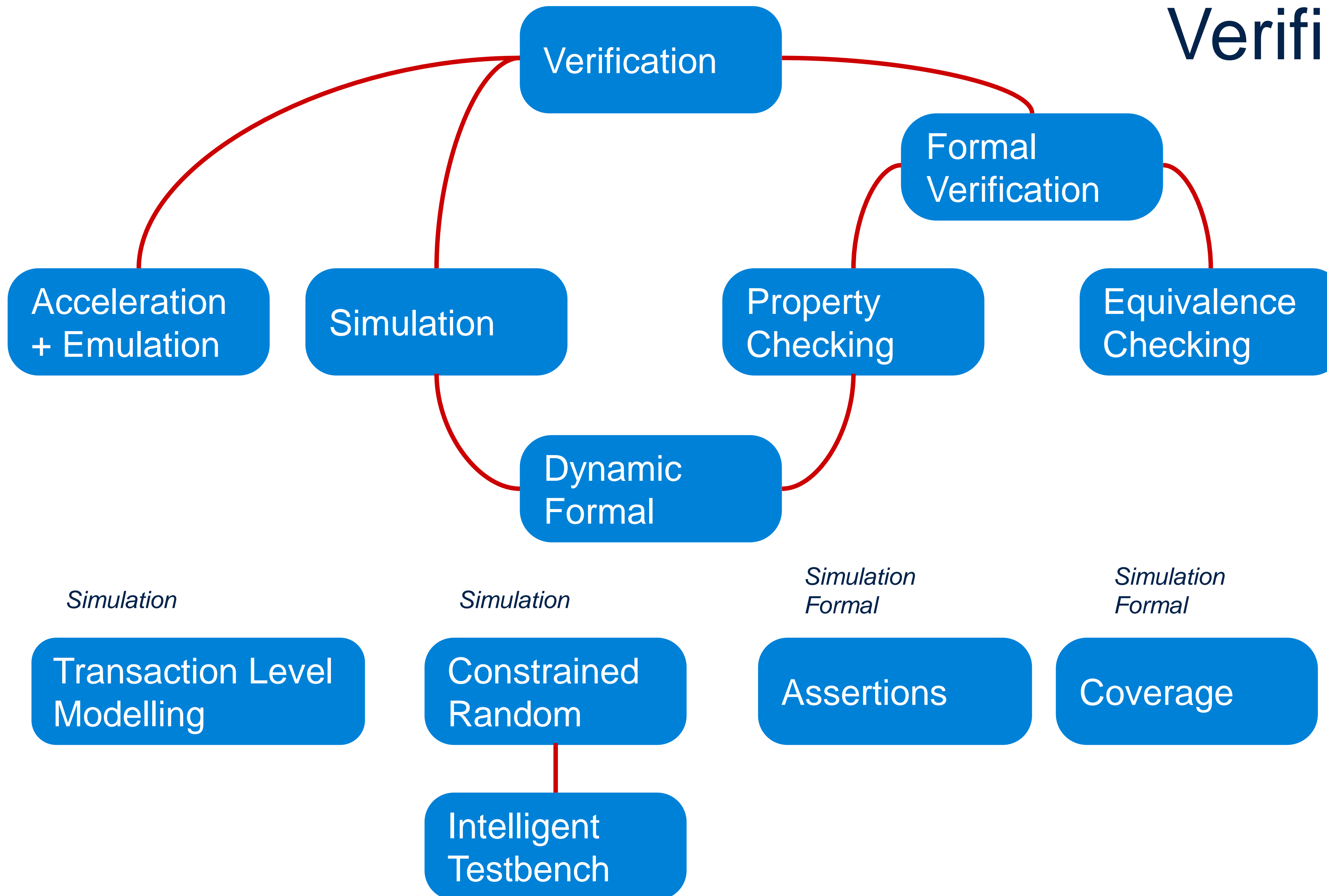
Sub System Verification

- Connectivity
- Interoperability
- Performance - Application Scenarios

IP Verification

- Functionality
- Protocol Compliance
- Standard Compliance
- Performance - Application Scenarios

Verification Space



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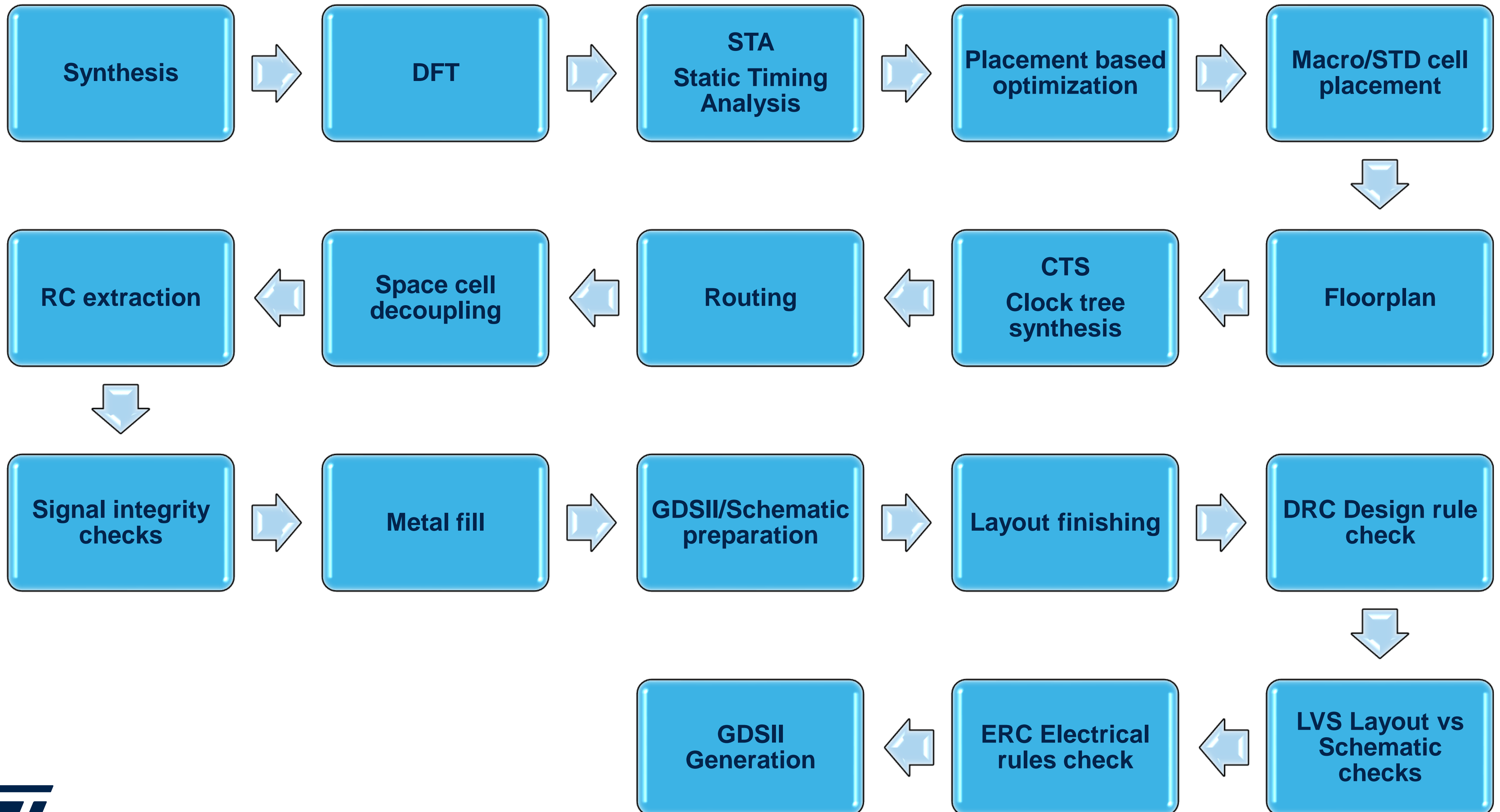
Physical Implementation



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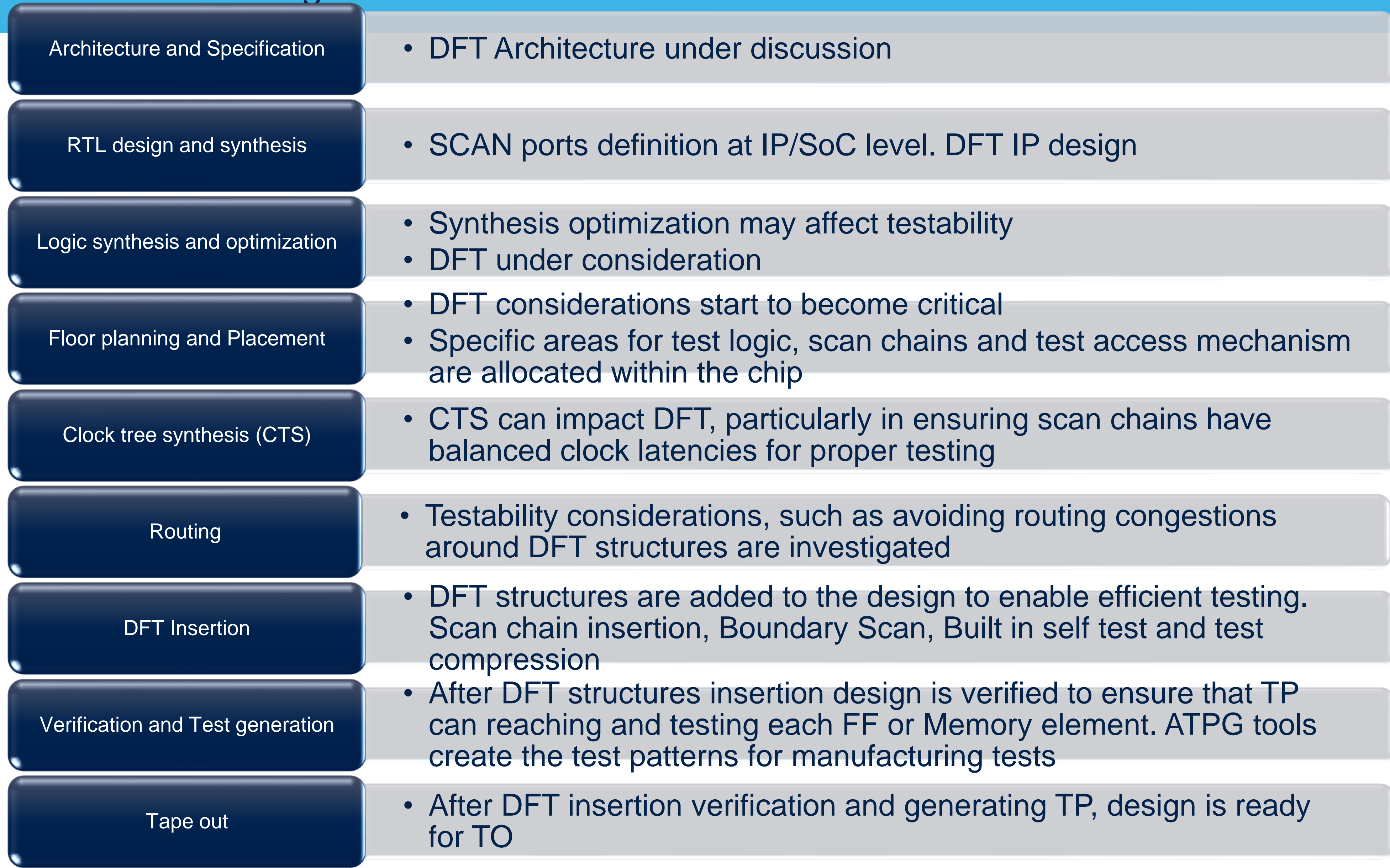
DFT

- A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.



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CAD and Methodology

- Infra management
  - Project disk space, Version control system
  - License – EDA tools, EDA AE enablement
  - NDA (Non-Disclosure Agreement)
  - Co-ordination with IT team
- Flow & Methodology development
  - Define methodology (process) to define common agreed way of working
  - Flow development around EDA tool
  - Custom Flow development (in-house scripts)
  - Automation to convert external vendor provided data structure as per STM needs
  - Local support to design team on STM internal tools, created by global teams

- Productivity: Avoid effort on tasks which are repetitive in nature
- Re-use: Maximum re-use as created flows are generic & scalable
- Quality: Same issue doesn't get repeated once fixed
- Design: Allow design team to focus on actual design issues
- Business: Allow to meet 'time to market' due to zero effort on repeated tasks

EDA Tools in RTL2GDS flow

	Tool Name
Documentation	IPXACT
Modelling	SVRN - System Verilog Real Numbers, C/C++, MATLAB, SciLAB, UML
Scripting	Python, Shell, PERL
High Level Synthesis	Catapult, HDL Coder, Vivado
RTL Design	VHDL, Verilog, System Verilog
Verification Language, Methodology, Simulators	Language (Verilog, System Verilog, C, Assembly) Methodology (UVM, Metric Driven) Formal Tools (CDNS JG Apps, VCS) Simulators (Xcelium, VCS, QuestaSim)
Emulation/Acceleration	Veloce, Zebu, Palladium, Protium
Coverage Analysis	Siemens Questa Cover, CDNS Incisive Enterprise Simulator (IES), SNPS VC Formal
Synthesis	SNPS DC, CDNS Genus, Siemens Précision
Floor planning, Placement, Routing, CTS	CDNS Innovas, SNPS ICC2, Siemens Olympus-SOC, Siemens Calibre
DRC/LVS	CDNS Virtuoso, SNPS IC Validator, Siemens Calibre
Static Timing Analysis	SNPS PrimeTime, CDNS Tempus, Siemens Calibre
Power Analysis	SNPS Primepower. CDNS Tempus, Siemens Calibre
Scan Insertion	SNPS DFT Compiler, CDNS Encounter Test, and Siemens Tessent
ATPG	SNPS TetraMAX, CDNS Encounter Test, Siemens Tessent
Boundary Scan	Corelis ScanExpress, JTAG Technologies ProVision, and XJTAG
Memory BIST	Synopsys STAR Memory System, Cadence Encounter Test, and Mentor Graphics Tessent
Logic BIST	Synopsys TetraMAX DFTMAX, Cadence Encounter Test, and Mentor Graphics Tessent
DFT Compilers	Synopsys DFTMAX, Cadence Encounter Test, and Mentor Graphics Tessent.
Fault Simulation	SNPS VCS Fault, CDNS Incisive Enterprise Simulator

Fabrication

- Semiconductor Manufacturing flow

- Semiconductor devices are manufactured in Wafer fabs through a process known known as wafer fabrication.
- Circular wafers of silicon are put through a cycle of chemical processes in order to etch an ion-charged transistor array as patterned on a set of masks.
- On top of the transistor array, layers of metal interconnect form pathways between the transistors; the layers are insulated by a dielectric material
- After wafer processing, the finished wafer is put through a dicing process, where individual die are separated.
- These are sent to a back-end facility for packaging and assembly and final test.

Wafer Manufacturing

Key Steps:
Crystal Pulling
Crystal Slicing
Wafer Lapping and Polishing
Cleaning
Oxidation

Wafer Processing

Key Steps:
Chemical Vapor Deposition
Coating
Align and Expose
Develop and Bake
Etch and Strip Resist
Ion Implantation
Physical Vapor Deposition
Chemical Mechanical Planarization (CMP)
Passivation
Wafer Probe/Test

Dicing

Key Steps:
Dicing

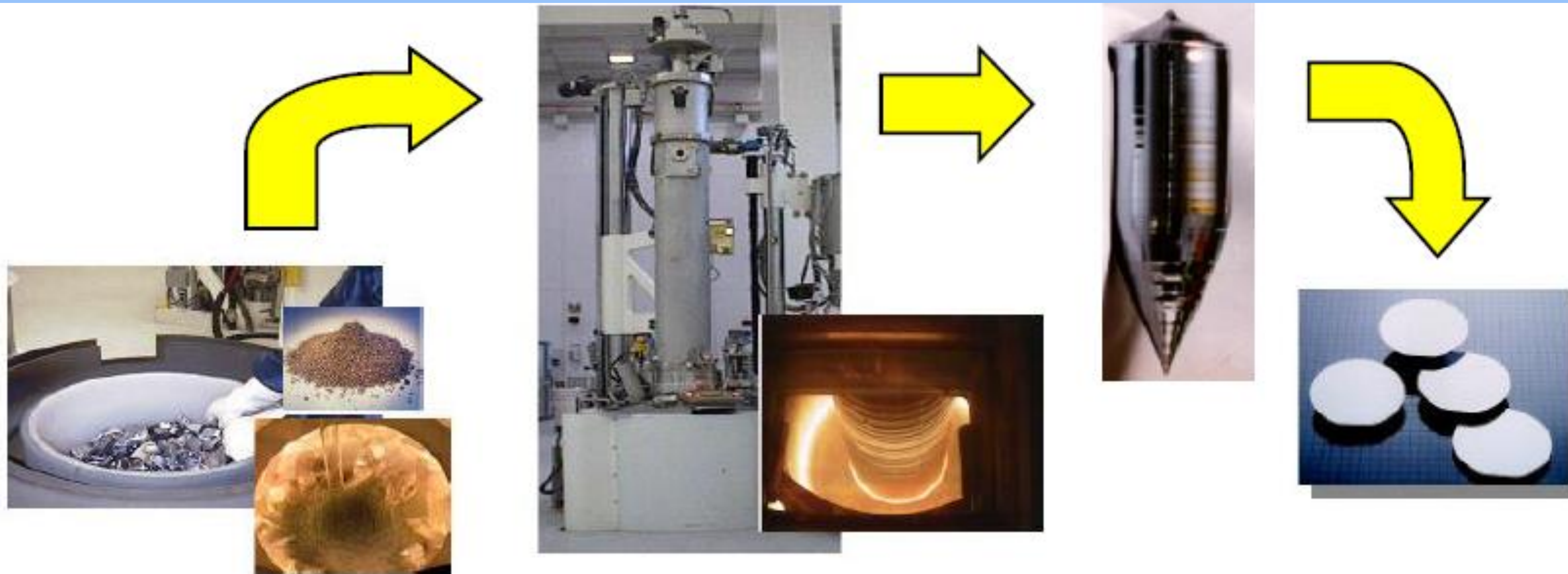
Assembly & Packaging

Key Steps:
Die Attach
Wire Bond
Encapsulation and Finishing
Final Test

Source: Oppenheimer & Co.

Wafer Manufacturing

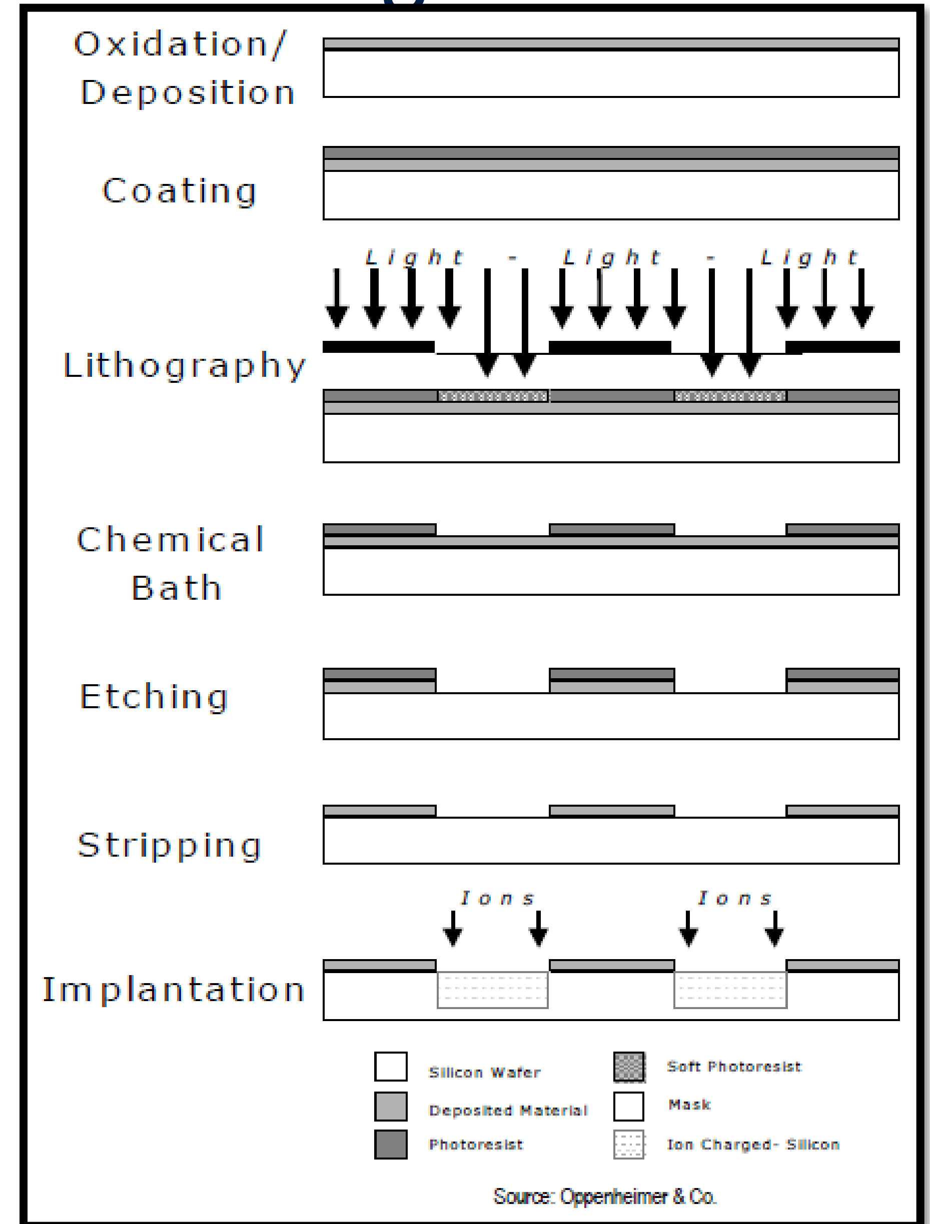
- Silicon wafers are produced by heating a mixture of silica and carbon in a furnace, creating wafer-grade silicon.
- A seed is then dipped into the molten silicon and is slowly twisted and pulled out.
- This creates a cylindrical ingot several feet long, which is ground to an appropriate diameter (200mm, 300mm, etc.).
- The ingot is then sliced into thin wafers for shipment to IDMs and foundries.



Source: MEMC, Oppenheimer & Co.

Wafer Processing – Pre-Metal

- In the pre-metal stage, wafers are put through an intense cycle of chemical processes in order to etch a transistor array patterned on a set of masks.
- Through cycles of *deposition/oxidation*, *photolithography*, *etching*, and *ion implantation*, the transistor array is created.
- Charged ions are then deposited to enable transistor functionality.



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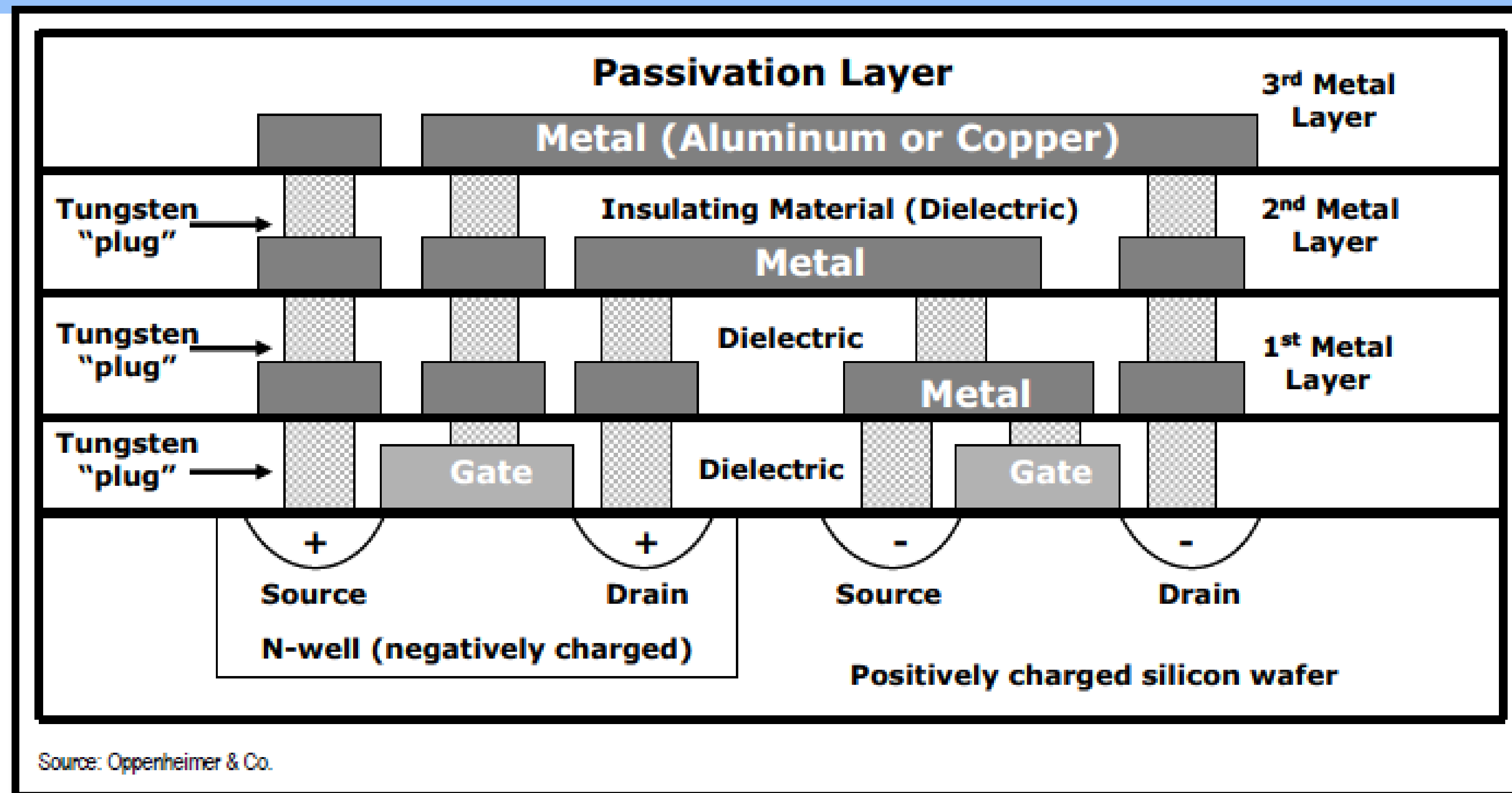
Wafer Processing - Interconnect

- After the transistors are created, they are connected to form logic gates using an interconnect material, usually aluminum or copper.
- The metal layers are built with stages of deposition, lithography, and etching, similar to the pre-metal stage but using separate equipment and masks.
- Dielectric material is deposited between the layers to insulate them from one another.



Source: Oppenheimer & Co.

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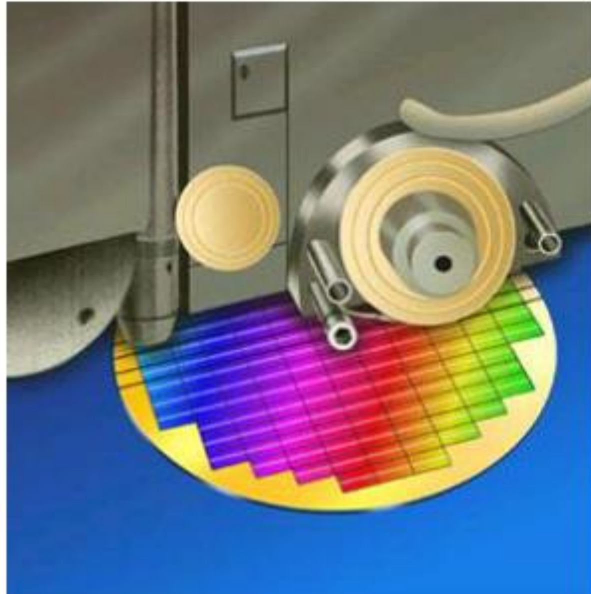
Dicing

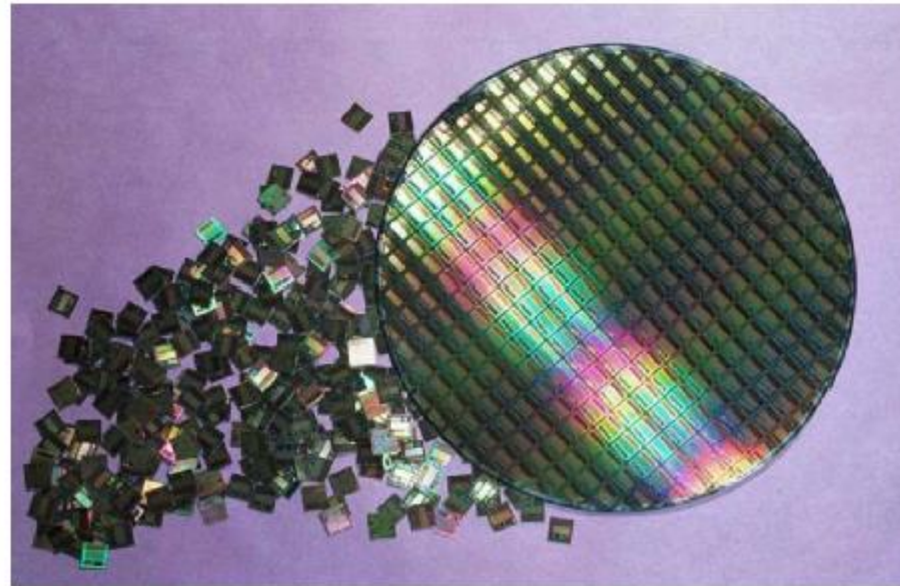
- After the wafer is processed, a diamond drill is used to slice the wafer into individual die.
- Each die is tested before being sent to the back-end facility.

Semiconductor Dicing Diamond Drill



Source: IBM

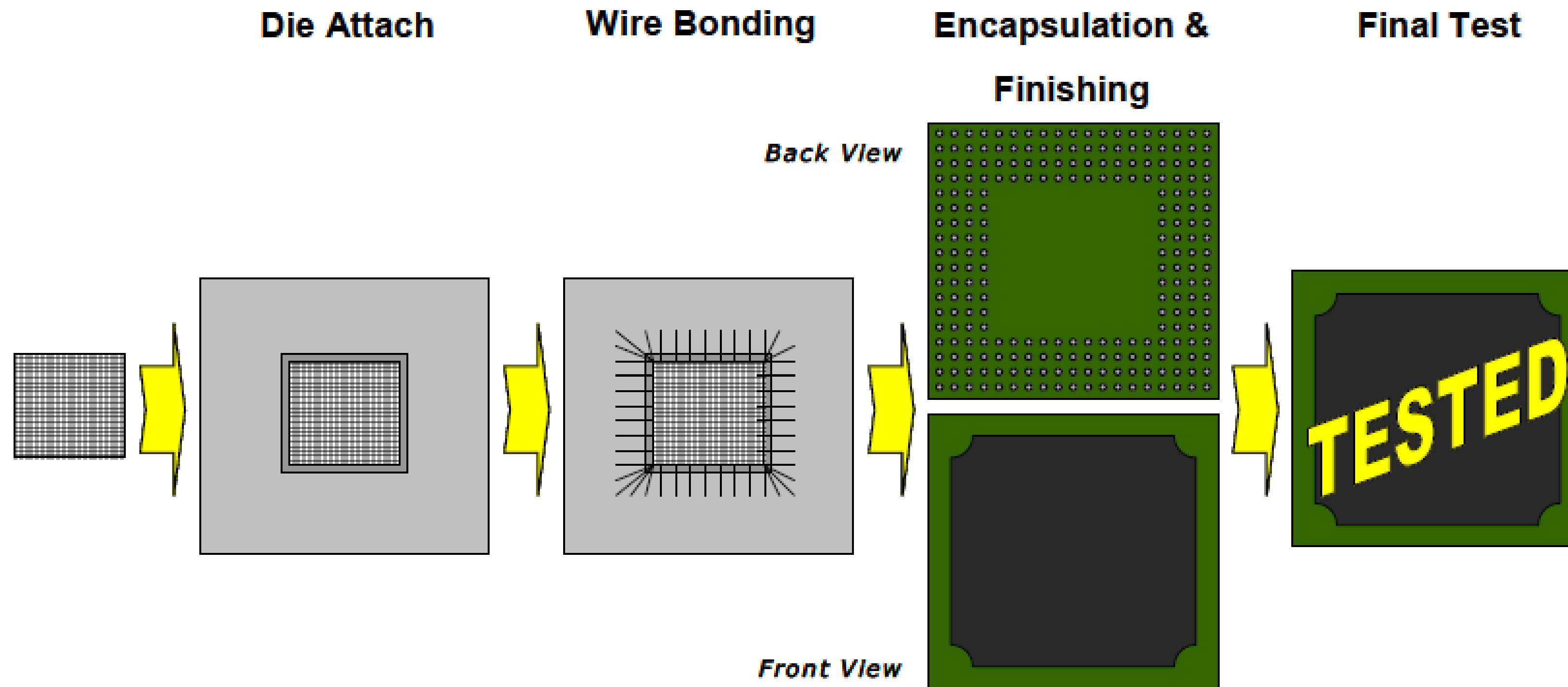
Finished Wafer and Individual Die



Source: LSI Logic, Denali Software

Back End: Assembly and Test

- The individual die are sent to a back-end assembly facility, where they are attached to a package, wire bonded, encapsulated, and run through final test.



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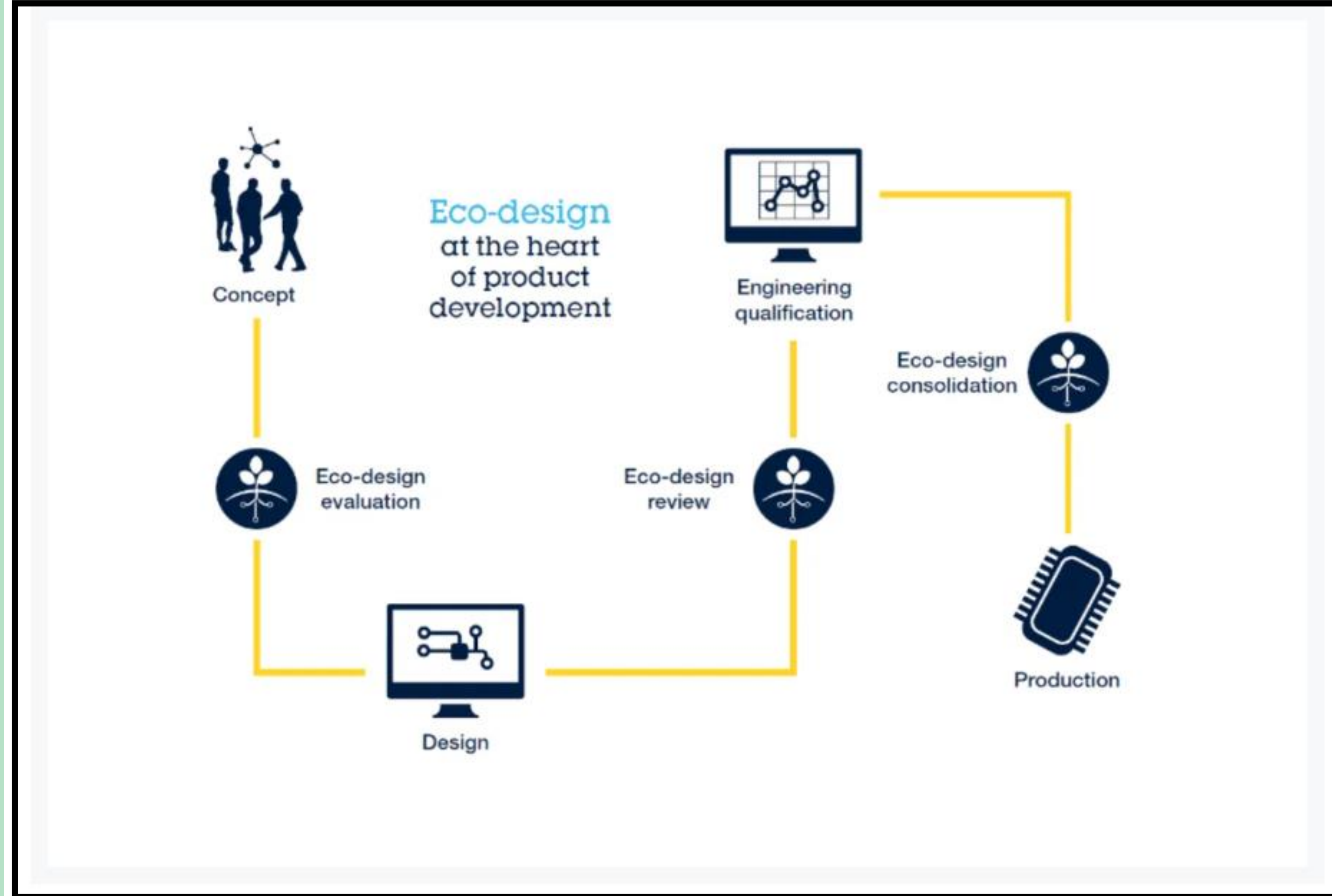
Sustainable Development

- **Environmentally & socially responsible products & applications**
  - We identify and promote innovative products that provide society with environmental and social benefits. In our Sustainable Technology program, we classify our products into four categories of responsible products:
    - **Low carbon products**
      - Thanks to optimized conception, these products reduce the footprint of our production equipment, utilities, and supply chain.
    - **Power efficient products**
      - State-of-the-art in reducing electricity consumption or power losses, these products reduce the footprint of the end-devices they are embedded in.
    - **Planet friendly applications**
      - Products that are key contributors to green applications, such as automotive powertrain electrification, solar panels, LED lighting.
    - **Human welfare applications**
      - Products that are powerful enablers for medical, health, safety, and security applications.



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How to be part of semiconductor industry

Knowledge

- Device Physics, Quantum effects
- Linear Algebra, probability, entropy, stochastic process
- Basics of Electrical Systems
- Basics of material science
- Signals and Systems
- Computer architecture (Advanced), microprocessor and microcontroller
- Electronics (Digital, Analog))
- Communication Theory
- Algorithms
- Digital Signal Processing
- VLSI (Architecture, Design, Verification, Physical Design, DFT, Mixed Signal Design, Fabrication)

Skills

- Passion, analytical thinking
- Digital electronics
- Analog fundamentals
- CMOS
- C, C++, Assembly Language
- VHDL, Verilog, System Verilog
- UVM
- Schematic, Layout design
- Scripting: UNIX, Shell, Perl, Python

Career Opportunities in VLSI domain

Domain					
Architect	SOC	Dig IP	Power	Security	
IP	Digital Designer	IP Verification	Analog Design	AMS Design	AMS Verification
SOC	SOC Lead	SOC Design	SOC Verification	Emulation	TB Architect
Physical Implementation	PNR	STA Expert	Layout and Schematic	DRC/LVS	
DFT	Verification	Test Engineer			
CAD/Meth	Automation Expert	Modelling	Packaging	Lib design	
Misc	Program Management	Domain Leads	Packaging	IO designer	Performance and Modelling

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Back UP

Slides to add

- Research topics as part of sustainability slides
- 5 days flow from soc to industry
- UPF/Constraints
- ~~Future applications~~
- Metric driven verification flow
- Skills/subjects required for VLSI
- ~~Why VLSI as profession~~
- ~~Importance of VLSI in our world – semiconductors will decide geopolitics of world around us~~
- ~~Speaker profile~~
- Addling laws of physics which play crucial role (slide 19)

Validation

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Quality

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