Pegasus Physical Verification

Massively scalable, provides the best cost of ownership

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Introduction

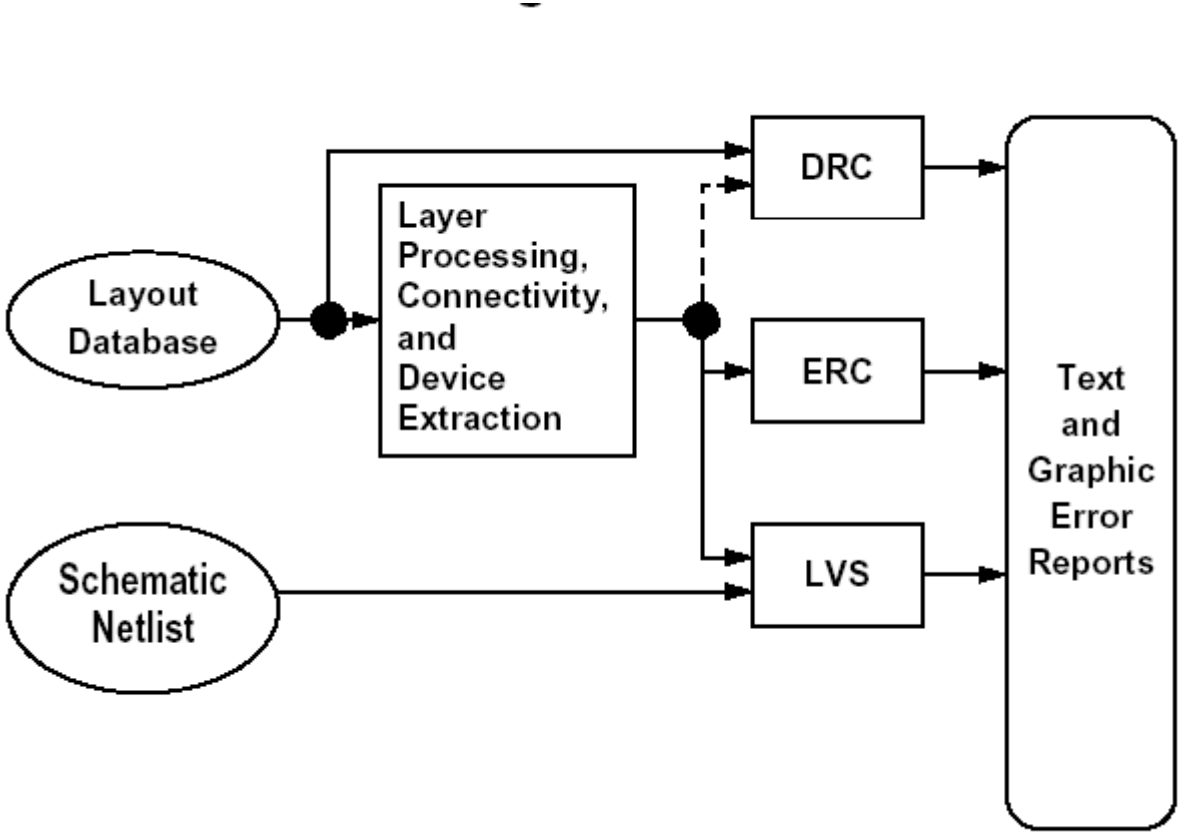
- Amit Kothari has been working for Cadence Design Systems India Pvt. Ltd. since 2006. With Overall 16+ years of Industry experience, he has expertise and interests in the areas of Design For Manufacturing, Physical Verification, Parasitic Extraction and Rule Deck Development for DRC/LVS. He has vast experience as a Sr. Principal Application Engineer focusing on Cadence Physical Verification tool suite, its customers and loves to teach and guide new engineers with Physical Verification Rule writing methodologies. He is a handy trainer and Customer Support professional, currently creating Knowledge artifacts for Cadence DFM/Physical Verification products.

Supported by

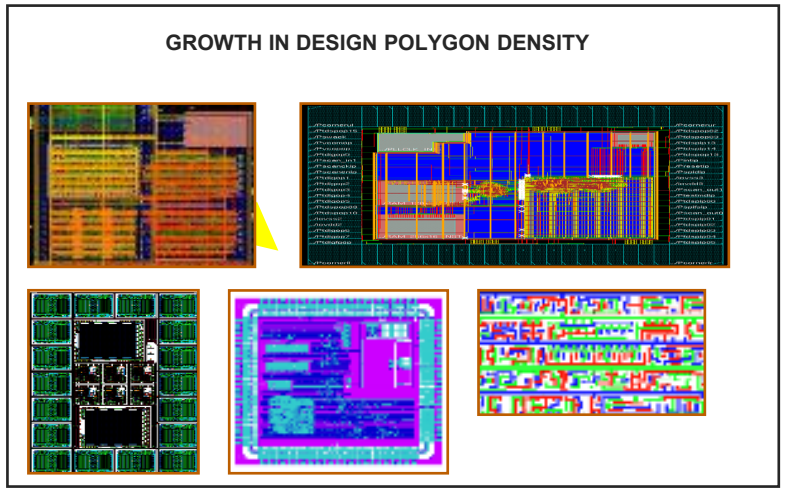
Agenda

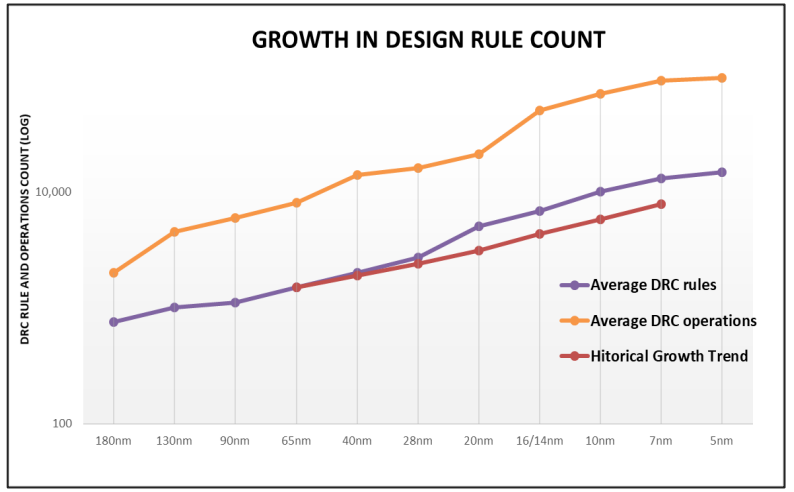
- Typical Physical Verification Flow
- Traditional Physical Verification Challenges
- Next-Gen EDA:
  - Pegasus in the Cloud
  - Large amount of design data, increasing rule complexity, large number of CPUs available – efficient, elastic utilization
  - Massive scalability
  - Accuracy readiness =~ Foundry Qualification
- Integration with implementation tools
  - Innovus/Pegasus In-Design Signoff
  - HMF, Smartverify DRC and LVS, PGFill/TBF
- Advanced node challenges and solutions
  - Early design phase, adv design complexities, power, performance area, ECO, and design closure
- Virtuoso/Pegasus In-design signoff
  - Interactive DRC, Metal Fill, Density Analysis
- Quantus Parasitic Extraction

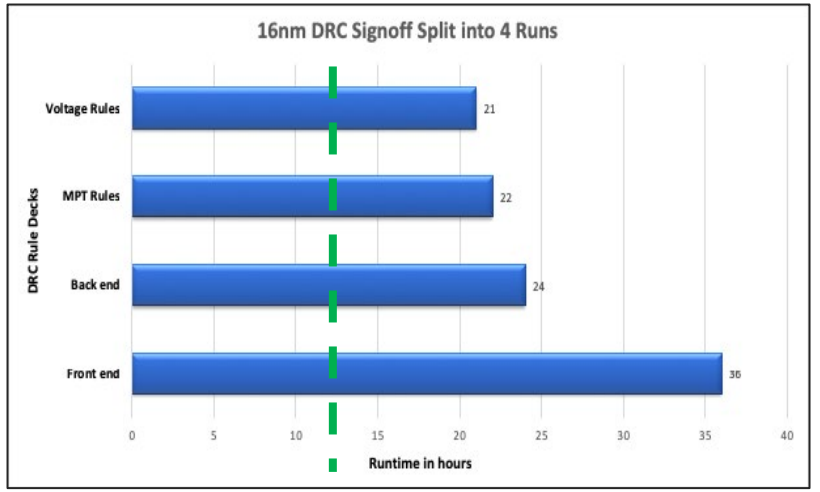
Steps in Physical Verification



Traditional Physical Verification Challenges







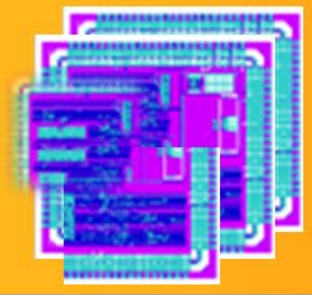
Growing design complexity

Growing number of rules

Overnight runs more difficult

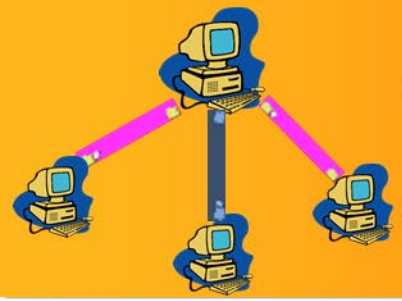
Late design stage iterations to fix violations are long and expensive, and can impact project TTM

Performance: Challenges with Current Tools



Data is split into large partitions, or kept as full-chip for complex rules

→ Long Poles in Distributed Processing



Master bottlenecks communication between workers and stores intermediate results

→ Poor CPU Utilization / Long I/O time

Few Large Machines

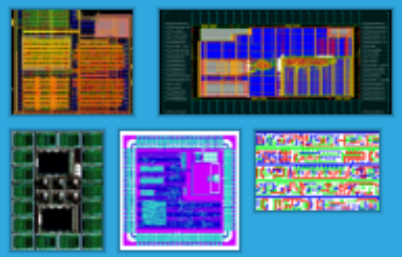
Parallel processing limited to Rules / Operation Groups

→ Poor Scalability Across Machines

What can be moved to cloud, will be moved to cloud

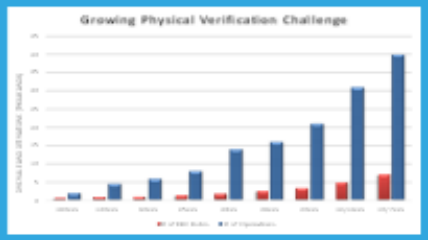
Introducing Pegasus Verification System

Large Amount of Design Data



Pegasus™ Verification System

Increasing Rule Complexity



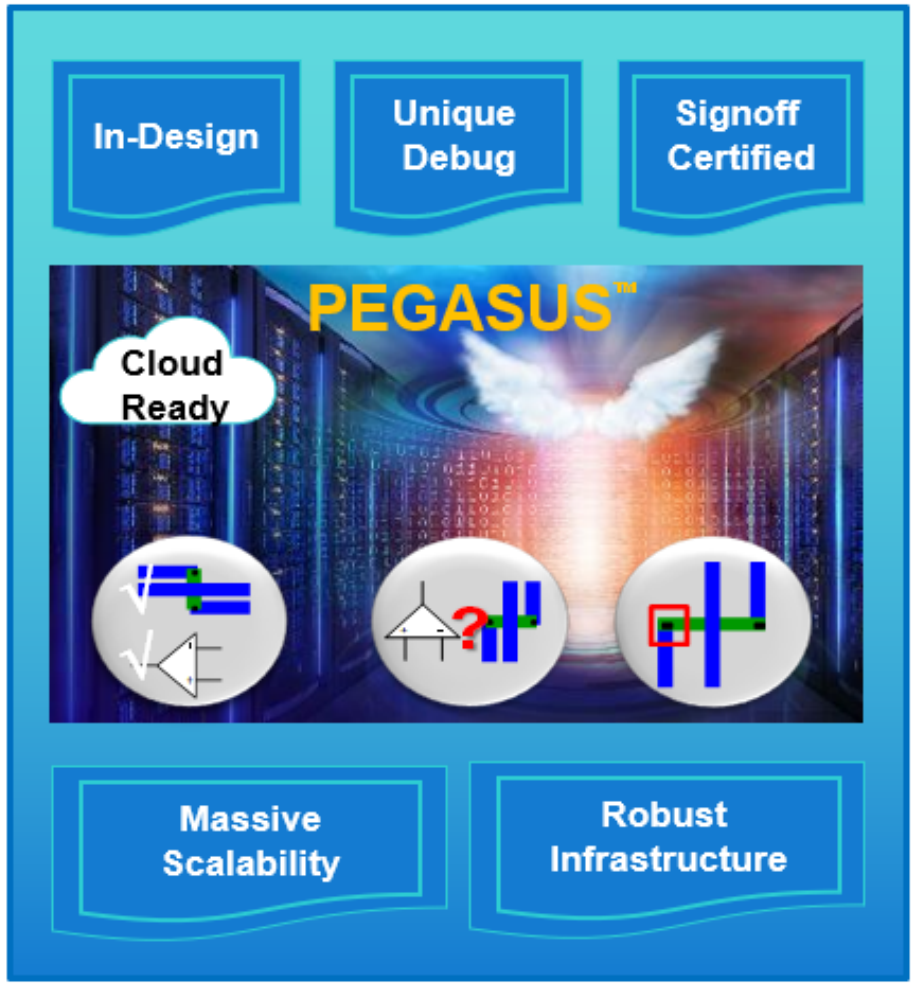
Large Number of CPUs Available

Compute Farm

Efficient, Elastic Utilization

Pegasus: Full-Chip TAT in 1 Day or Less

Massively scalable physical in-design and signoff platform



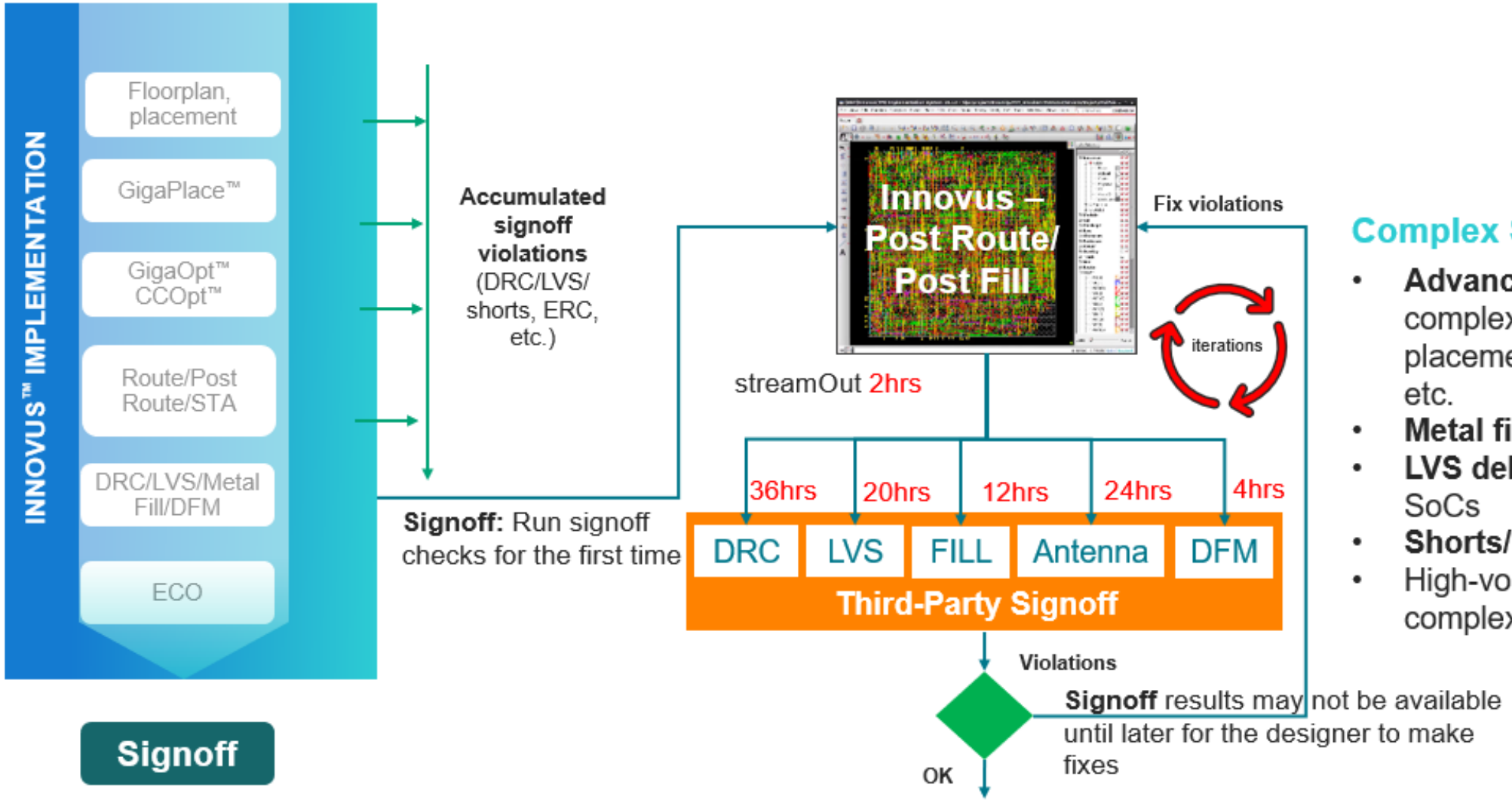
- Accuracy Readiness Through Foundry Certification
- Overnight Runtimes with Massive Scalability
- Integration with Best-In-Class Implementation Tools
- Cloud-Ready with Cost-Effective Hybrid Solutions

Innovus/Pegasus In-Design Signoff

Integrated Signoff Closure

Typical Innovus + Third-Party Signoff DRC/LVS/Fill/DFM Flow

Signoff checks are run late in the design flow

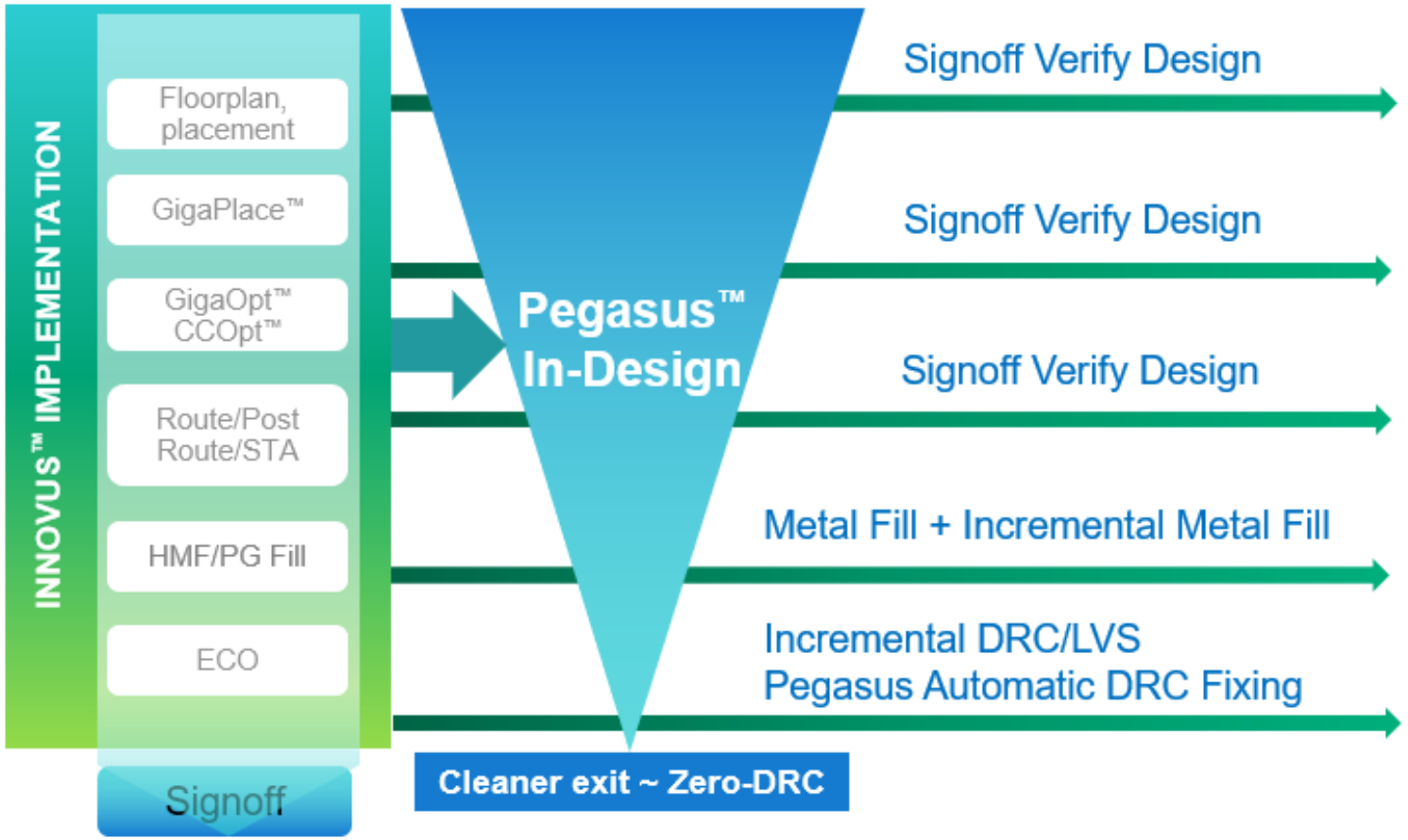


Complex Signoff Checks:

- **Advanced-node** process complexities impact placement, routing, coloring, etc.
- **Metal fill** impact on timing
- **LVS debug** issue on large SoCs
- **Shorts/opens debug** delay
- High-voltage, ERC rule complexities

Zero-DRC from Innovus with Pegasus In-Design Verification

Pegasus: Massively scalable physical in-design and foundry-certified signoff



- Early Floorplan checks, Placement checks, Pre-routed Net DRC
- Lightweight and configurable DRC for gross DRCs
- Signoff DRC Checking
- Fast and interactive short/open checks
- Timing aware Foundry Metal Fill, IR aware PG Fill for IR Critical Blocks
- Incremental, Area based DRC checks and Auto-fixing of signoff DRC viols

Pegasus In-Design Enables 10X+ Productivity Improvement w/ Innovus

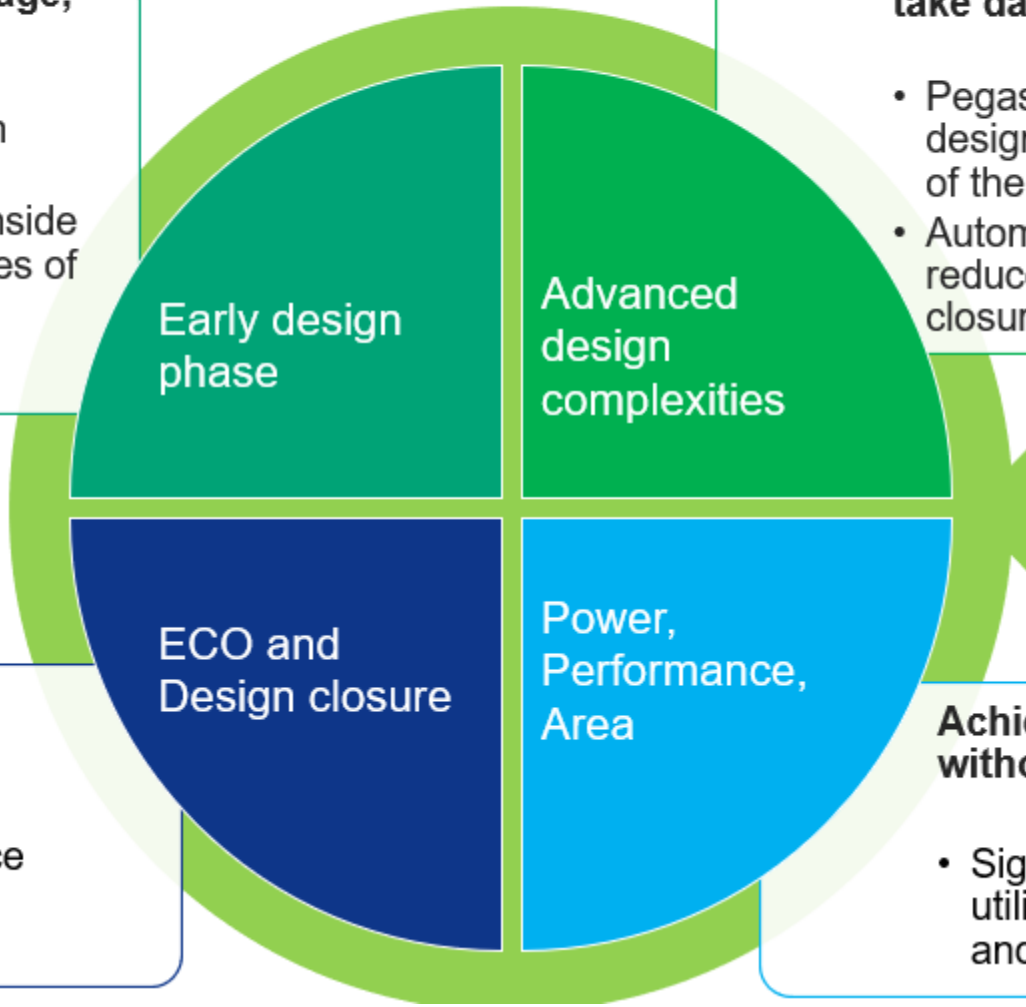
Advanced Node Challenges and Solutions

DRC turnaround-time on early-stage, dirty designs

- Pegasus™ Signoff Verify DRC can identify gross layout issues
- Pegasus Signoff DRC checking inside Innovus™ adapts to different stages of design flow for faster TAT

Full Signoff DRC/LVS could potentially take days to run/debug/fix

- Pegasus Signoff Verify LVS can identify design connectivity issues at any stage of the design cycle
- Automated Signoff DRC Fixing (Beta) reduce manual fixing at last-mile closure



Pegasus integrated within Innovus ensures predictable design closure

Time-to-Market

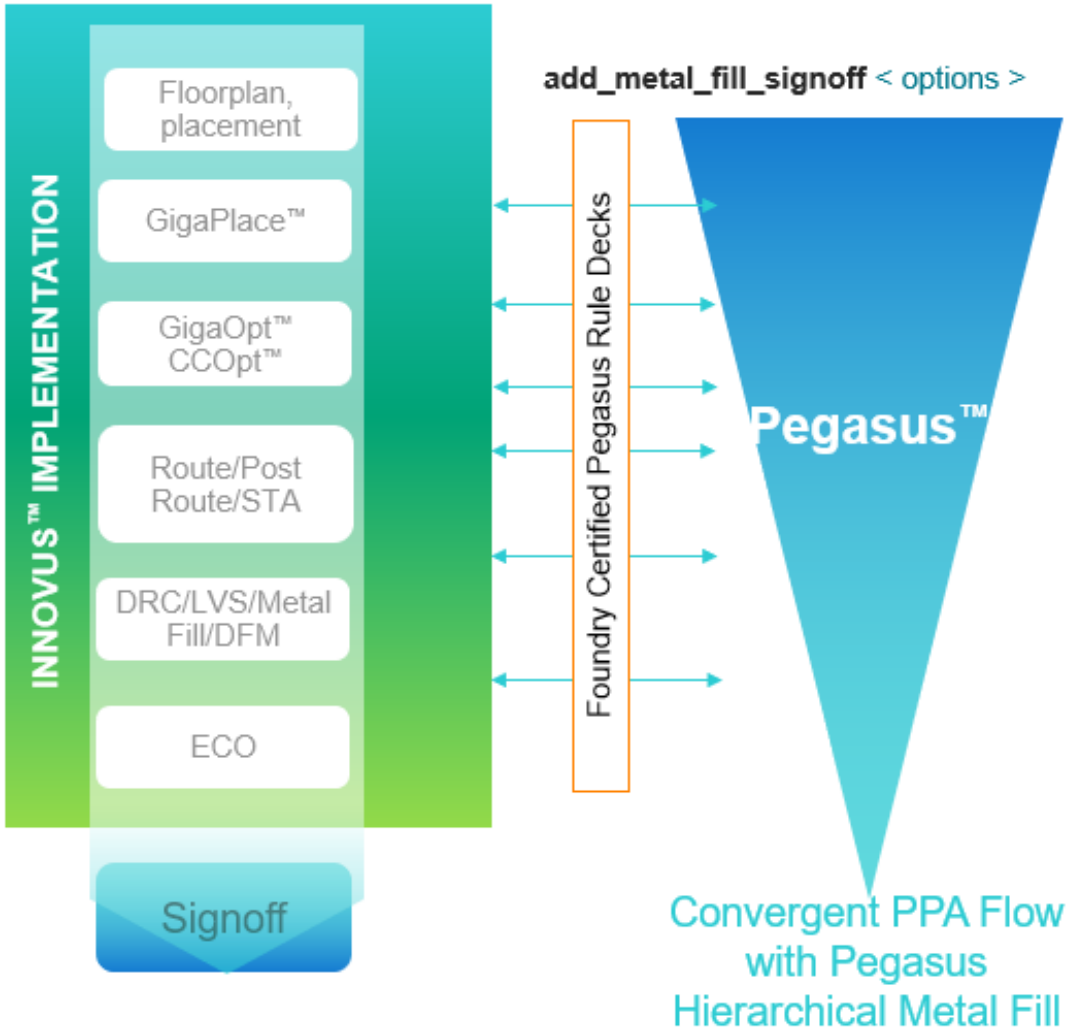
- Window-based and Incremental flows DRC, LVS, and FILL reduce TAT without compromising timing/power

Achieve clean physical verification without compromising PPA

- Signoff DRC, Fill, PG-Fill and multiple utilities are integrated with Innovus and Tempus to address PPA integrity

Innovus/Pegasus Signoff Fill Flow

Timing-aware flow



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Foundry Certified Pegasus Rule Decks

Pegasus™

Convergent PPA Flow with Pegasus Hierarchical Metal Fill

Massively Scalable Signoff Pegasus

Signoff Fill

Hierarchical Fill DB in Innovus

Timing-Aware Fill

Automated Timing-Aware flow

Incremental Fill

50% to 80% ECO fill runtime reduction

Window-Based Fill

10X-100X Faster Targeted DRC fixes

Pegasus Metal Fill

Timing preserved with timing-aware

			Baseline	postFill	Timing Aware Fill
POST-ROUTE	REG2REG	WNS	-0.114	-0.119	-0.116
		TNS	-201.422	-249.1	-210.402
		FEP	[illegible]	[illegible]	[illegible]
	REG2ICG	WNS	-0.089	-0.093	-0.09
		TNS	-12.939	-16.289	-13.776
		FEP	1091	1536	1220
	REG2MEM	WNS	-0.114	-0.117	-0.115
		TNS	-37.311	-432.233	-38.036
		FEP	1593	2133	1668
	MEM2REG	WNS	-0.131	-0.129	-0.129
		TNS	-52.356	-59.175	-55.4
		FEP	2343	2878	2604
	MEM2MEM	WNS	-0.103	-0.103	-0.101
		TNS	-2.457	-2.502	-2.463
		FEP	32	32	32

Design	Full Signoff	Window based DRC fix in HMF
Chip D (70GB gds.gzip)	18 hours	**22mins**
Chip M (20GB gds.gzip)	5 hours	**3 mins**

Virtuoso/Pegasus In-Design Signoff

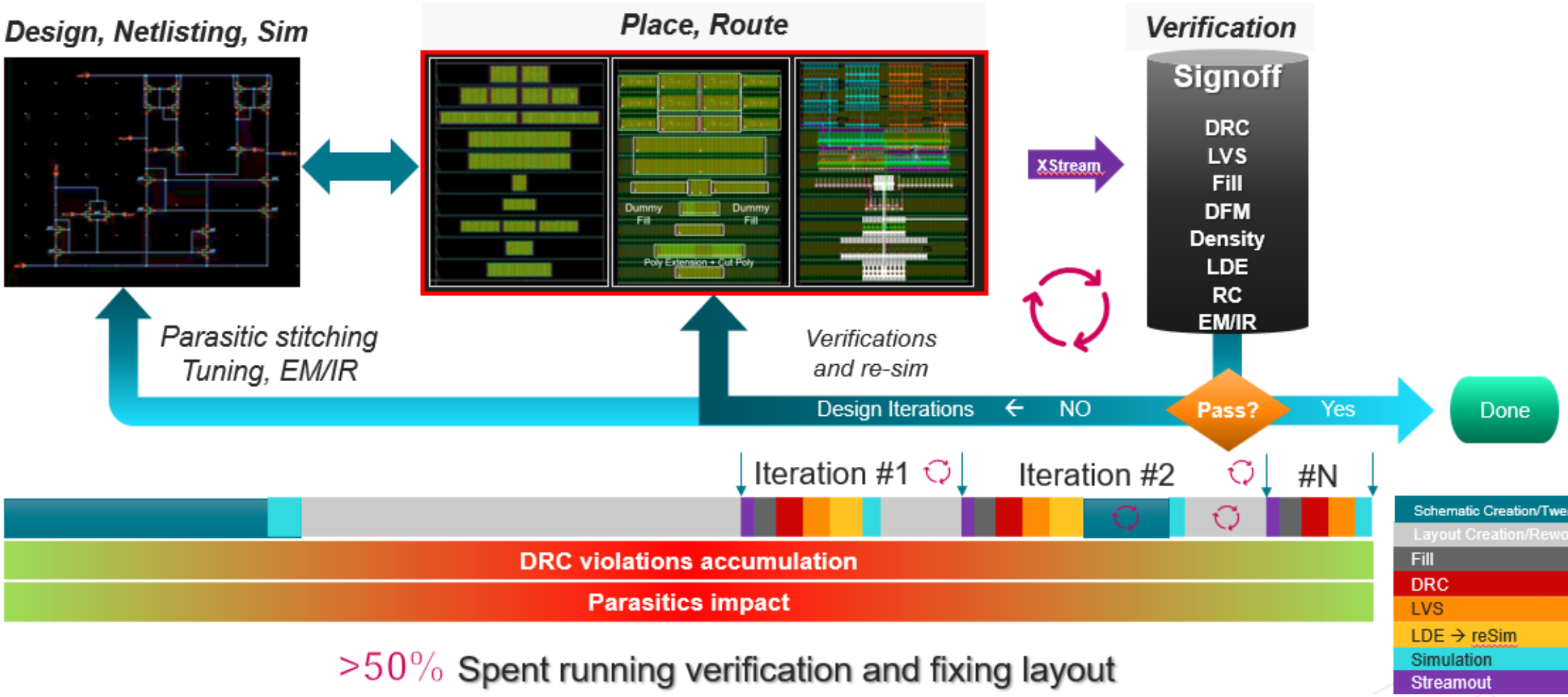
Integrated Signoff Closure

Advanced Methodologies Flow and Challenges

The importance of in-design verification at the layout development step

Iterative

$ Expensive



>50% Spent running verification and fixing layout

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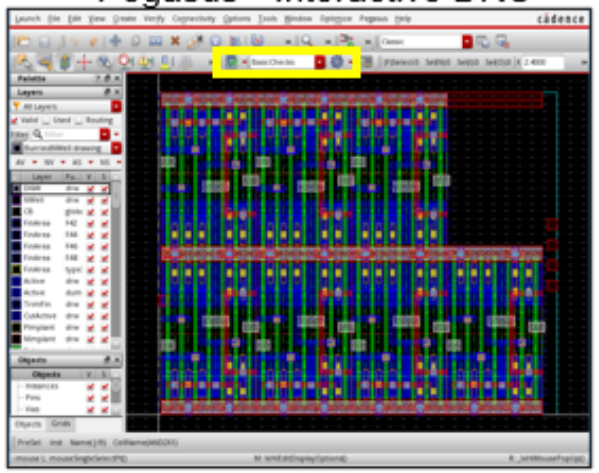
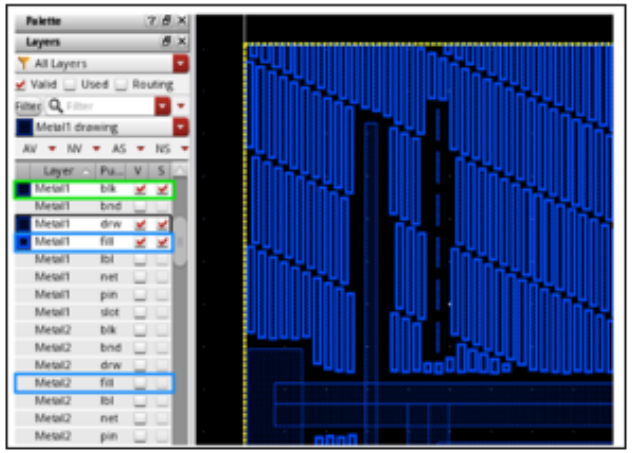
Virtuoso/Pegasus Interactive DRC, Metal Fill, Density Analysis

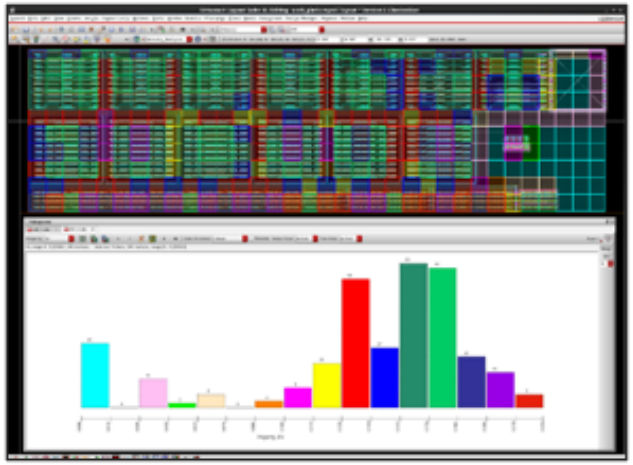
Pegasus™ Interactive DRC



Pegasus Interactive Signoff Fill



Pegasus Interactive Density Analysis



Enabling Higher Quality Layout, Faster

Quantus Extraction Solution

RLCK Extraction You Trust!

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Types of Extraction

- Quantus™ cell-level extraction option
  - Inputs
    - Design: DEF, cell library: LEF/GDSII/OA
  - Outputs
    - DSPF, SPEF, VolgageStorm, SignalStorm
  - Cell-level static IR drop/static timing and/or signal integrity analysis

- Quantus device-level extraction option
  - Inputs
    - Assura LVS, PVS-LVS, GDSII, Calibre-LVS data.
  - Outputs
    - SPICE, Spectre, SPEF, Tx-SPEF, DSPF, xDSPF. Extracted_view
  - Transistor-level /IR drop and static timing verification

Cadence Flow Advantages

- Quantus™
  - Supports Calibre LVS
  - Single extraction engine capable of generating all the signal and power net parasitics to support VoltusFi-XL EM-IR flow
  - Tight integration with Voltus-Xfi XL to support EMIR, S.H.E, and reliability flows.
  - Tight integration with Virtuoso and provides additional GUI, customized to support TSMC nodes, to generate Voltus-Fi compatible dspf file

- Voltus™-XFi XL
  - No need to write extra mapping files when using Quantus extraction
  - Voltus-FI XL tech file uses similar language as Quantus ICT tech files
  - Quantus extraction data can be directly used to analyze Voltus-Fi generated EM and IR heatmaps
  - Supports PGV flow