Custom IC Design Platform

Sameer Garg

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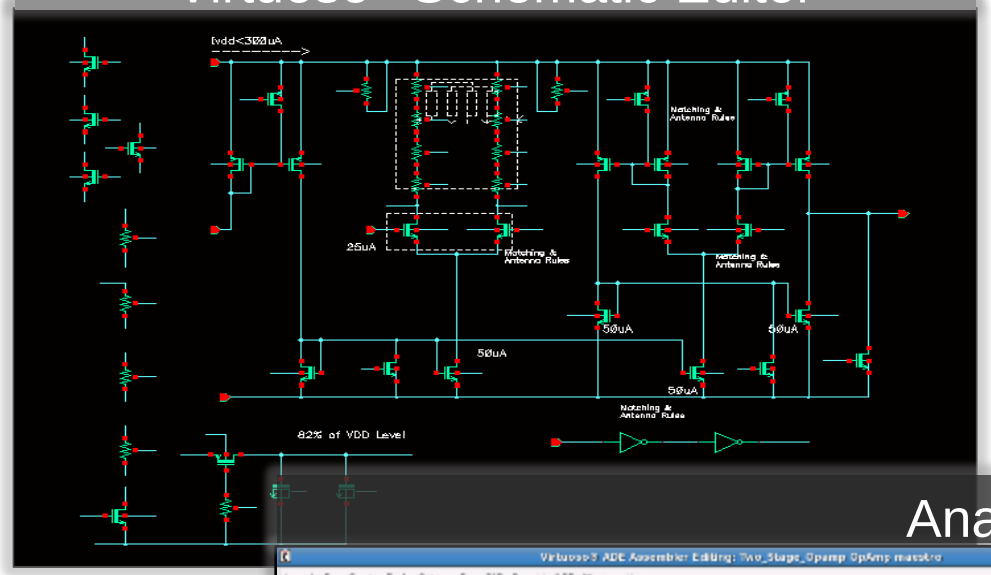
cadence®

Agenda

- Custom IC Design Platform
- Mixed-Signal Implementation flows
- Custom IC Design Flow/Tools
- Layout Automation: Advanced Methodologies
  - Concurrent Layout Editing (CLE)
  - Simulation-Driven Routing (SDR)
  - Design Planning and Analysis (DPA)

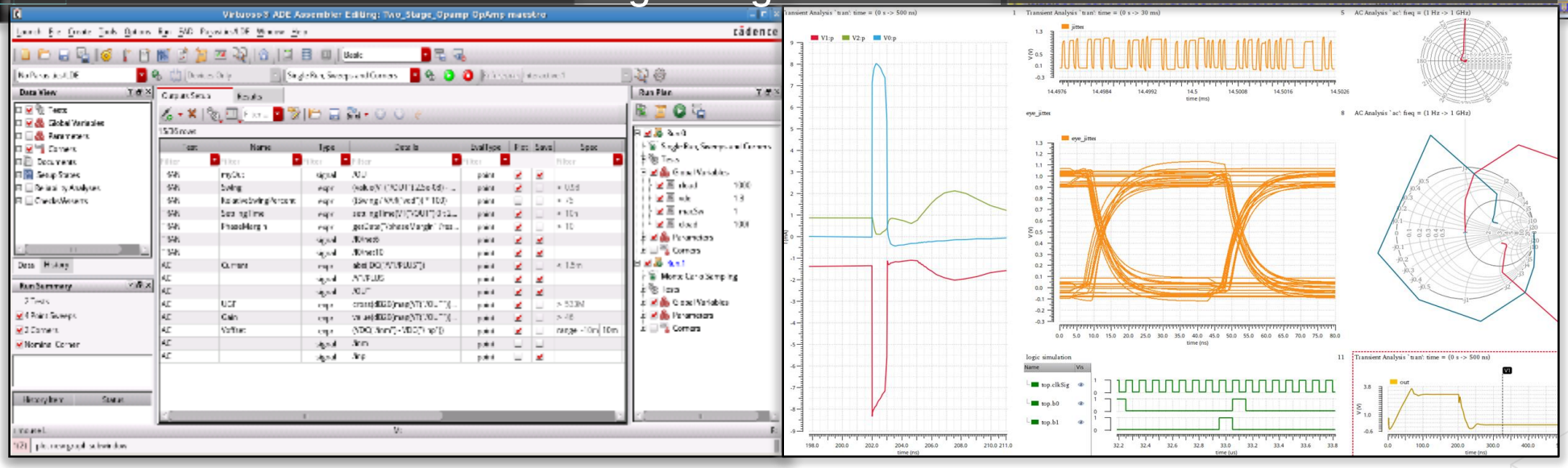
Custom IC Design Platform

Virtuoso® Schematic Editor



Virtuoso Layout Editor

Analog Design Environment



Mixed-Signal Implementation Flows

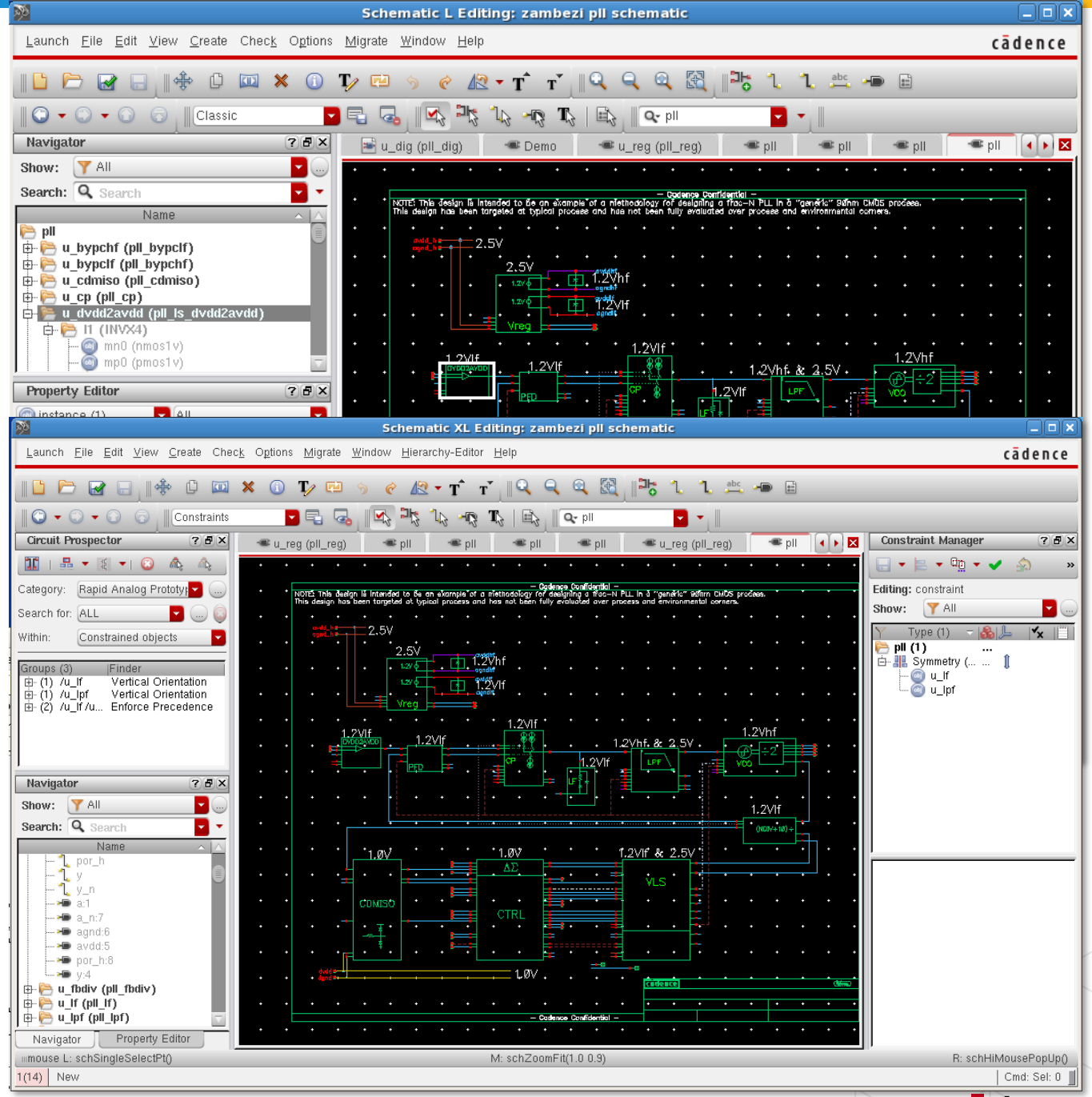
Methodology	Schematic-driven		Netlist-driven	
	Analog/Custom	Analog on Top (AoT)	MSoT	Digital on Top (DoT)
Design	Analog; might have very small number of standard cells placed and routed without digital P&R tools	Top-level is analog; standard cell digital contained inside block designed using digital flow.	Analog and standard cell digital mixed at the same level.	Predominantly digital design with analog integrated as hard macro
Top level connectivity	Schematic	Schematic	Verilog	Verilog
Floorplanning	Virtuoso	Virtuoso & Innovus	Virtuoso & Innovus	Innovus & Virtuoso
Analog content	Main/Top	Main/Top	Co-designed	Black-boxed
Digital content	Custom digital	Black-boxed	Co-designed	Main/Top
Routing	All routing done by the Virtuoso space-based router	Top level and analog block by VSR; routing within digital block by NR	Analog block by VSR; Digital block by NR; Top: analog by VSR, standard cell by NR	Top-level analog by VSR. All other routing by NR.
Chip Integration	Virtuoso	Virtuoso	Innovus	Innovus
Signoff	SPICE Simulation	Static Timing Analysis & Simulation	Static Timing Analysis	Static Timing Analysis
Chip Finishing	Virtuoso	Virtuoso	Virtuoso	Virtuoso/Innovus

Analog: Virtuoso Space-based Router(VSR) Digital: NanoRoute(NR)

Custom IC Design Flow/Tools

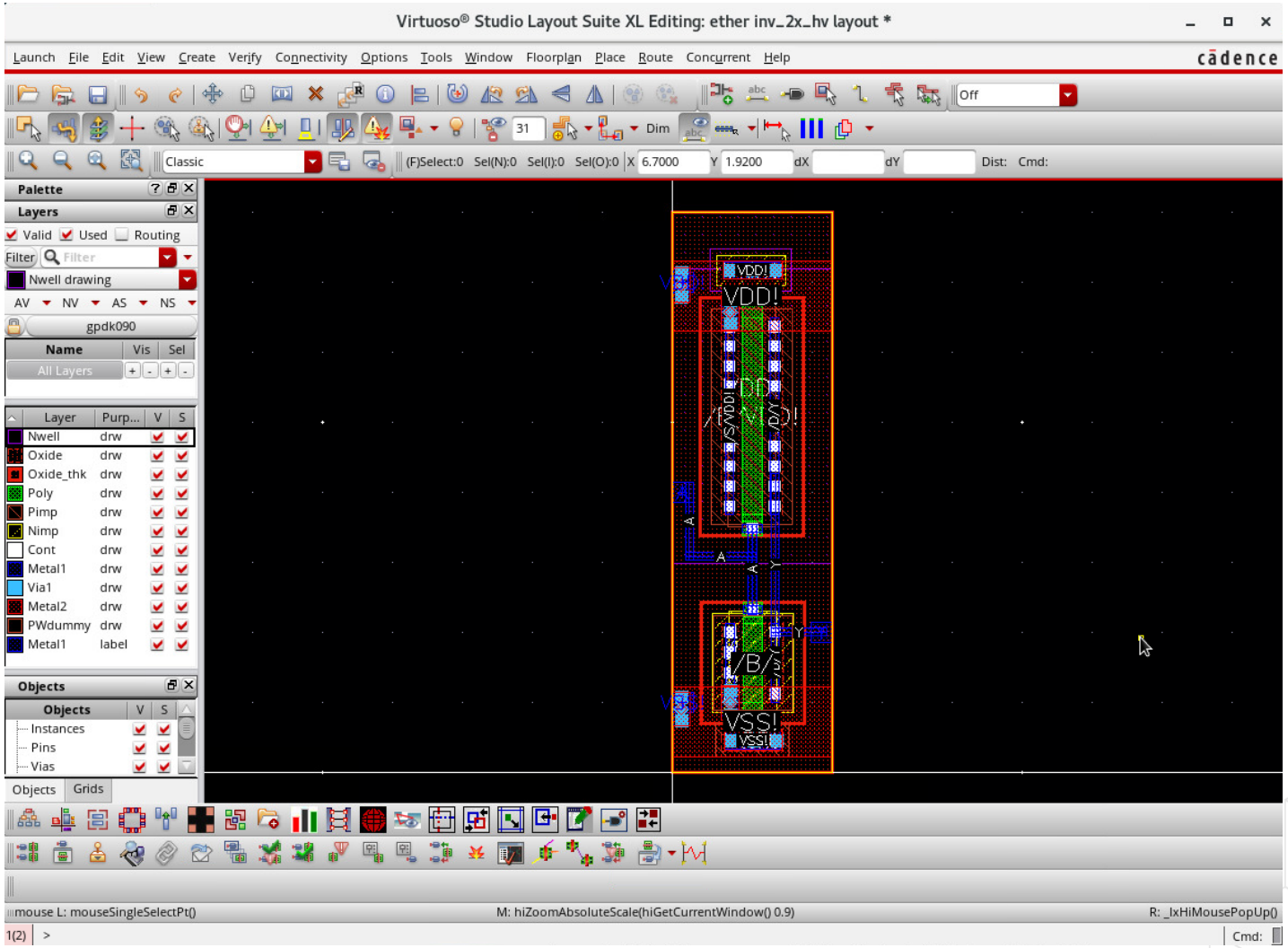
Schematics

- Is a *circuit diagram*
- Is a logical view of the design
- Depicts logical connectivity
- Both top-down and bottom-up styles are possible
- Heavily used by analog/MS designers
- Netlister converts schematic data to text input for simulators



Layouts

- Is a physical representation of the design
- Can be a bottom-up or a top-down design process
- Contain logical connectivity
- Netlisters are used to convert extracted data to text input understood by a simulator (Post-Layout Simulation)



Layout Automation: Advanced Methodologies

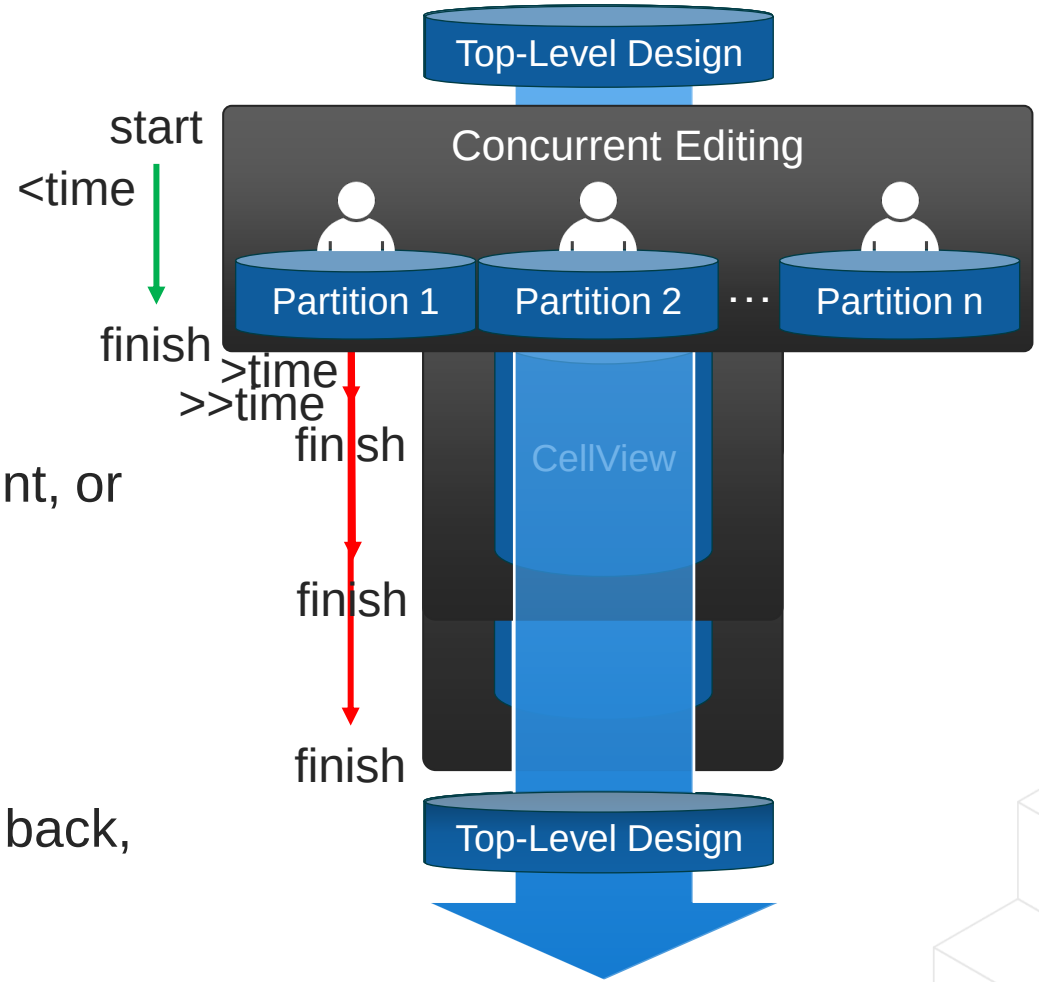
Advanced methodologies for mature and advanced process nodes

- Concurrent Layout Editing
- Simulation-Driven Routing
- Design Planning and Analysis

Concurrent Layout Editing (CLE)

Advanced methodologies for mature and advanced nodes

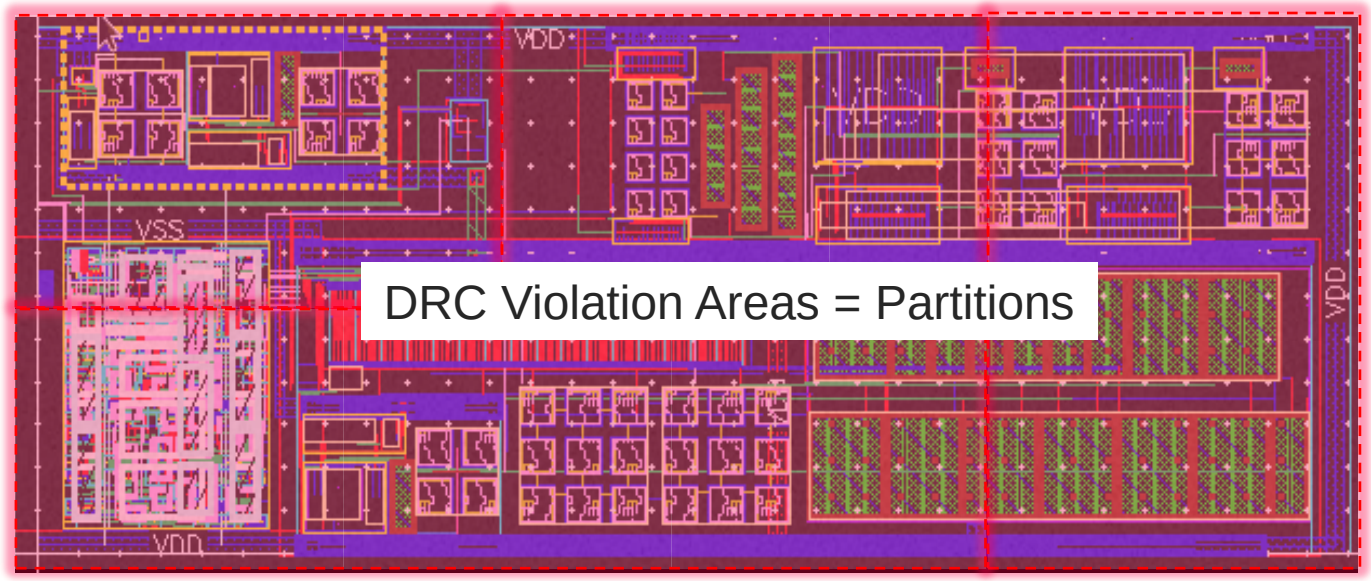
- What problem does it solve? Who needs it?
- Whenever “1 person / 1 task” is a bottleneck
  - Top-level chip finishing/DRC cleaning
  - Top-level assembly routing
- What causes that problem?
  - Unix permissions restrict editing a single file, document, or design database to only one user at a time
- Why can't you just add hierarchical partitions?
  - Top-level chip finishing/DRC cleaning and top-level assembly routing are the last tasks of verification and assembly, and it is difficult and time-consuming to go back, re-partition, and restart
- Concurrent layout enables team design at late stages without changing the original design hierarchy

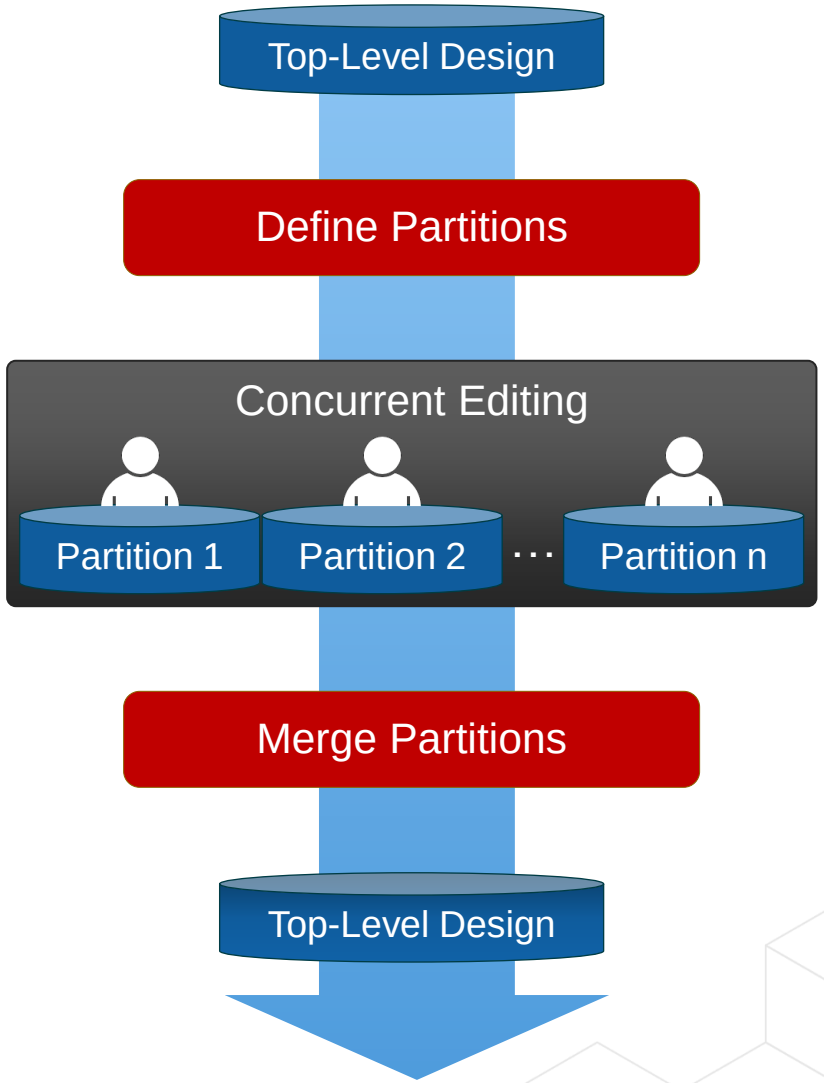


Concurrent Layout Editing (CLE)

Advanced methodologies for mature and advanced nodes

- What is it?
  - Multiple users concurrently edit a single top-level design, in a non-destructive mode, within the context of the entire top-level
  - Design lead partitions top-level, reviews and approves edits, and merges edits from partitions back into top-level design

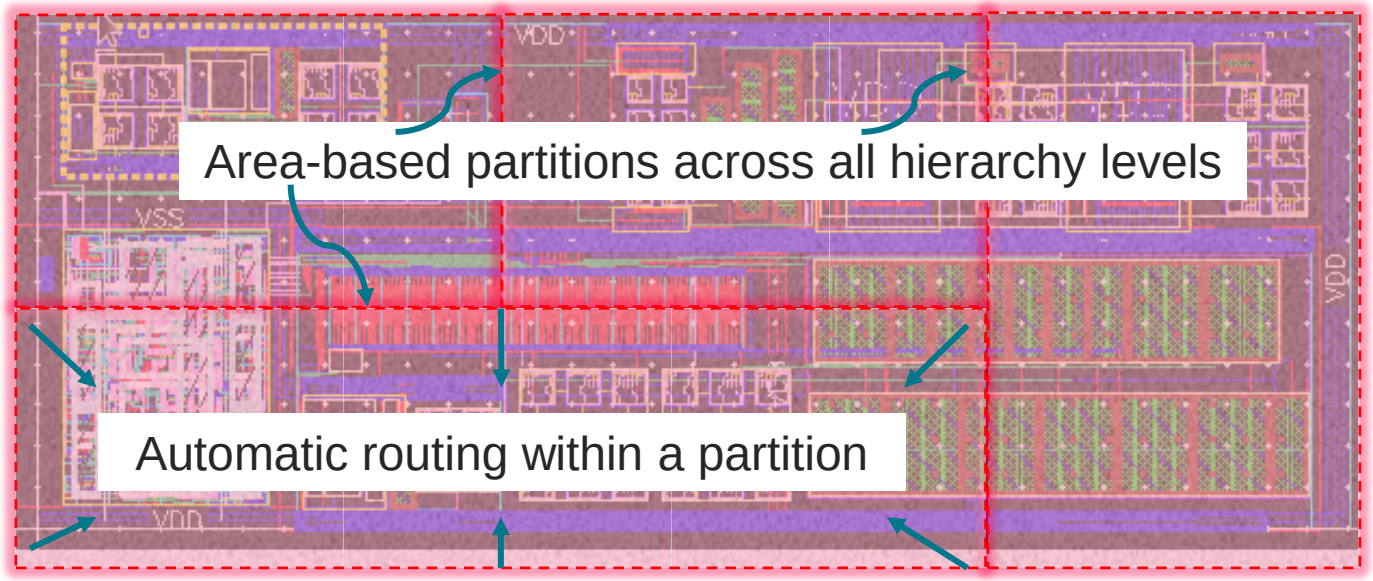


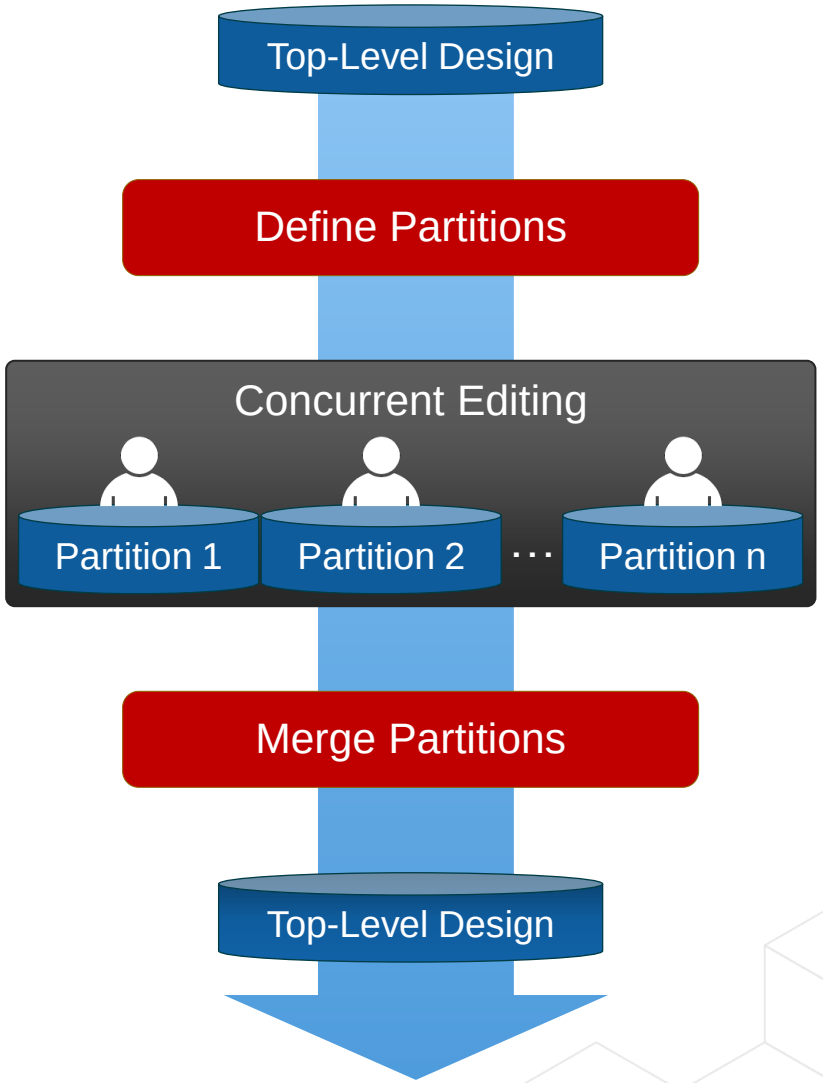


Concurrent Layout Editing (CLE)

Advanced methodologies for mature and advanced nodes

- What's New?
  - Layer-based partitioning
    - L1-L4 parition1:User1, L5-8 partition2:User2, L9-12 partition3:User3 ...
  - Area-based partitioning across all hierarchy levels
  - Partition-based Automatic Routing





Simulation-Driven Routing (SDR)

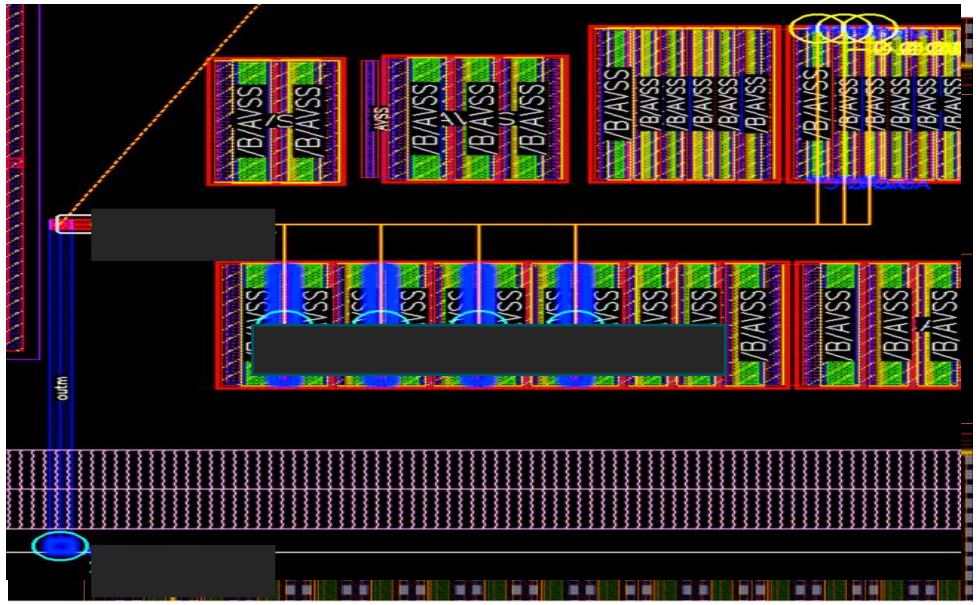
Advanced methodologies for mature and advanced nodes

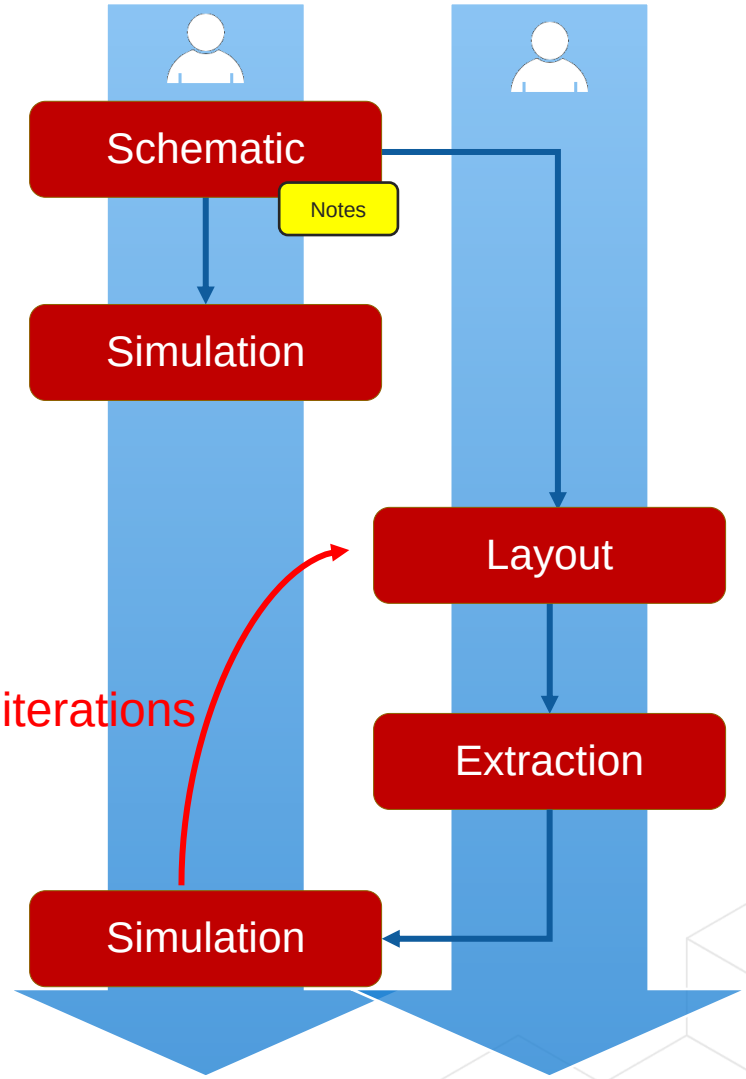
- What problem does it solve? Who needs it?
  - Every analog design and every designer must properly size every wire and every via per electrical specifications
  - In existing flows, “electrical impact” is unknown until the layout is completed, extracted and re-simulated
  - “Check n Fix” flows require many long iterations

Every wire and via must be properly sized to handle specifications:

width = f(i)

via cuts = f(i)

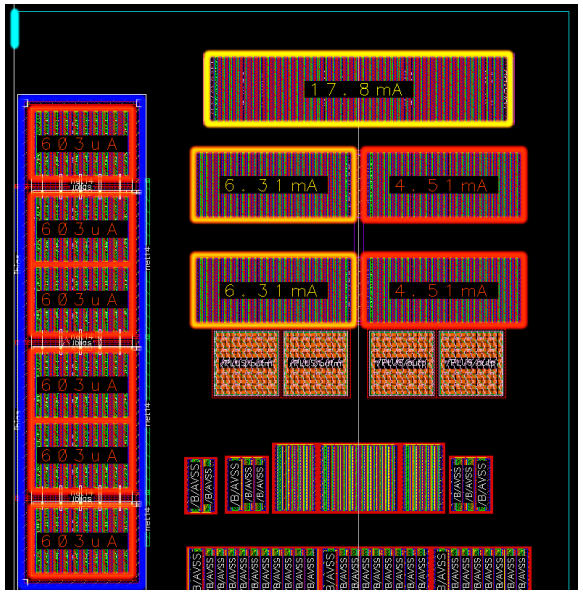


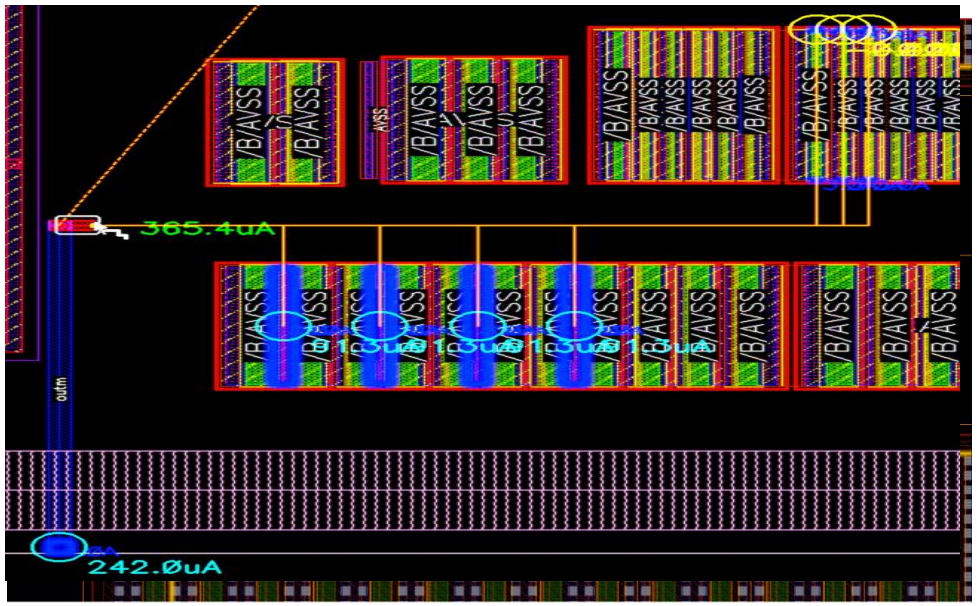


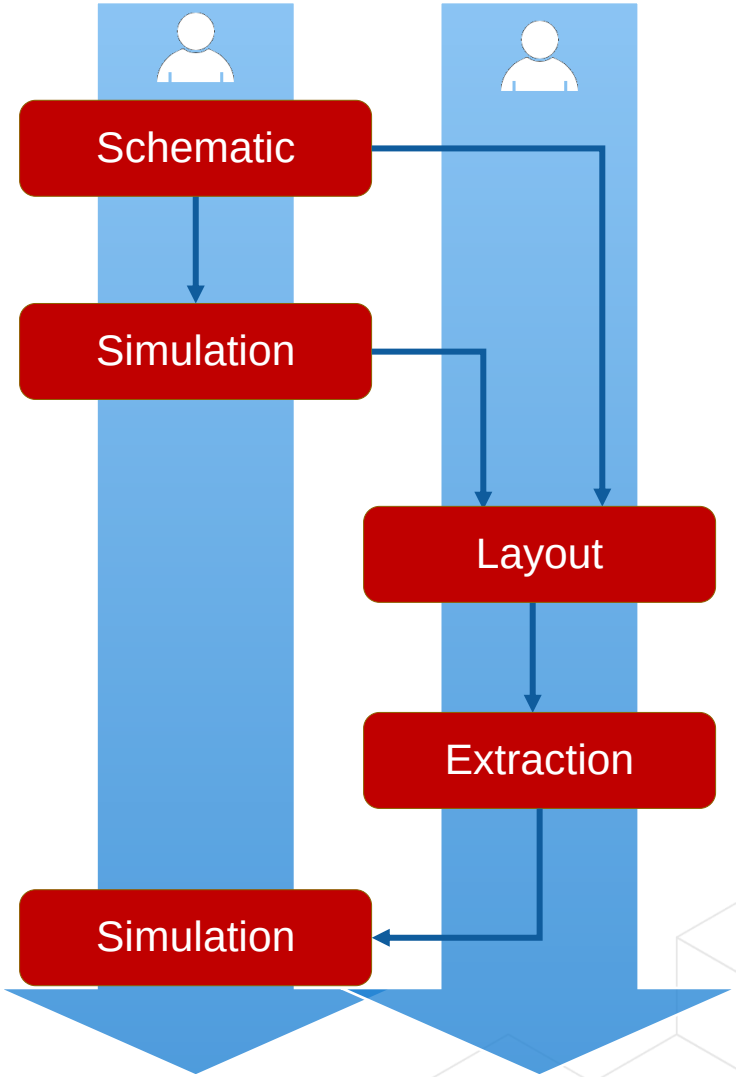
Simulation-Driven Routing (SDR)

Advanced methodologies for mature and advanced nodes

- What is it?
  - Combined schematic-driven and simulation-driven layout
  - Visualize current distribution during device placement
  - Automatically size wires and vias based on current and automatically connect to devices during interactive routing



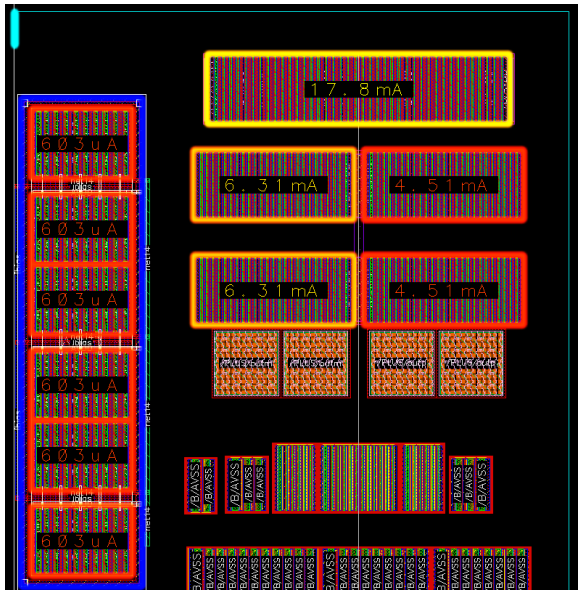


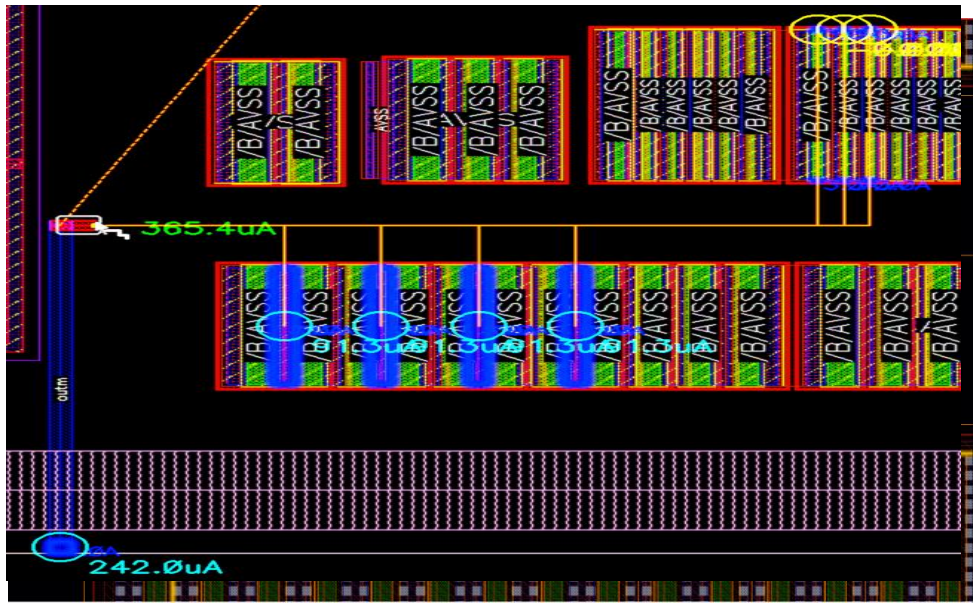


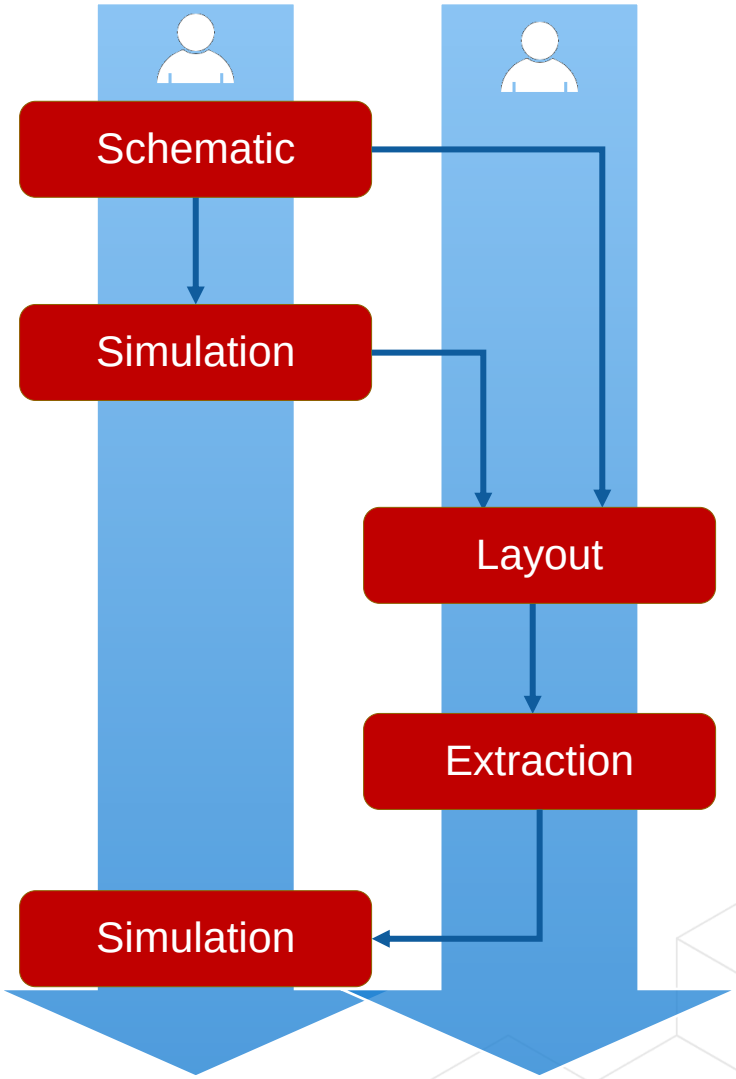
Simulation-Driven Routing (SDR)

Advanced methodologies for mature and advanced nodes

- What is new?
  - WSPs and AdvNode support
  - Design Intent (DI) driven flow, for early layout prior to simulation, or when simulation data is not available
  - Over-the-device routing



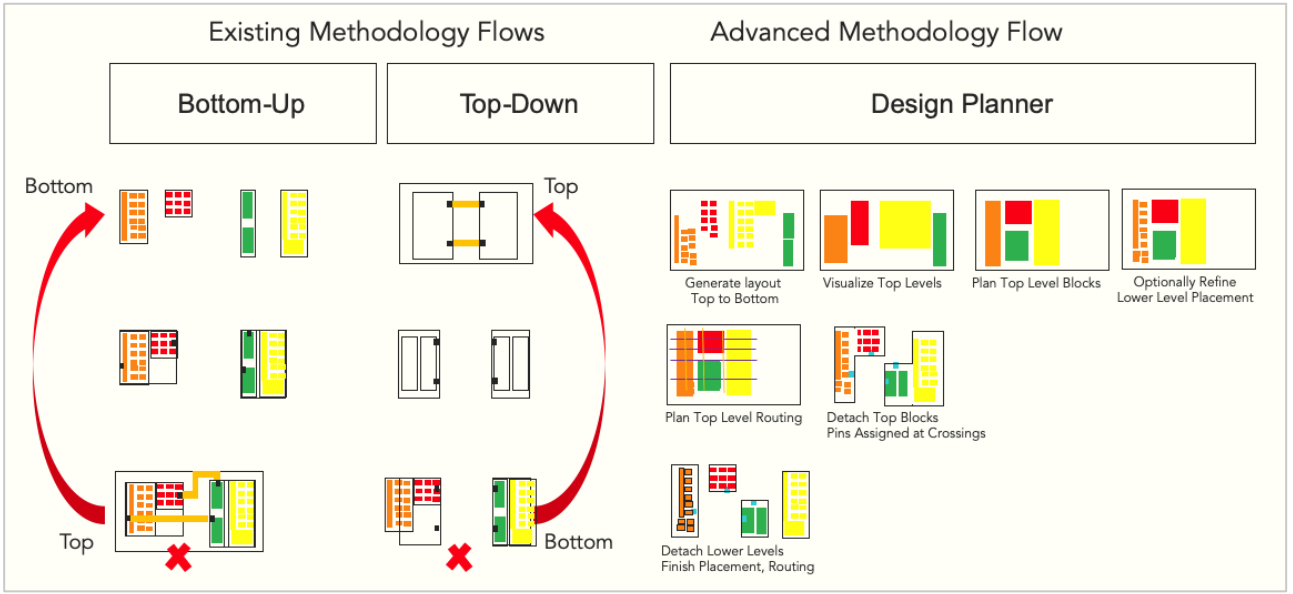




Design Planning and Analysis (DPA)

Advanced methodologies for mature and advanced nodes

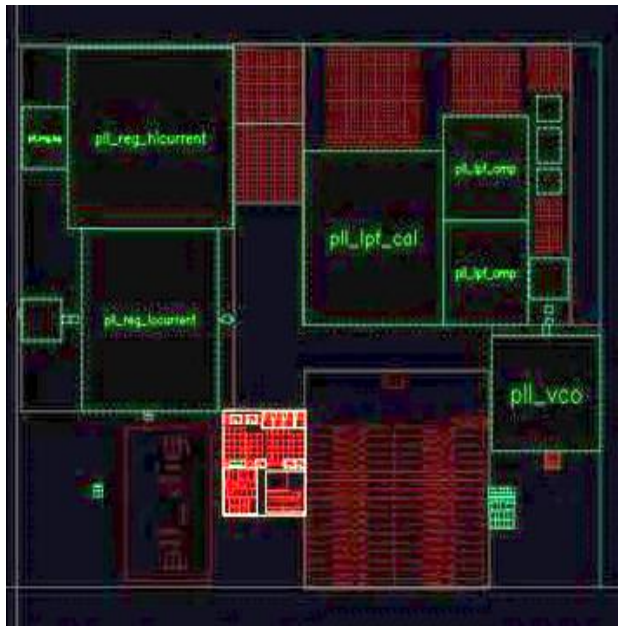
- What problem does it solve? Who needs it?
  - All customers have some variation of two primary hierarchical floorplanning flows:
    - ” Bottom-Up” and “Top-Down”
  - Both lack awareness of the hierarchy above or below, respectively
    - This causes early design decisions to be made with partial and inadequate information
    - Only to encounter unforeseen problems later in the design cycle
    - Only to cause long iteration cycles

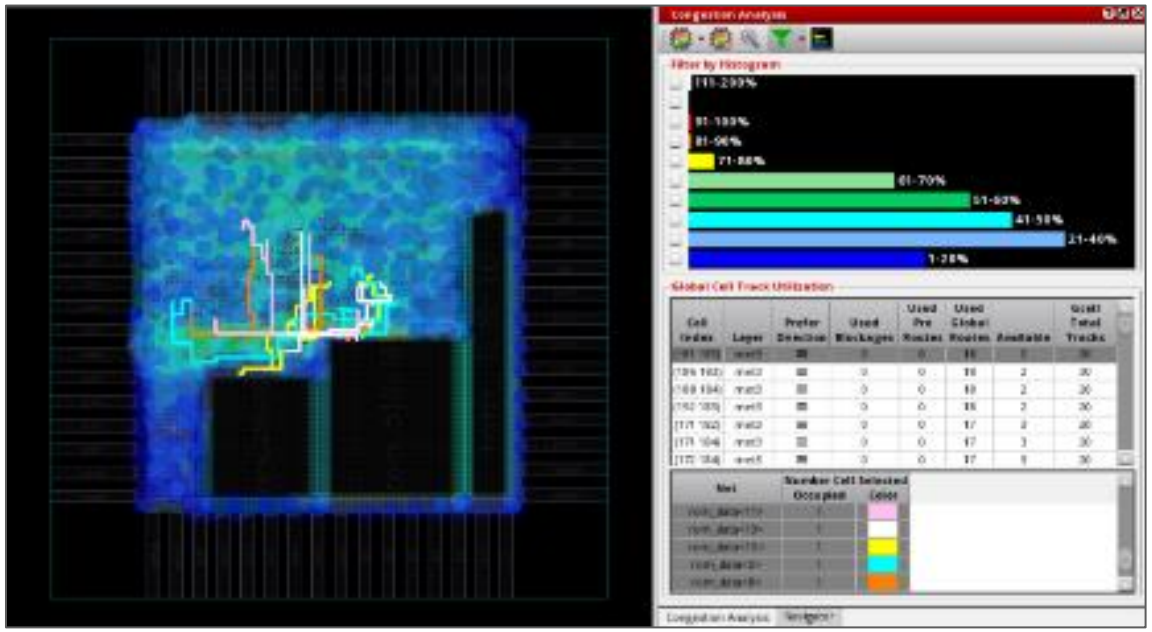


Design Planning and Analysis (DPA)

Advanced methodologies for mature and advanced nodes

- What is it?
  - Novel hierarchical layout generation, and multi-level planning
  - Combines the best of Bottom-up and Top-Down approaches
  - Congestion-aware pin generation, and optimization
  - Global route planning, and congestion analysis



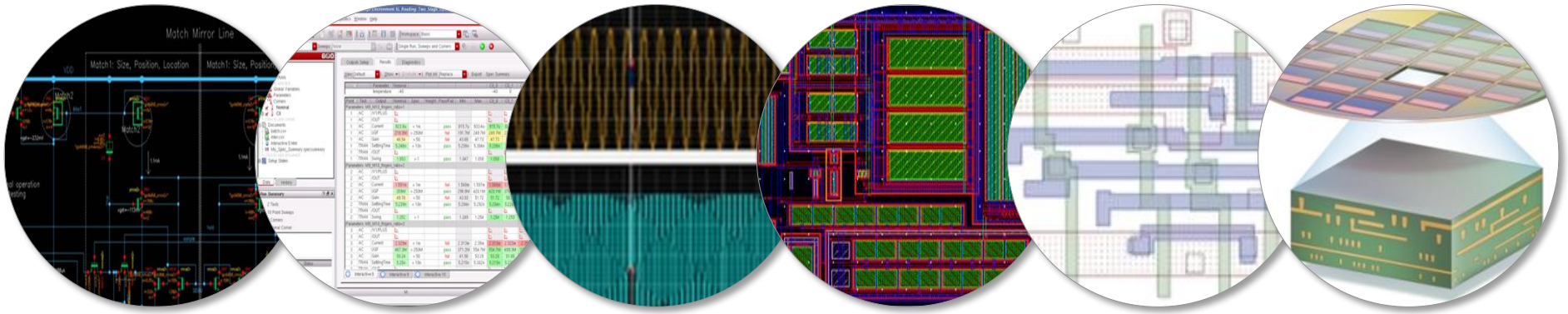


- Generate Hierarchy
- Block Planning
- Route Planning
- Pin Planning
- Placement
- Routing

Offering Overview

Virtuoso integrated custom/analog flow

Virtuoso® custom/analog flow



Measure early and often for first-pass success

- Uniquely integrated tools servicing the entire custom design space
- Custom design, low power, advanced node, RF, mixed-signal
- Approximately 80% MSS for IC Schematic, Layout, and Environment
- Hub for the most extensive technical ecosystem in the industry