Physical Design

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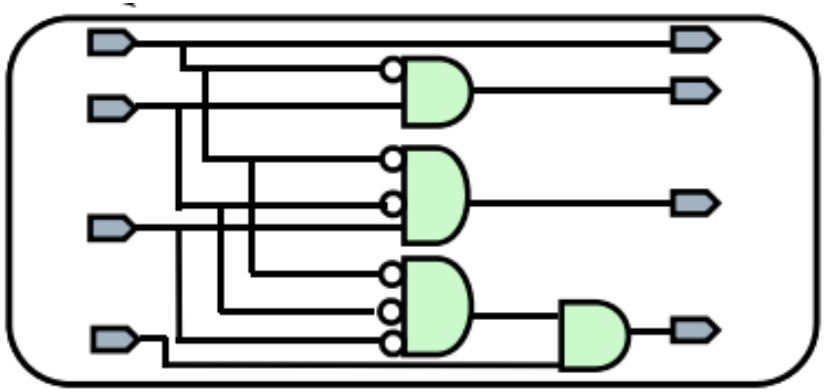
Flow Recap

Synthesis

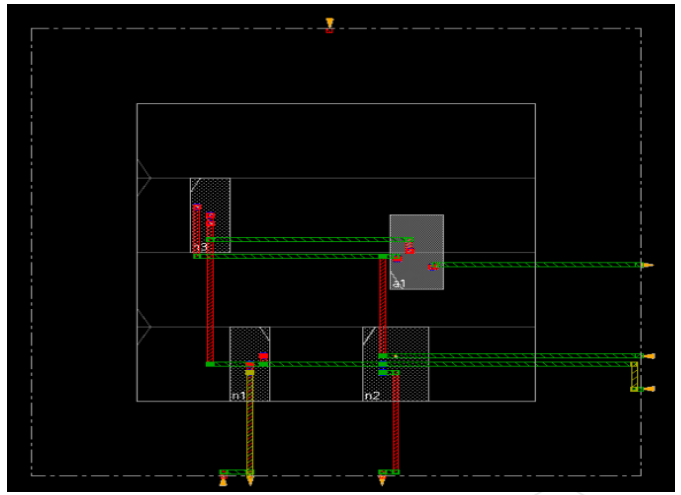
```
if(high_bits == 2'b10)begin
  residue = state_table[i];
end
else begin
 residue = 16'h0000;
end
```

Behavioral HDL

Technology mapped and optimized gate-level netlist



PnR

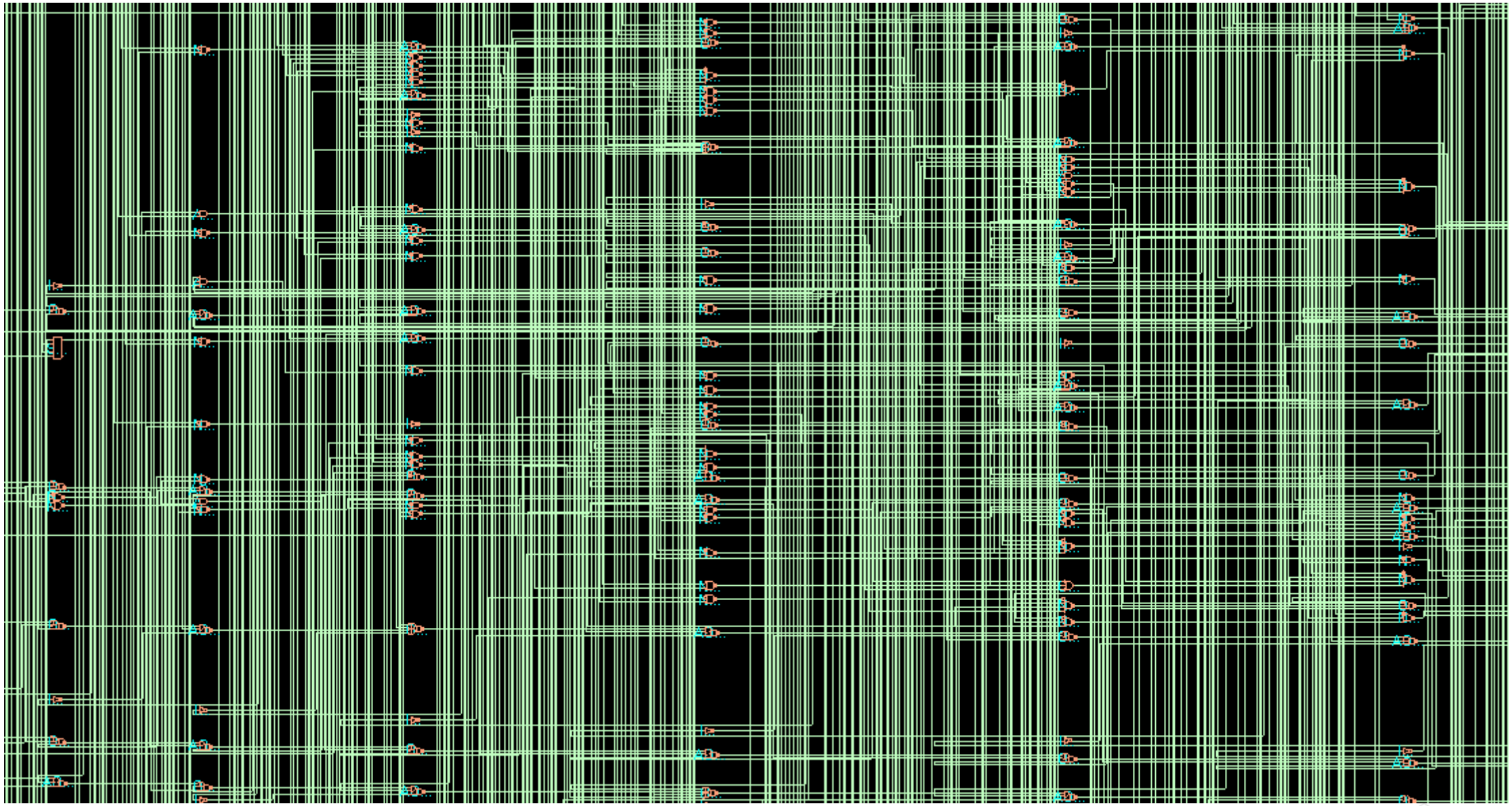


Placed and Routed design

Goal :

- Technology constraints – Ensures chip can be fabricated
- Electrical constraints – Ensures desired electrical behavior of chip

With More Components…



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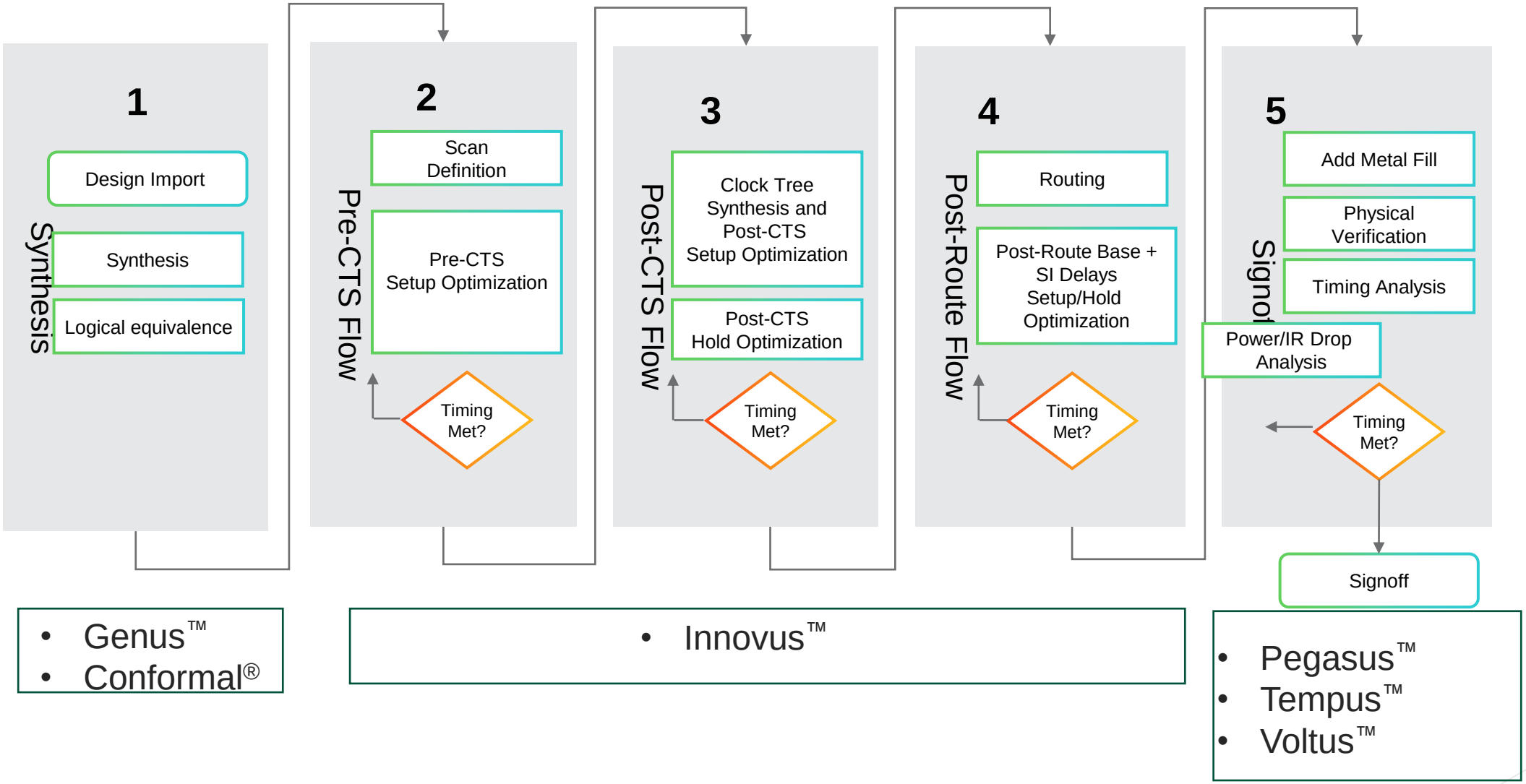
Flowchart: The Digital Implementation Flow



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Steps and EDA Tools

Implementation steps :

- Make changes in the design
- Expectation is to get the best QoR.

Analysis steps :

- Analyze the design at a given step
- Expectation is to be accurate

Implementation Steps
Synthesis and optimization
Floorplan
Placement
Clock Tree Synthesis
Routing
Timing optimization

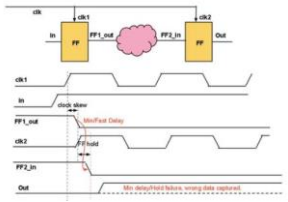
Analysis Steps
Timing Analysis [Signoff]
Power Calculation
IR Drop analysis
Logical Equivalence
Power intent
DRC and LVS

Digital Implementation

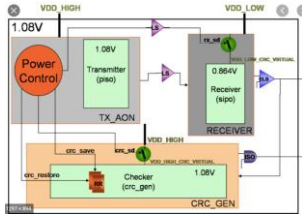
From designers

RTL

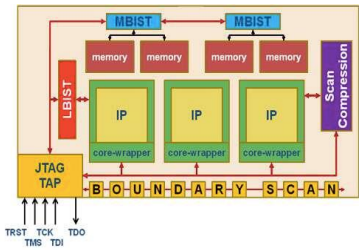
Timing Intent



Power Intent



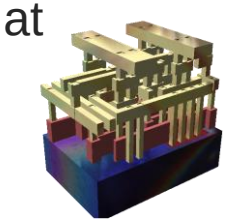
DFT architecture



Design collaterals

From Foundary

Timing, electrical, and physical properties of target technology at which design will be fabricated



Technology collaterals

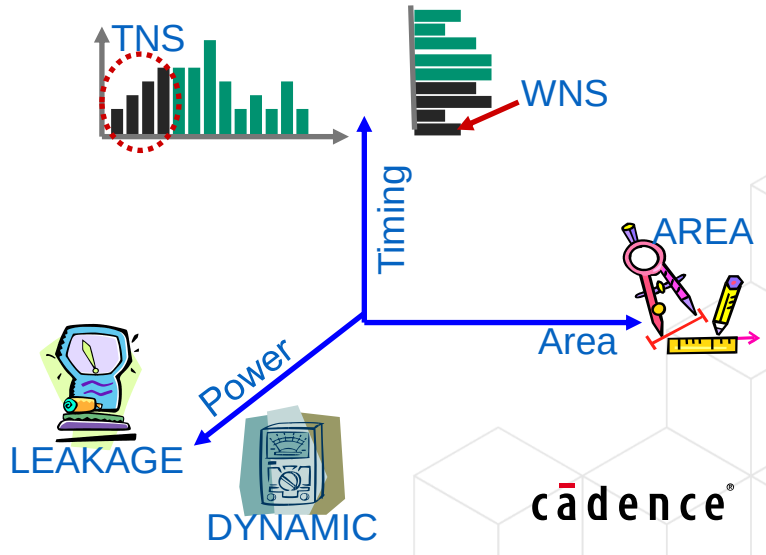
EDA Software

Mathematical representation of design problem

Algorithms to optimize the target variables

Computation power of machines

GDS



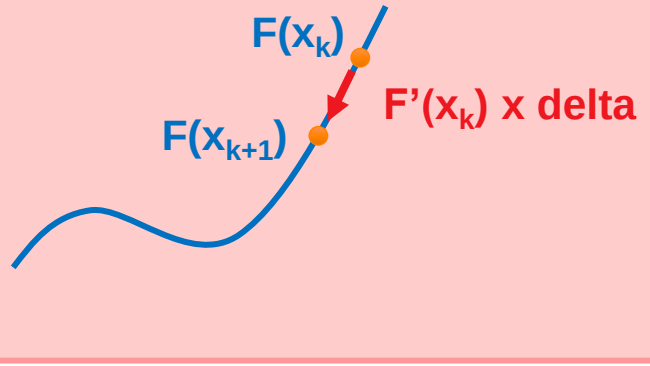
Placement

Equation to be Solved

Ability of the solver to find the answer

$$F(x) = \Sigma wirelength\_cost + \beta.\Sigma overlap\_cost + \gamma.\Sigma timing\_cost$$

(must be differentiable)



EDA Goals

- Best QoR
- Less runtime
- Less compute resources

There is usually a tradeoff among the above factors. For example, more runtime might be required to improve the QoR.

Challenges

- Increasing design complexities
- Exponential jump in technology constraints for advanced nodes
- Predictability
- Scalable solution

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