



# Mixed-Signal Verification

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Date

# Agenda

- Verification Review- Analog, Digital, and Mixed-Signal
- Mixed-Signal Verification and Challenges of Mixed-Signal Verification
- Mixed-Signal Verification Flow and Methodology
- Cadence Spectre and AMS Designer Mixed-Signal Verification Platform
- Mixed-Signal Verification– Managing Accuracy and Performance
  - Understanding AMS Designer
  - Behavioral models
  - Connect modules
- Spectre AMS Designer: Advanced Methodologies
  - Extend analog analyses to mixed-signal: aging, fault simulation
  - Power-aware mixed-signal verification
  - Extend digital verification methodologies to mixed-signal: UPF, UVM, coverage, assertions
- Summary

# Verification – Analog, Digital, and Mixed Signal

### Analog

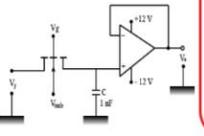


```

subckt ana_gate inleft[0] inleft[1] inright[0] in
xand1 inleft[0] inleft[1] out1 out2 out1 nand2
xand2 inright[0] inright[1] out1 out2 nand2
.ends ana_gate
                    
```

DSPF for Post Layout

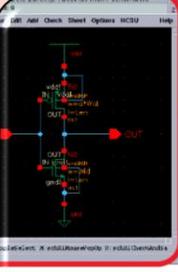
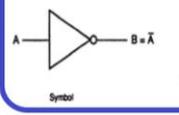
V, I, W



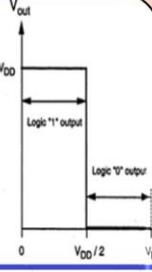
```

`include "constants"
`include "disciplines"
module inverter_1(
output out;
input in;
electrical out_in;
integer d_out,vdd;
analog begin
vdd = 1;
                    
```

### Mixed Signal

A	B
0	1
1	0



Translation needed from analog "VDD" to Logic "1" and vice versa.

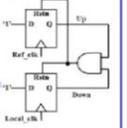
A2D and D2A conversion

Need both 'Analog' & 'Digital' simulation.

### Digital

```

if (!posedge ref_clk or posedge ff_clr or anedge rate)
begin
1: (ffdata) up <= 1'b0;
else if (ff_clr) up <= 1'b0;
else up <= 1'b1;
end
always @(posedge local_clk or posedge ff_clr)
begin
1: (ffdata) down <= 1'b0;
else if (ff_clr) down <= 1'b0;
else down <= 1'b1;
end
                    
```



Signal a	Signal b	Measured value of a and b
0	0	0
0	1	1
1	0	0
1	1	1
X	X	X
Z	Z	Z
W	W	W
U	U	U
V	V	V

Functional Timing verification.  
Coverage Assertions

Analog schematic, netlist or Verilog-A behavioral model.

**Quantities : V,I,W**

Measurements such as **Gain, Bandwidth, Power, leakage, Noise figure, etc.**

Need analog simulations(Spectre)

Analog netlist + RTL (e.g. Spice + Verilog)

**Quantities : V,I,W & Logic states : 1,0,X,Z,U**

Mainly functional coverage + analog measurements

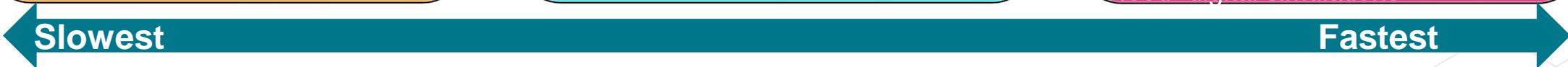
Need 'Mixed Signal simulations'.  
**Analog +Digital**

RTL representation(.v, sv, etc.)

Logic states: 1,0,X,Z,U

Measurements such as timing delays (Setup, hold violations).Mainly functional coverage

Need "digital simulations"



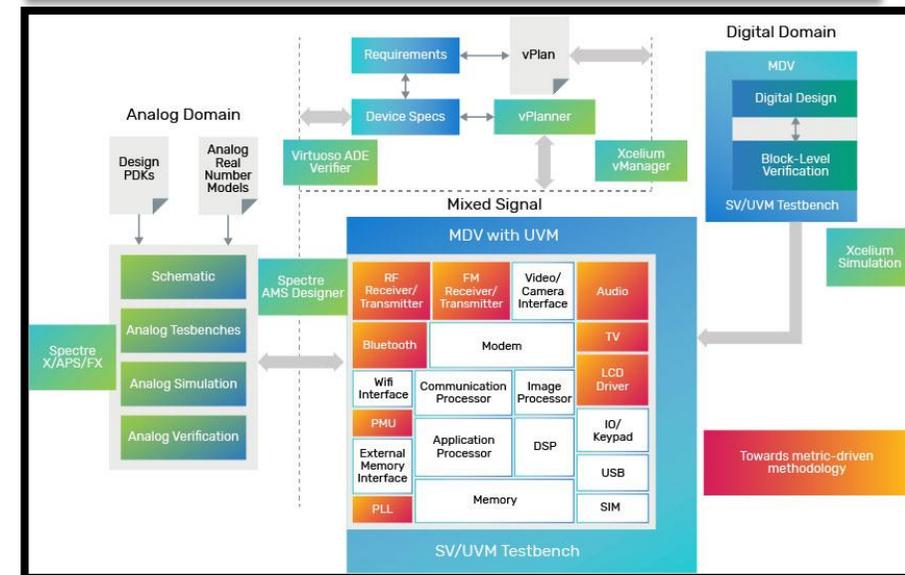
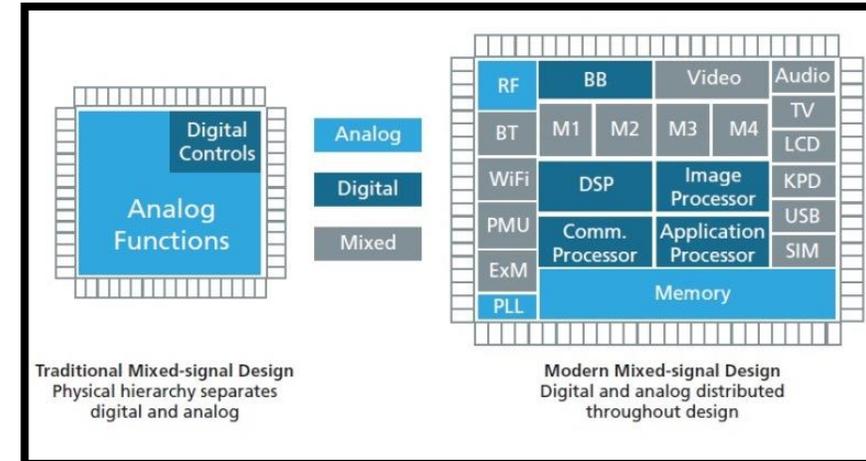
# Mixed-Signal Verification

Mixed-signal applications are among the fastest-growing market segments in the electronics and semiconductor industry.

Consumers expect electronics *to do more—in more places—than ever before*.

- In today's SoC designs, the level of interaction between analog structures and digital logic is dramatically more complex
- Mixed-Signal Verification is about bringing together the analog and digital sides- Integration of analog behavior modeling and analog and digital solvers into one flow
- Mixed-Signal Verification Use Models
  - Digital-centric approach- Big D, Small A
  - Analog-centric approach- Big A, Small D
- With today's complex, mixed-signal SoCs, users must run full-chip verification that covers all possible analog and digital interactions

**No Black Box Approach**

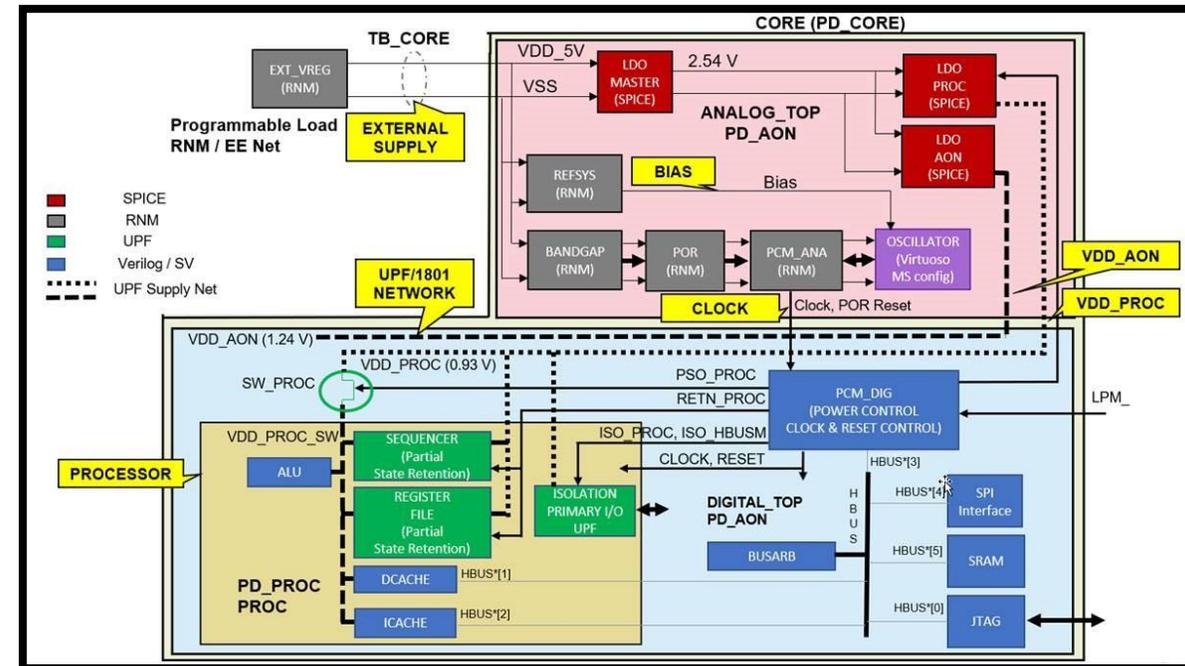


# Mixed-Signal Verification-Challenges

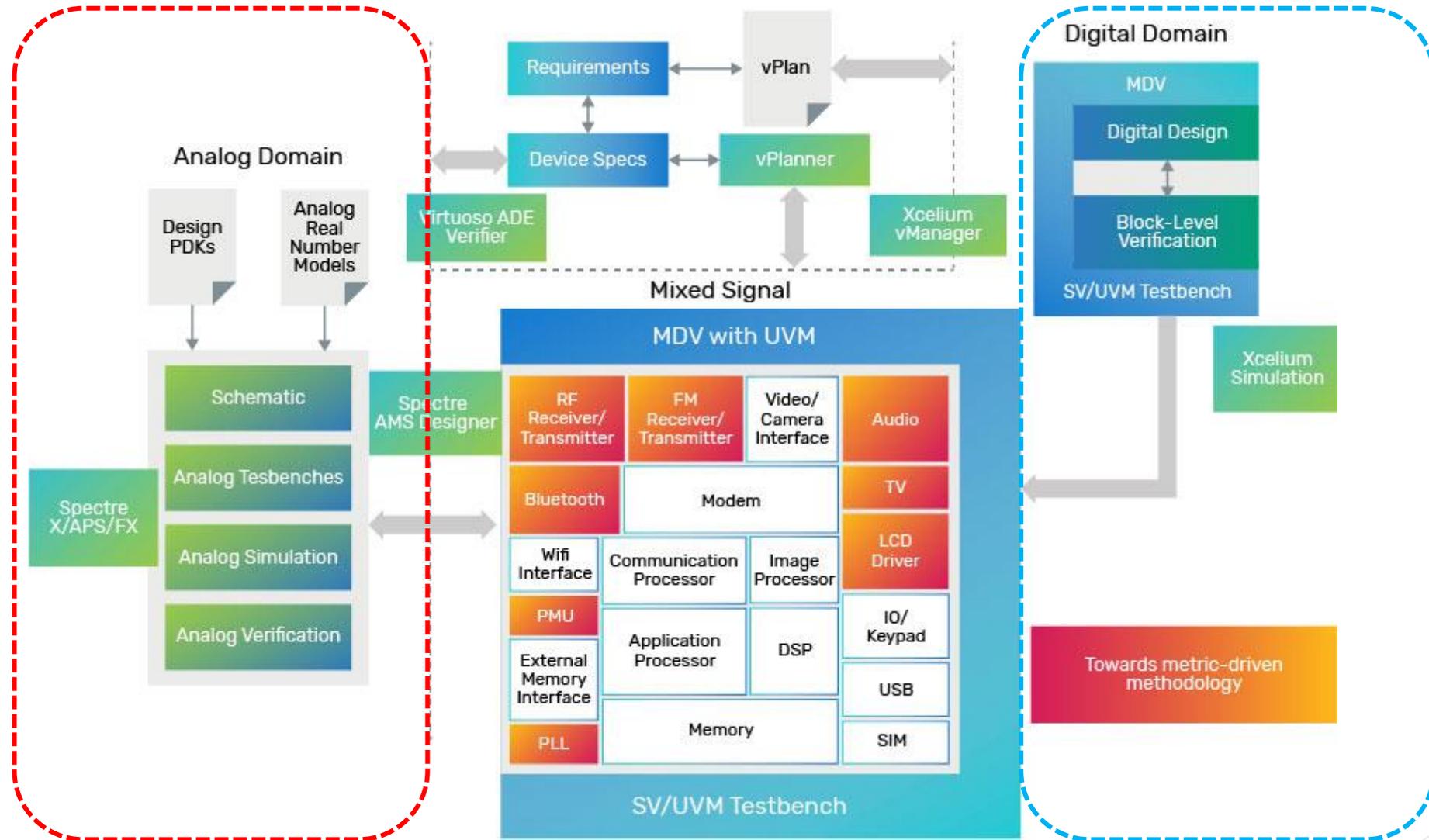
Today's mixed-signal designs have multiple feedback loops through analog and digital domains. The new world is a complex, multilayered fusion of the two disciplines, *where the boundaries are fuzzy and the interactions complex!*

- How do I verify the digital content in this SoC?
- How do I verify the mixed-signal interconnects?
- How do I verify the mixed-signal IP?
- How do I abstract analog behavior?
- Analog and digital simulations use fundamentally different paradigms. While digital simulators solve logical expressions sequentially by triggering events, analog simulators must solve the entire analog system matrix at every time step
- Today's designs involve a lot more advanced low-power techniques that are causing new complications for mixed-signal verification

*Need for a single verification environment combining both analog and digital solvers that can be used to functionally verify at the desired level of accuracy.*

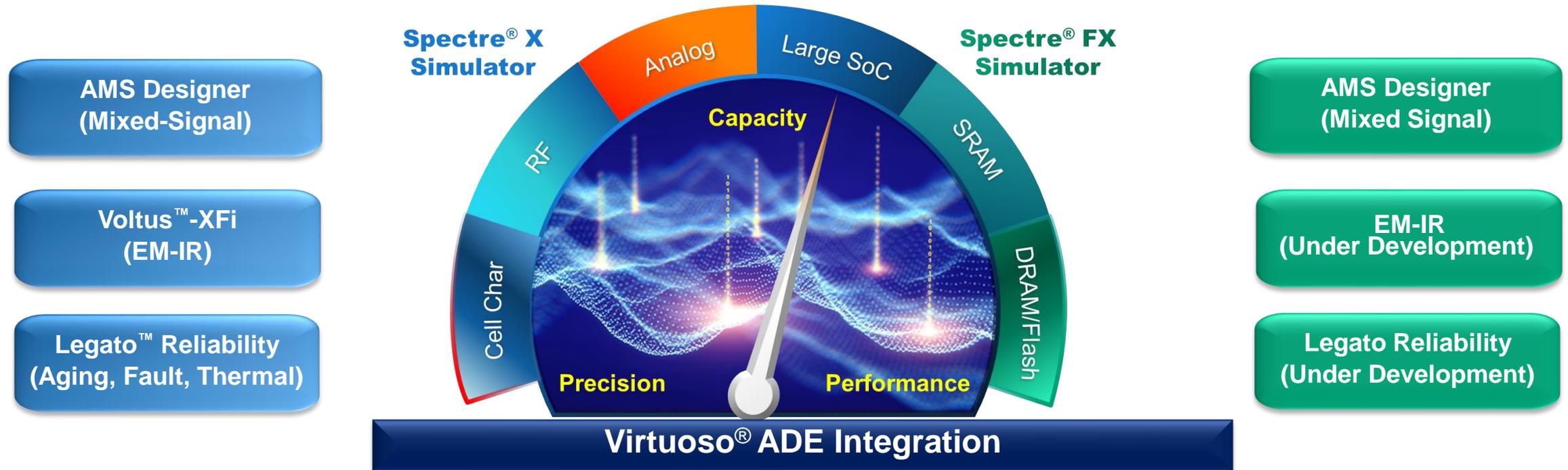


# Mixed-Signal Verification Flow and Methodology



# Spectre Simulation Platform Offers a Complete Portfolio

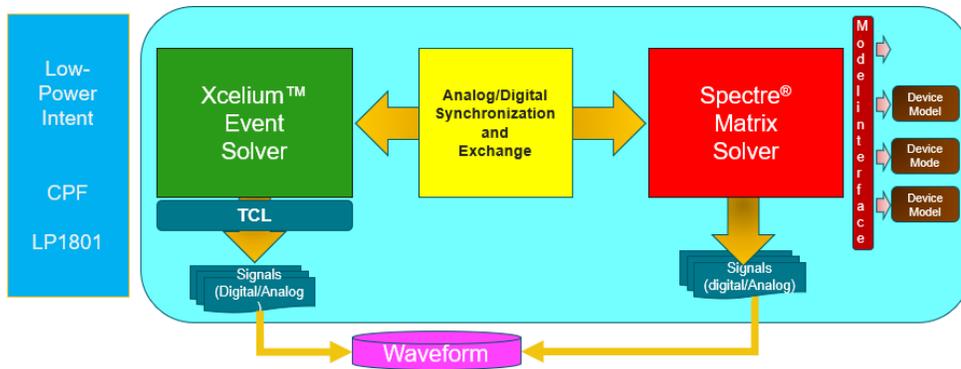
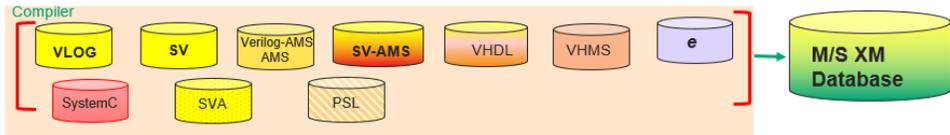
Industry's most comprehensive custom simulation solution



- ▶ **Golden** SPICE - Industry standard: Most trusted with golden SPICE accuracy
- ▶ **Fast:** Spectre X: 3X – 10X speedup and up to 5X increased capacity while maintaining accuracy
- ▶ **Even Faster:** Spectre FX FastSPICE: Up to 3X speedup with the required accuracy on large designs

# Mixed-Signal Verification

## Managing accuracy and performance



### Integration on Digital & Analog simulators

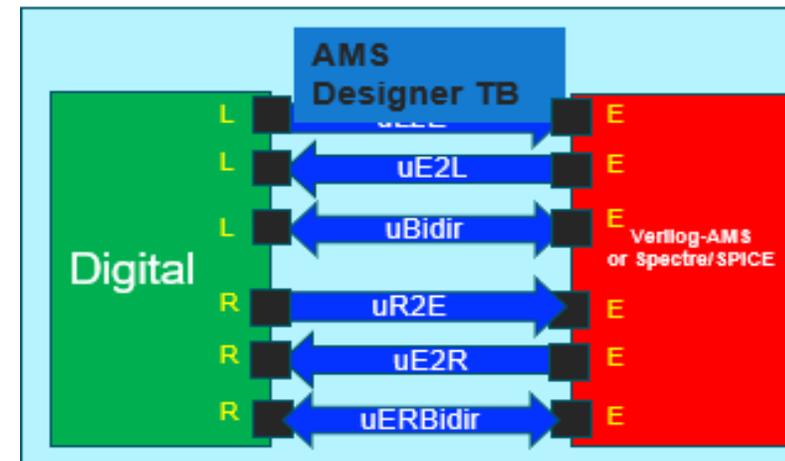
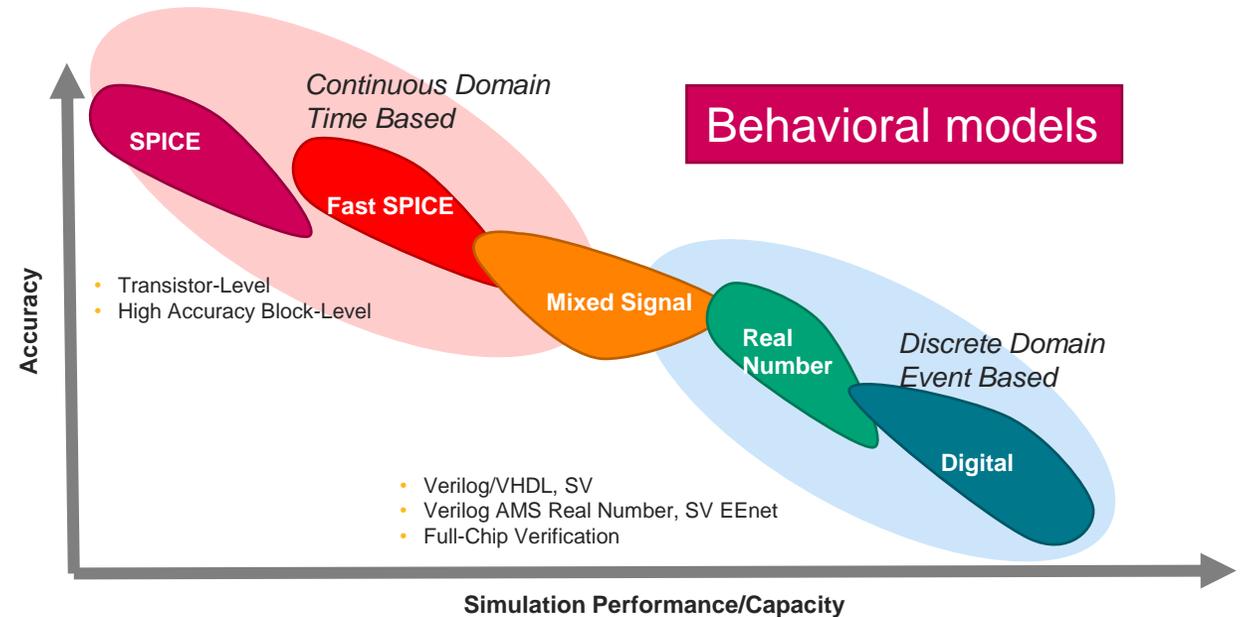
- Multi-engine support with a choice of different solvers Spectre X and FX
- Single kernel execution (Analog and Digital).

### Behavioral models

- Support for all types of HDL and RNM approaches
- Provides the ability to trade-off between accuracy and performance

### Connect Modules

- Translation of digital events into analog values and vice versa.
- Should be able to define current strength and loading effects as well



UCM  
Unified Connect  
Module

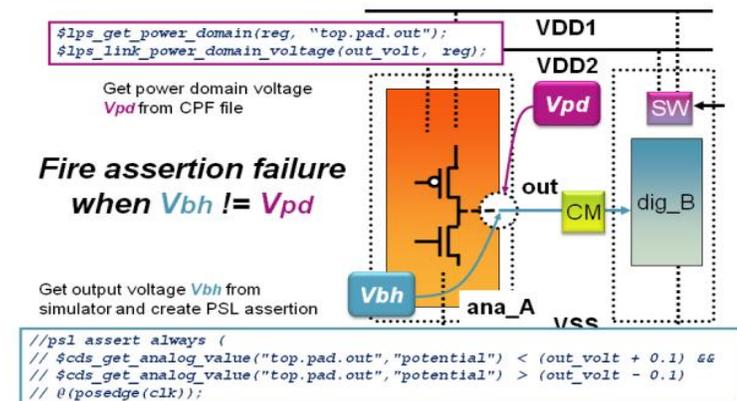
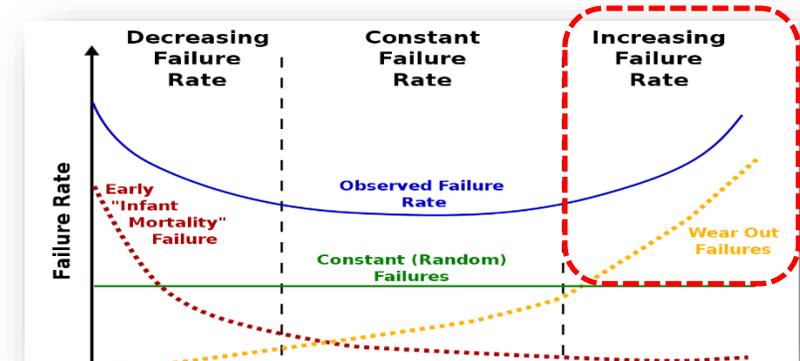
# Advanced Methodologies

Maximize verification coverage and quality with advanced methods

Extend Analog analyses to mixed-signal: Aging, Fault simulation

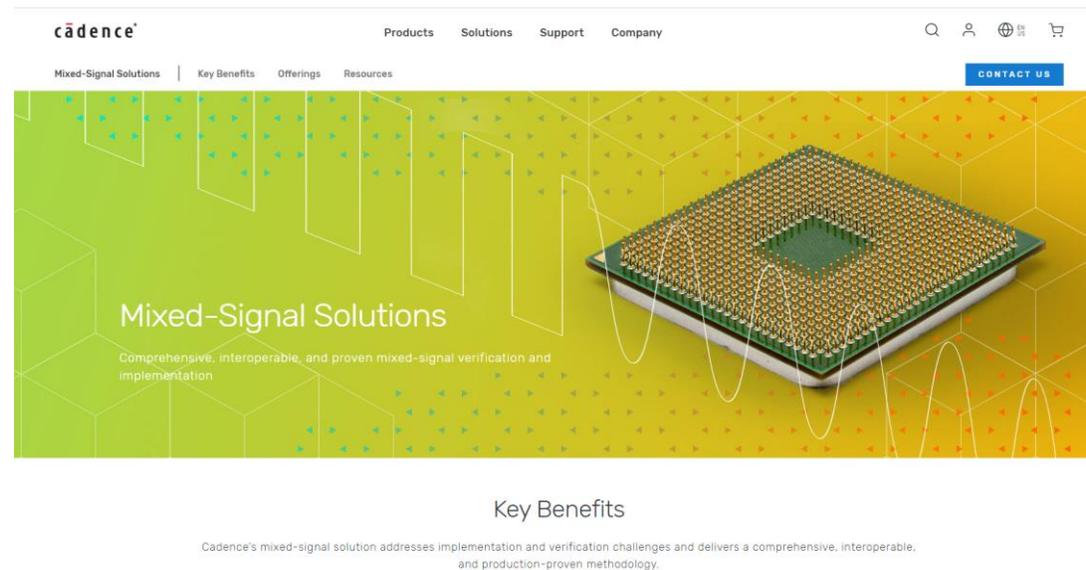
Power-aware mixed-signal simulation

Extend digital verification methodologies to Mixed-signal: UPF, UVM, Coverage, Assertions



# Summary

- In modern SoC designs, the level of interaction between analog structures and digital logic is dramatically more complex than in the past and poses more challenges
- Integrating analog behavior modeling and analog and digital solvers into one flow, the methodology lets you balance the right amount of accuracy and speed based on your design requirements
- For more details on Mixed-Signal Solutions: [www.cadence.com](http://www.cadence.com)





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