Designing with TSMC's Ultra Low Power (ULP) platform to connect intelligently and efficiently

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Outline

- About TSMC and TSMC's Grand Alliance
- TSMC and ARM Collaboration
- Implementation Recipe
- Summary
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TSMC: Full Technology Coverage

- **Expanding Functionality**
  - MEMS (Embedded Flash)
  - MCU
  - RF CMOS
  - Analog (5V)
  - Logic
  - BCD-Power IC
  - CMOS Image Sensor
  - High Voltage
  - Embedded DRAM

**Technology Node Sizes**
- 10nm
- 16nm
- 20nm
- 28nm
- 40nm
- 65/55nm
- 90/80nm
- 0.13/0.11µm
- 0.18/0.15µm
- 0.25µm
- 0.35µm
- >0.5µm

**Available (Red)**
- 10nm
- 16nm
- 20nm
- 28nm
- 40nm
- 65/55nm
- 90/80nm
- 0.13/0.11µm
- 0.18/0.15µm
- 0.25µm
- 0.35µm
- >0.5µm

**Developing (Green)**
- 10nm
- 16nm
- 20nm
- 28nm
- 40nm
- 65/55nm
- 90/80nm
- 0.13/0.11µm
- 0.18/0.15µm
- 0.25µm
- 0.35µm
- >0.5µm
Total Capacity Growth 11% in 2013

6” & 8” Fabs
- 6” Fab 2
- 8” Fabs
  - Fab 3
  - Fab 5
  - Fab 6
  - Fab 8
- 8” Fabs overseas
  - Fab 10 (China)
  - Fab 11 (USA)
  - SSMC (Singapore)
- Affiliate Fab (Vanguard)

12” GIGAFABs
- GIGAFAB 12
  - P1 + P2
  - P3
  - P4
  - P5
  - P6
- GIGAFAB 14
  - P1 + P2
  - P3
  - P4
  - P5
  - P6
- GIGAFAB 15
  - P1 + P2
  - P3 + P4

Total Capacity Growth 11% in 2013
Our Technologies Are In Your Mobile

**Advanced Technologies**

- **Application Processor**
  - (40/28/20/16nm)
- **Baseband**
  - (40/28/20/16nm)
- **BT/Wi-Fi/GPS**
  - (65/40nm)
- **Mini-USB**
  - (65nm)
- **Flash Controller**
  - (65/45nm)

**Specialty Technologies**

- **CIS Camera**
  - (0.11um/90/65nm)
- **Touch Controller**
  - (0.18/0.13um/90/55nm)
- **Power IC & Audio**
  - (0.25/0.18/0.13um)
- **Display Driver**
  - (80/55nm)
- **MEMS Microphone & Sensors**
  - (0.35/0.18um)
- **Fingerprint Sensor**
  - (0.18um)
Collaborate at a New Level – TSMC Grand Alliance

EDA / IP / Design Service

Key Equipment & Material Makers

Open Innovation Platform

Customers

TSMC Grand Alliance

2008 total IPs: <1,000
Today total IPs: >7,500

More R&D than any large IDM

The Most Powerful Innovation Force
TSMC OIP Innovation Partners

**IP (40)**

**EDA (27)**

**DCA (25)**

**VCA (9)**
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TSMC & ARM together

- Mutual Customers and Focus
- *Leaders* in Our Respective Industries
- Collaborative Business Model
  - We only succeed if our customers succeed
  - We help our customers, we do not compete with them
A Legacy of Success

Cortex-A9 on 28HPM

Cortex-A15 Multicore on 20SoC

Cortex-A57 & Cortex-A53 on 16FF

10FF + ??
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FinFET Key Benefits

- Better $I_{D_{\text{Sat}}}$ performance
  - Higher intrinsic gain

- Faster for the same power
  - Or, lower power for same speed

- Better matching behavior

- Low leakage
  - Appreciably lower leakage
  - Lower off-state current
  - Lower voltage operation
FinFET Challenges

- Power scaling
  - Dynamic power does not scale linearly as the leakage power
  - High pin capacitance of the FINs

- Device tuning
  - Quantized transistor sizing
  - Minimum transistor sizing

- New variation signatures
  - Requires AOCV/SB-OCV-based sign-off
Double Patterning Technology

Mask 0

$$2X \text{ Pitch}$$

Mask 1

$$1X \text{ Pitch}$$

Final Pattern

$$2X \text{ Pitch}$$

Silicon Wafer
Smallest Cell != Smallest Logic Area

- Insufficient Pin Access
- DRC Error after Abutment
- Adequate Pin Access
- DRC-free after Abutment
Cortex-A57/A53 on N16FF
Cortex-A57/A53 on N16FF
Cortex-A57/A53 on N16FF
Cortex-A57/A53 on N16FF
Cortex-A57/A53 on N16FF
Cortex-A57/A53 on N16FF

- Total Power
- Tablet Sustained Power Envelope
- Smartphone Sustained Power Envelope

Performance:
- N16 Signoff
- N16 Silicon
- 2.3GHz
- 75mW

Cortex-A57
Cortex-A53
Cortex-A57/A53 on N16FF
Ultra-Low-Power Technology Summary

- TSMC offers ULP technology platform for IoT applications
  - 0.18eLL, 90uLL: In production
  - 55ULP, 40ULP and 28ULP: Risk production in 2015
  - RF and Embedded Flash features for IoT SoC integration

- Multiple technology options to meet diverse IoT product requirements
  - Low-duty-cycle applications / Low leakage: 0.18eLL, 90uLL, 55ULP or 40ULP
  - High-performance applications / Low dynamic power: 40ULP, 28ULP

- OIP ecosystem shortens product time-to-market by leveraging existing solutions while evolving toward ultra low power support
Ultra-Low-Power Technology Offering

- **Lower Vdd for Power Reduction**
  - N55: 1.2V, 0.9V
  - N40: 1.1V, 0.9V
  - N28: 0.9V, 0.7V

- **High-Vt Device for Leakage Control**
  - N55: 1X, 0.3X
  - N40: 1X, 0.3X
  - N28: 1X, 1X

- **Low-leakage SRAM Bit Cell**
  - N55: 1X, 0.2X
  - N40: 1X, 0.2X
  - N28: 1X, 0.6X

- **Ideff Improvement for Speed (N28ULP)**
  - HVT: 0.9V, 0.7V
  - LVT: 1.2V, 1.1V
  - SVT: 0.9V, 0.7V

- **Lower Vdd for Power Reduction**
  - LP: 1.2V, 1.1V, 0.9V
  - uLP: 0.9V, 0.7V

- **High-Vt Device for Leakage Control**
  - LP: 1X, 0.3X, 1X
  - uLP: 0.3X, 1X, 1X

- **Low-leakage SRAM Bit Cell**
  - LP: 1X, 0.2X, 0.9V
  - uLP: 0.2X, 0.2X, 0.6X
Ultra-Low-Power Technology Definition

Technology
- Device optimized for 0.7V~0.5V range
- Device enhancement for extremely low leakage
  - High-Vt device for leakage reduction
  - Low-Vt device to achieve target speed
- SRAM bit cell enhancement and innovation for low Vccmin

Ecosystem
- EDA tool accuracy at 0.5V
- Sign-off corner tightening to reduce conservatism
- Low-Vdd design methodology
- Low-Vdd foundation IP’s: standard cells, SRAM, RF
# 28ULP Design Enablement Plan

<table>
<thead>
<tr>
<th>Deliverable</th>
<th>Item</th>
<th>V0.1</th>
<th>V1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Collateral</strong></td>
<td>DRM</td>
<td></td>
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<td></td>
<td>SPICE</td>
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<td>Tech Files</td>
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<td></td>
<td>PDK</td>
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<td><strong>Foundation Library/IP</strong></td>
<td>Standard Cell</td>
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<td>SRAM Compiler/Macro</td>
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<td><strong>Non Volatile Memory</strong></td>
<td>Electrical Fuse</td>
<td></td>
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<td>OTP</td>
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<td><strong>Interface IP</strong></td>
<td>DDR3/DDR3L</td>
<td>Re-use</td>
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<td>LPDDR3</td>
<td>Re-use</td>
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<td>PCIe G2/3</td>
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<td>MIPI M/D-PHY</td>
<td>Re-use</td>
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<td>SATA I/II/III</td>
<td>Re-use</td>
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<td>USB 2.0</td>
<td>Re-use</td>
<td></td>
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<td>HDMI 1.4/MHL 2.0</td>
<td>Re-use</td>
<td></td>
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<tr>
<td><strong>Mixed-Signal / Analog</strong></td>
<td>ADC/DAC</td>
<td>Re-use</td>
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<td>VR</td>
<td>Re-use</td>
<td></td>
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<td>RF</td>
<td>Re-use</td>
<td></td>
</tr>
</tbody>
</table>

- **Q3’14**
- **Q4’14**
- **Q1’15**
- **Q2’15**
## 40ULP & 55ULP IP Plan

<table>
<thead>
<tr>
<th>Deliverable</th>
<th>Item</th>
<th>N40ULP</th>
<th>N40eF_ULP</th>
<th>N55ULP</th>
<th>N55eF_ULP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collateral</td>
<td>DRM</td>
<td></td>
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<td></td>
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<td></td>
<td>SPICE</td>
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<td>Tech Files</td>
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<tr>
<td>Foundation IP</td>
<td>Standard Cell</td>
<td></td>
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<tr>
<td></td>
<td>Thick Oxide Standard Cell</td>
<td></td>
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<td></td>
<td>GPIO</td>
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<td></td>
<td>SRAM Compilers</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td></td>
<td>Security ROM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NVM IP</td>
<td>eFuse</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>eFlash</td>
<td>N/A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interface IP</td>
<td></td>
<td></td>
<td>Re-use</td>
<td></td>
<td>Re-use</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(USB)</td>
<td></td>
<td>(USB)</td>
</tr>
<tr>
<td>Mixed-Signal IP</td>
<td>High-Resolution, Low-Speed ADC</td>
<td></td>
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- New design kits to support lower Vdd (0.9V)
- Existing IPs can still be used at original Vdd (1.1V/1.2V)
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TSMC and ARM are industry leaders collaborating to create the best solution for our customers.

TSMC and ARM understand the importance of offering a broad range of products and working with ecosystem partners to fit your needs for today and tomorrow.

TSMC offers the most comprehensive ultra-low power technology platform aimed at Internet of Things (IoT) and wearable device markets, with significant power reduction benefits and a comprehensive design ecosystem to accelerate time-to-market.