ARM® Versatile™ Express Juno Development Platform

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V2M-Juno Technical Reference Manual

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Frontmatter

V2M-Juno Technical Reference Manual

Release information

Document History

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A-01	27 January 2014	Confidential - Draft	First draft
A-02	20 February 2014	Confidential - Draft	Second draft
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110 Fulbourn Road, Cambridge, England CB1 9NJ.

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Product status

The information in this document is for a Beta product, that is a product under development.

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Contents

ARM® Versatile™ Express Juno Development Platform V2M-Juno Technical Reference Manual

Preface

This preface introduces the *ARM® Versatile™ Express Juno Development Platform V2M-Juno Technical Reference Manual*.

It contains the following:

About this book

This book describes the Versatile Express Juno Development Platform (V2M-Juno)

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n*
: Identifies the major revision of the product.

p*n*
: Identifies the minor revision or modification status of the product.

Intended audience

This book is written for experienced hardware and software developers to aid ARMv8 software and tooling development in the Juno ARM Development Platform SoC using the V2M-Juno motherboard.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter provides an introduction to the Versatile Express Juno Development Platform.

Chapter 2 Hardware Description

This chapter describes the Versatile Express V2M-Juno motherboard hardware.

Chapter 3 Configuration

This chapter describes the powerup and configuration process of the Versatile Express V2M-Juno motherboard.

Chapter 4 Programmers Model

This chapter describes the programmers model of the Versatile Express V2M-Juno motherboard.

Appendix A.1 Signal Descriptions

This appendix describes the signals present at the interface connectors of the Versatile Express V2M-Juno motherboard.

Appendix B.2 Prototype V2M-Juno motherboard

This appendix describes the Versatile Express V2M-Juno motherboard that provides two SMC USB 2.0 ports.

Appendix C.3 Specifications

This appendix contains the electrical specifications of the Versatile Express V2M-Juno motherboard

Appendix D.4 Revisions

This appendix describes the technical changes between released issues of this book.

Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM Glossary* for more information.

Typographic conventions

italic
: Introduces special terminology, denotes cross-references, and citations.

bold
: Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
: Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space
: Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
: Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
: Denotes language keywords when used outside example code.

<and>
: Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

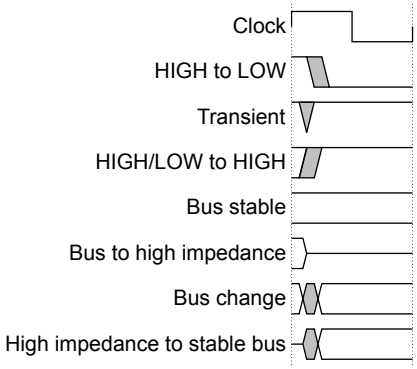

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
: The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n
At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

ARM publications

- *Juno ARM® Development Platform SoC Technical Reference Manual* (DDI 0515).
- *Application Note AN415 Example LogicTile Express 20MG design for a V2M-Juno Motherboard* (ARM DAI 0415).
- *LogicTile Express™ 3MG Technical Reference Manual* (DUI 0449).
- *ARM® LogicTile Express™ 13MG Technical Reference Manual* (ARM DUI 0556).
- *LogicTile Express™ 20MG Technical Reference Manual* (DDI 0498).
- *ARM® CoreLink™ TLX-400 Network Interconnect Thin Links Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0028).
- *ARM® PrimeCell™ Technical Reference Manual Real Time Clock (PL031)* (ARM DDI 0224).
- *ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050)* (ARM DDI 0143).
- *ARM PrimeCell™ General Purpose Input/Output (PLO61)Technical Reference Manual* (ARM DUI 0142).
- *ARM Dual-Timer Module (SP804) Technical Reference Manual* (ARM DDI 0271).
- *ARM Watchdog Module (SP805) Technical Reference Manual* (ARM DDI 0270).
- *CoreLink SMC-35x Static Memory Controller Series Technical Reference Manual* (ARM DDI 0380).
- *AMBA 3 AHB-Lite Protocol Specification v1.0* (ARM IHI 0033).
- *AMBA 3 APB Protocol Specification v1.0* (ARM IHI 000024).
- *ARM DSTREAM® Setting up the Hardware* (ARM DUI 0481).
- *ARM DSTREAM® and RVI® Using the Debug Hardware Configuration Utilities* (ARM DUI 0498).
- *CoreSight Components Technical Reference Manual* (ARM DDI 0314).

Other publications

- See the Linaro website *http://www.linaro.org/downloads/* for Linaro software.

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Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

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- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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- The title.
- The number ARM DDI0524A_03h.
- The page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

——— **Note** ———

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Chapter 1
Introduction

This chapter provides an introduction to the Versatile Express Juno Development Platform.

It contains the following sections:

1.1 Precautions

This section contains advice about how to prevent damage to your V2M-Juno motherboard.
This section contains the following subsections:

1.1.1 Ensuring safety

An on-board connector supplies 12V DC to the Juno Development Platform.

Warning

Do not use the Juno Development Platform near equipment that is sensistive to electromagnetic emissions, for example, medical equipment.

1.1.2 Preventing damage

The Juno Development Platform is intended for use within a laboratory or engineering development environment. It is supplied with an enclosure that leaves the board sensitive to electrostatic discharges and permits electromagnetic emissions.

Caution

To avoid damage to the Juno Development Platform, observe the following precautions:

- You must connect the external power supply to the board before powerup to prevent damage.
- Never subject the board to high electrostatic potentials. Observe Electrostatic Discharge (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Do not use the board near a transmitter of electromagnetic emissions.

1.2 About the Versatile Express Juno Development Platform

The Juno Development Platform, the V2M-Juno motherboard is a development motherboard that provides access to the Juno ARM Development Platform SoC. The Juno ARM Development Platform SoC is a development chip that supports ARMv8 software tooling, evaluation and development.

The V2M-Juno motherboard provides the following:

Juno ARM Development Platform SoC (Juno SoC)

The Juno ARM Development Platform SoC provides a fully coherent dual-core Cortex-A57 cluster, a fully coherent quad-core Cortex-A53 cluster and an IO-coherent Mali-T624 quad-core GPU cluster.

The dual-core Cortex-A57 cluster contains a 2MB L2 cache and NEON and FPU operating at nominal 800MHz, overdrive 1.1GHz.

The quad-core A53 cluster has a 1MB L2 cache and NEON and FPU operating at nominal 700MHz, overdrive 850MHz.

The Mali-T624 quad-core cluster operates at nominal 600MHz, no overdrive.

Separate power domains support power management through *Dynamic Voltage and Frequency Scaling* (DVFS) of the A57, A53 and GPU clusters.

LogicTile site

The V2M-Juno motherboard provides two headers that enable you to fit a Versatile Express LogicTile daughterboard. A Thin Links TLX Network Interconnect connects the motherboard and daughterboard.

Powerup and configuration

An on-board EEPROM stores board and file identification information and a microSD card stores software images and configuration files. You can access the microSD card to perform configuration file editing and to update software images.

Configuration of the V2M-Juno motherboard and the LogicTile daughterboard, if fitted, proceeds automatically under the control of the *Motherboard Configuration Controller* (MCC) after powerup or reset.

You can customize the clock speeds and other configuration settings.

IOFPGA

The IOFPGA provides low-bandwidth peripherals that the Juno SoC does not provide. The IOFPGA connects to the Juno SoC through a 32-bit *Static Memory Bus* (SMB) with dedicated chip selects.

The IOPFGA also contains energy meters, consisting of dedicated registers, that form part of the power control and DVFS system.

External user memory

8GB on-board DDR3L 800MHz connects to memory interfaces in the Juno SoC. 64MB NOR Flash connects to the IOFPGA. The IOFPGA contains 256KB of user RAM.

Access ports

The V2M-Juno motherboard provides access through a general-purpose dual-UART, SMC 10/100 Ethernet, four USB 2.0 ports, and keyboard and mouse ports.

——— **Note** ———

The prototype version of the V2M-Juno motherboard also provides two SMC USB 2.0 ports. See *B.2.1 Overview of the prototype V2M-Juno motherboard* on page Appx-B-131 for information.

———————————

Video and audio output

The V2M-Juno motherboard provides dual HDMI outputs. The Juno SoC sends two independent 24-bit RGB video channels to the HDMI transmitters. Both HDMI ports share the same single I^2S audio from the Juno SoC.

Additional user key entry

The V2M-Juno motherboard supports trusted keyboard entry and additional key entry to simulate hand-held devices.

User LEDs

The V2M-Juno motherboard provides eight user LEDs that connect to the IOFPGA. The meaning of these LEDs depend on the software that you implement in the Juno SoC.

System LEDs

The V2M-Juno motherboard provides LEDs that denote the status of the board power supplies and read and write access to the configuration microSD card through the configuration USB port or configuration Ethernet port.

Debug

The V2M-Juno motherboard supports P-JTAG Processor debug that enables connection of DSTREAM or a compatible third-party debugger. The board also supports 32-bit trace.

1.3 Location of components on the V2M-Juno motherboard

The following figure shows the physical layout of the upper face of the V2M-Juno motherboard.

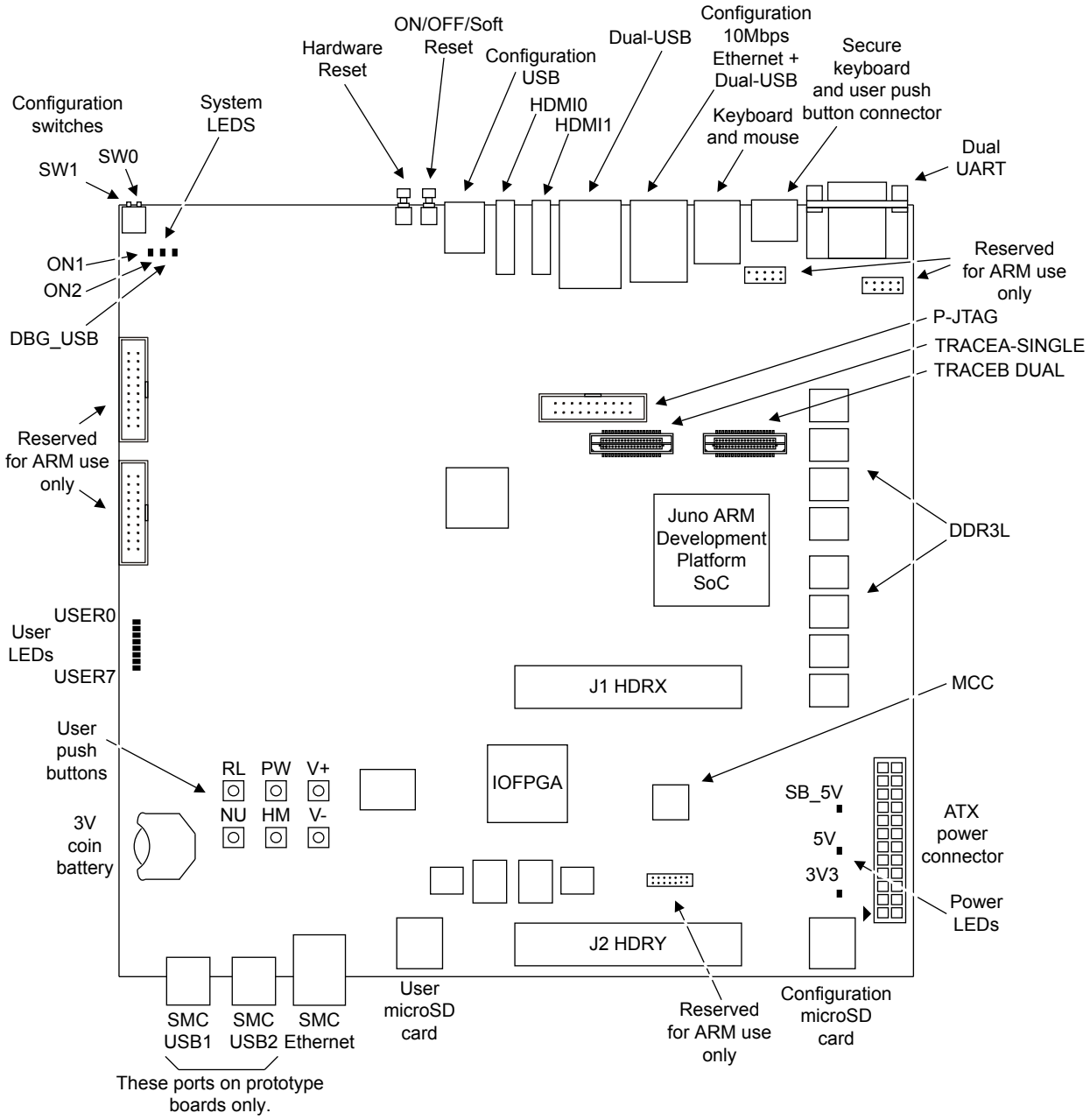

Figure 1-1 V2M-Juno motherboard layout, upper face

Note

The production version of the V2M-Juno motherboard does not provide the SMC USB ports. The prototype V2M-Juno motherboard provides these ports. See *B.2.1 Overview of the prototype V2M-Juno motherboard* on page Appx-B-131 for information on the prototype version of the V2M-Juno motherboard.

Chapter 2
Hardware Description

This chapter describes the Versatile Express V2M-Juno motherboard hardware.

It contains the following sections:

2.1 Overview of V2M-Juno motherboard hardware

The hardware infrastructure of the V2M-Juno motherboard supports ARMv8 software evaluation and tooling development using the Juno ARM Development Platform SoC.

The following figure shows the hardware infrastructure of the V2M-Juno motherboard.

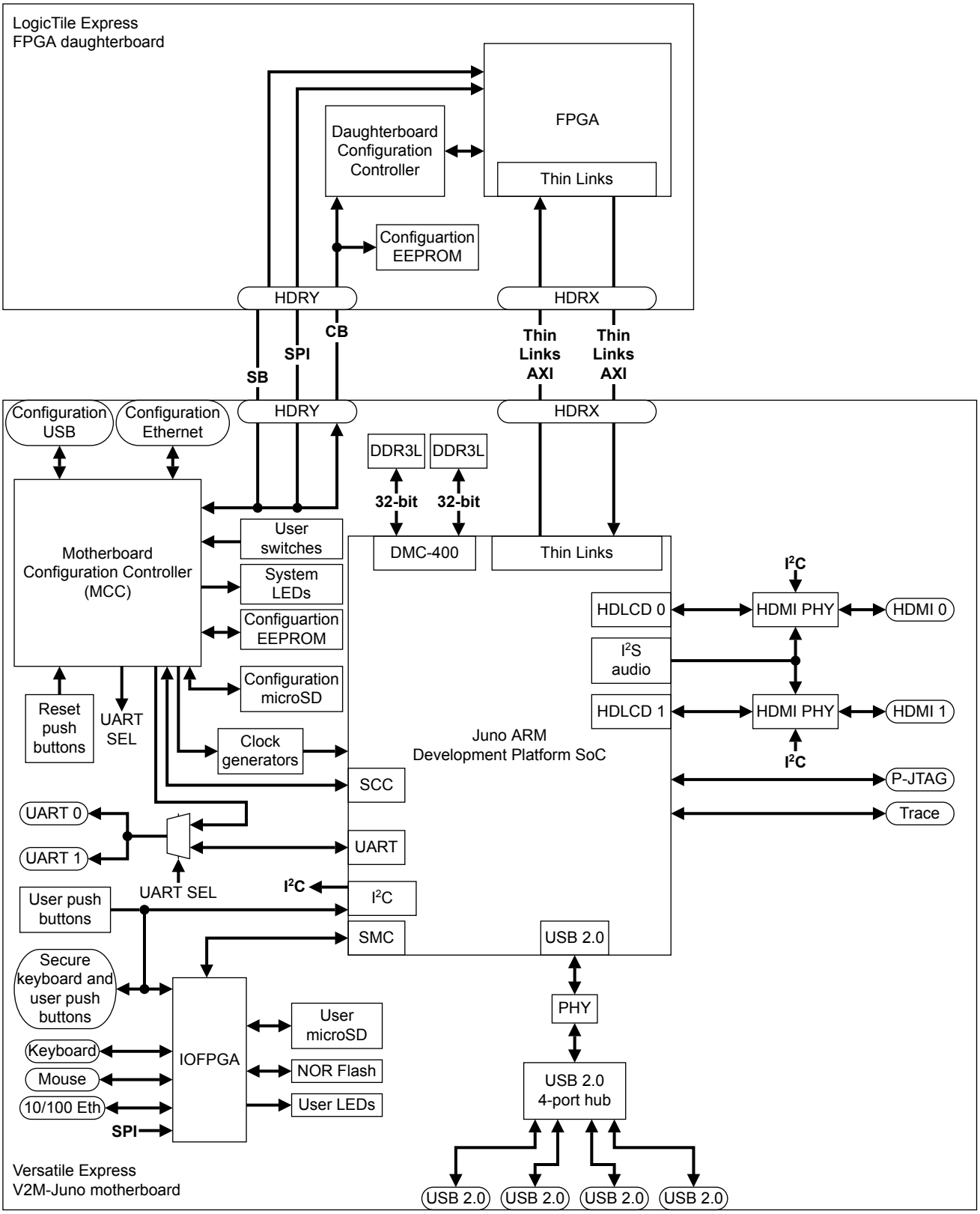

Figure 2-1 V2M-Juno motherboard system architecture with LogicTile FPGA daughterboard

The V2M-Juno motherboard contains the following components and interfaces:

- One Juno ARM Development Platform SoC:

  - Dual-core Cortex-A57, Quad-core Cortex-A53 and Mali-T624 quad-core GPU.
  - Memory interfaces, HDLCD display controllers, and other on-chip peripherals.
- Site for LogicTile Express daughterboard:
  - Two headers, *HDRX* and *HDRY*, enable you to fit any Versatile Express LogicTile daughterboard in this site.
  - Thin Links AXI master and slave interfaces to LogicTile site.
- One ARM Cortex-M3 *Motherboard Configuration Controller* (MCC):
  - Supports configuration of the Juno SoC and V2M-Juno motherboard at powerup or reset.
    - Clock generator configuration.
    - Loading of *Real Time Clock* (RTC) registers.
    - Board configuration.
    - Pre-loading of external memory.
- One microSD card that stores the following:
  - Board configuration files.
  - Software images.
- One EEPROM that stores board identification information and file names for the configuration system.
- Configuration ports.

  The following ports support Drag-and-Drop editing of configuration files in the configuration microSD card:
  - Configuration USB 2.0 port.
  - Configuration 10Mbps Ethernet port.
- Two 32-bit 4GB DDR3L on-board memories:
  - Low-power.
  - 800MHz, 1600 million transfers per second (MTs).
- *Static Memory Controller* (SMC) 10/100 Ethernet.
- Four USB 2.0 ports, USB 4-port hub and USB PHY.
- Two UARTs:
  - UART 0 can connect to the Juno SoC or to the MCC.
  - UART 1 can connect to the Juno SoC or to the Daughterboard Configuration Controller on the LogicTile daughterboard fitted in the daughterboard site.The board configuration files, that you can edit using the configuration ports, determine the connectivity of the UART ports during runtime.

    Note

    The Daughterboard Configuration Controller is a microcontroller on the LogicTile that controls the configuration of the daughterboard during powerup or reset.
- Two HDLCD ports that each support:
  - HDMI 1.4a up to 1080p.
  - One I^2S four-channel stereo audio output.
- Four USB 2.0 ports, USB 4-port hub and USB PHY.
- Additional user key entry:
  - Trusted User Keyboard entry using the secure keyboard connector.
  - Additional user key entry using the push buttons on the V2M-Juno motherboard to simulate hand-held devices.

- IOFPGA that contains registers that form part of the Power Control and DVFS system. The IOFPGA also provides access to low-bandwidth peripherals, user switches and user LEDs that the Juno SoC does not provide.

  — 64MB NOR Flash.
  — 256KB IOFPGA internal block RAM.
  — User microSD card slot.
  — Keyboard and Mouse ports.
  — Six user push buttons for additional user key entry.
  — System registers.
  — Current, voltage, power and energy meters.
  — Timers.
  — Eight user LEDs. Application software defines their meaning.

  Note

  The prototype V2M-Juno motherboard also provides two SMC USB 2.0 ports that connect through the IOFPGA. See *B.2.1 Overview of the prototype V2M-Juno motherboard* on page Appx-B-131.

- Nine programmable clock generators.
- A real-time clock in the MCC:

  — A 3V coin battery powers the real-time clock when the board is powered down.
- Three system LEDs.

  These LEDs connect to the MCC:

  — *ON1* LED. Reserved for ARM use only.
  — *ON2* LED. Denotes ATX power supply powered up.
  — *Debug USB* LED. Denotes read or write access to the configuration microSD card through the configuration USB 2.0 port.
- Debug ports:

  — 32-bit CoreSight Trace port.
  — Processor CoreSight debug (P-JTAG) port.

2.2 Juno ARM Development Platform SoC

This section provides an overview of the components of the Juno ARM Development Platform SoC. This development chip, or Juno SoC, provides a a dual-core Cortex-A57 cluster, quad-core Cortex-A53 cluster, a quad-core Mali-T624 graphics cluster, interfaces, on-chip peripherals and internal network connect.

The following figure shows the architecture of the Juno ARM Development Platform SoC.

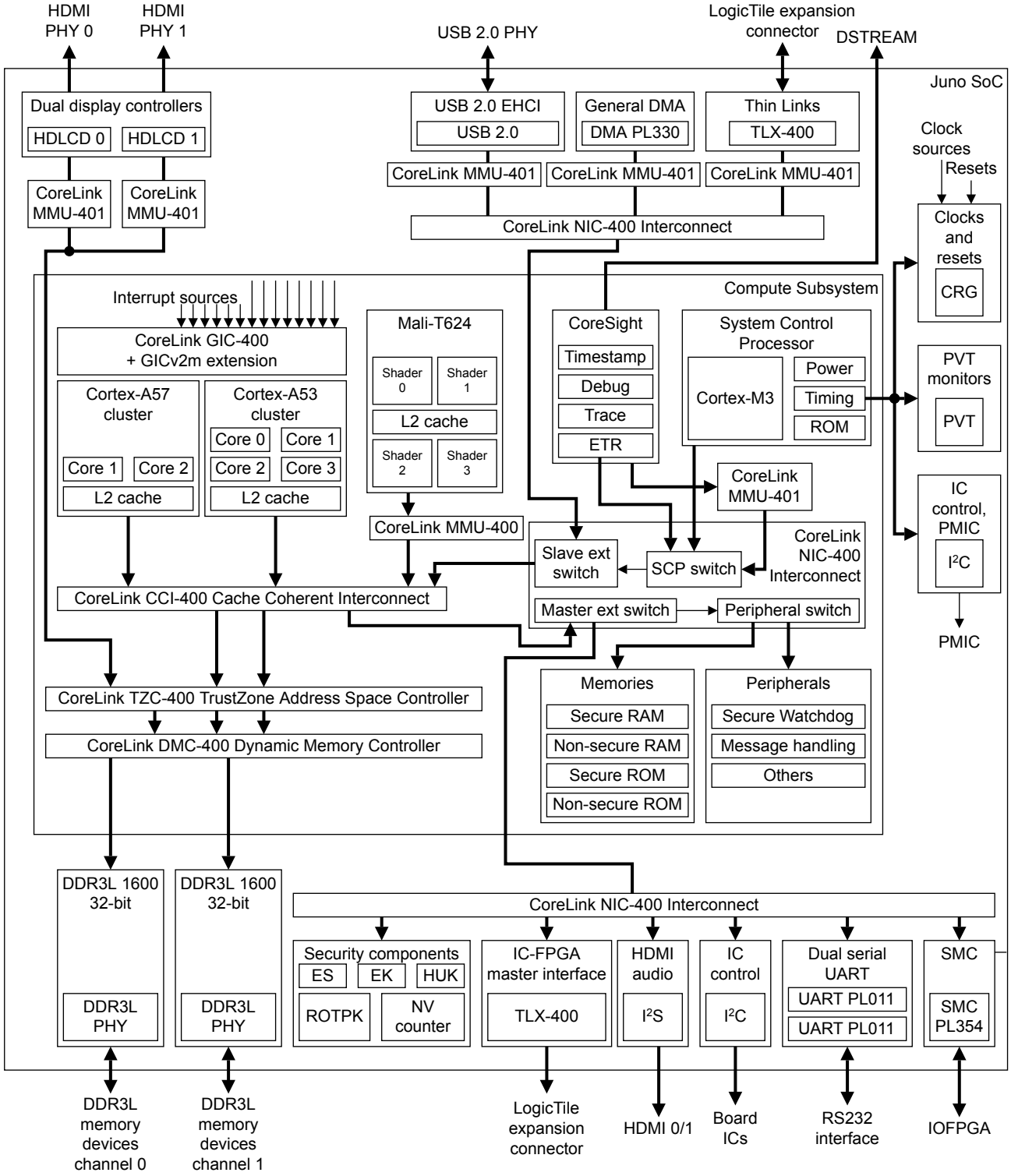

Figure 2-2 Architecture of the Juno ARM Development Platform SoC

The Juno ARM Development Platform SoC contains the following components and interfaces.

- Dual-core Cortex-A57 cluster operating at nominal 800MHz, overdrive 1.1GHz:
  - 2MB L2 cache.
  - NEON and *Floating Point Unit* (FPU).
- Quad-core Cortex-A53 cluster operating at nominal 700MHz, overdrive 850MHz:

  - 1MB L2 cache.
  - NEON and *Floating Point Unit* (FPU).
- Mali-T624 quad-core GPU cluster operating at 600MHz.
- Internal AXI subsystem operating at up to 533MHz.
- Dual ARM HDLCD Display Controllers:
  - Supports HDMI 1.4a up to 1080p.
- Dual DDR3L PHY and 32-bit DDR3L interfaces.
- Thin Links AXI master and slave interfaces to the LogicTile site. At the default clock frequency of 61.5MHz, the operating bit rates are:
  - Master interface: 68Mbps in the forward direction and 78Mbps in the reverse direction.
  - Slave interface: 246 Mbps in the forward direction and 305Mbps in the reverse direction.

    Note

    The forward direction is from master to slave and the reverse direction is from slave to master.
- USB 2.0 Host Controller:
  - 480Mbps ULPI interface to off-chip PHY.
- PL354 *Static Memory Controller* (SMC).
- PL330 *Direct Memory Access* (DMA) controller.
- CoreSight Processor debug (P-JTAG) and Trace.
- APB subsystem:
  - Dual-UART.
  - I^2S 4-channel stereo audio.
  - Power, Voltage, and Temperature (PVT) monitoring of Juno ARM Development Platform SoC.
  - Non-volatile counter. A real time clock that retains its stored value after powerdown.
  - *System Control Processor* (SCP). This is a Cortex-M3 processor integrated into the Juno ARM Development Platform SoC. It initiates the system architecture and pre-load memory at powerup and performs power management and system control functions during runtime.
  - I^2C. This connects to HDMI controllers, the UART transceiver and other components on the V2M-Juno motherboard.
  - Secure I^2C. This connects to the Secure Keyboard.
  - Keys. Encryption keys for signing software.
  - Random-number generator. This operates with the encryption keys when validating software.
  - System override registers that enable you to override various aspects of the Juno ARM Development Platform SoC.

See the *Juno ARM® Development Platform SoC Technical Reference Manual* for information on the Juno ARM Development Platform SoC.

2.3 External power

You supply power to the V2M-Juno motherboard from the mains supply using the on-board connector and an external power supply unit and connector cable that ARM supplies with the board.

The external power supply unit converts mains power to 12V DC that connects to a plug-in ATX power module. The unit accepts mains power in the range 100-240V AC.

Alternatively, you can remove the module and connect an ATX power supply unit directly to the board.

On-board regulators supply power to the V2M-Juno motherboard power domains and to the power domains of the Juno ARM Development Platform SoC.

Power LEDs indicate that power domains are active:

5V
: 5V domain powered.

3V3
: 3V3 domain powered

SB_5V
: Standby 5V domain powered.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.
A.1.11 ATX power connector on page Appx-A-129.

2.4 Power control and Dynamic Voltage and Frequency Scaling (DVFS)

DVFS provides voltage, current, and power monitoring.

The V2M-Juno motherboard contains a *Power Management IC* (PMIC) that generates the V2M-Juno motherboard and Juno ARM Development Platform SoC power supplies. The Juno ARM Development Platform SoC, the Juno SoC, configures the PMIC through the System Control Processor (SCP) I^2C interface during powerup or reset.

Direct control of the PMIC through the SCP interface during runtime supports voltage scaling.

Varying the Juno ARM Development Platform SoC PLL dividers during runtime supports frequency scaling.

Note

ARM recommends that you use this method to achieve DVFS frequency scaling and do not use external control of the clock generators through the V2M-Juno motherboard SCP I^2C interface.

Dedicated logic blocks in the IOFPGA contain energy meters for the Cortex-A53, Cortex-A57, Mali-T624 GPU and VSYS supplies. The energy meters consist of current, voltage, power and energy registers in the APB Registers memory space.

The following figure shows the V2M-Juno motherboard power control and DVFS system.

Note

The VSYS supply powers the fabric of the Juno SoC outside the Cortex-A53, Cortex-A57 and Mali-T624 GPU clusters.

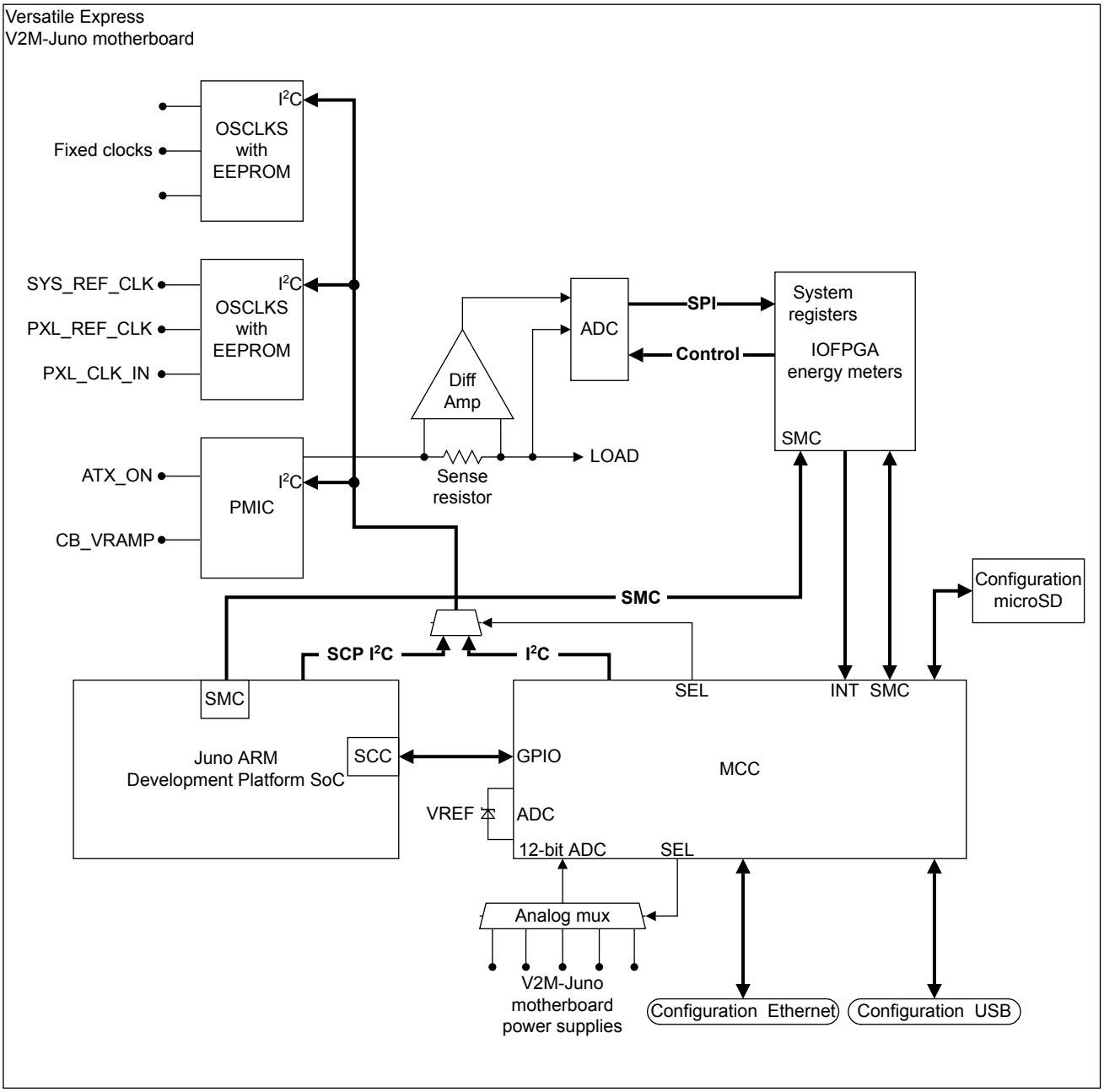

Figure 2-3 Power control and DVFS system

See the following documents for more information:

- *Juno ARM® Development Platform SoC Technical Reference Manual*

Related concepts

4.3.1 APB system register summary on page 4-87.

2.5 Clocks

This section describes the V2M-Juno motherboard clocks that drive the board, the Juno ARM Development Platform SoC and the LogicTile, if fitted in the daughterboard site.
This section contains the following subsections:

2.5.1 Overview of clocks

Clock generators on the V2M-Juno motherboard generate clocks for the internal blocks in the Juno ARM Development Platform SoC, the internal blocks in the IOFPGA, and the peripherals on the board.

During powerup or reset, internal EEPROMs in the clock generators configure the generators to the correct operational clock frequencies. The `board.txt` file also defines these default clock frequencies. You can change the operational clock frequencies by modifying the configuration `board.txt` file.

Note

ARM recommends that you operate the V2M-Juno motherboard at the default clock frequencies.

Related concepts

3.3.3 Contents of the MB directory on page 3-70.

2.5.2 Juno SoC and V2M-Juno motherboard clocks

The following figure shows the Juno ARM Development Platform SoC clocks and clock domains. The figure includes the clocks that connect to the LogicTile Express daughterboard, to some of the peripherals on the V2M-Juno motherboard and to the IOFPGA.

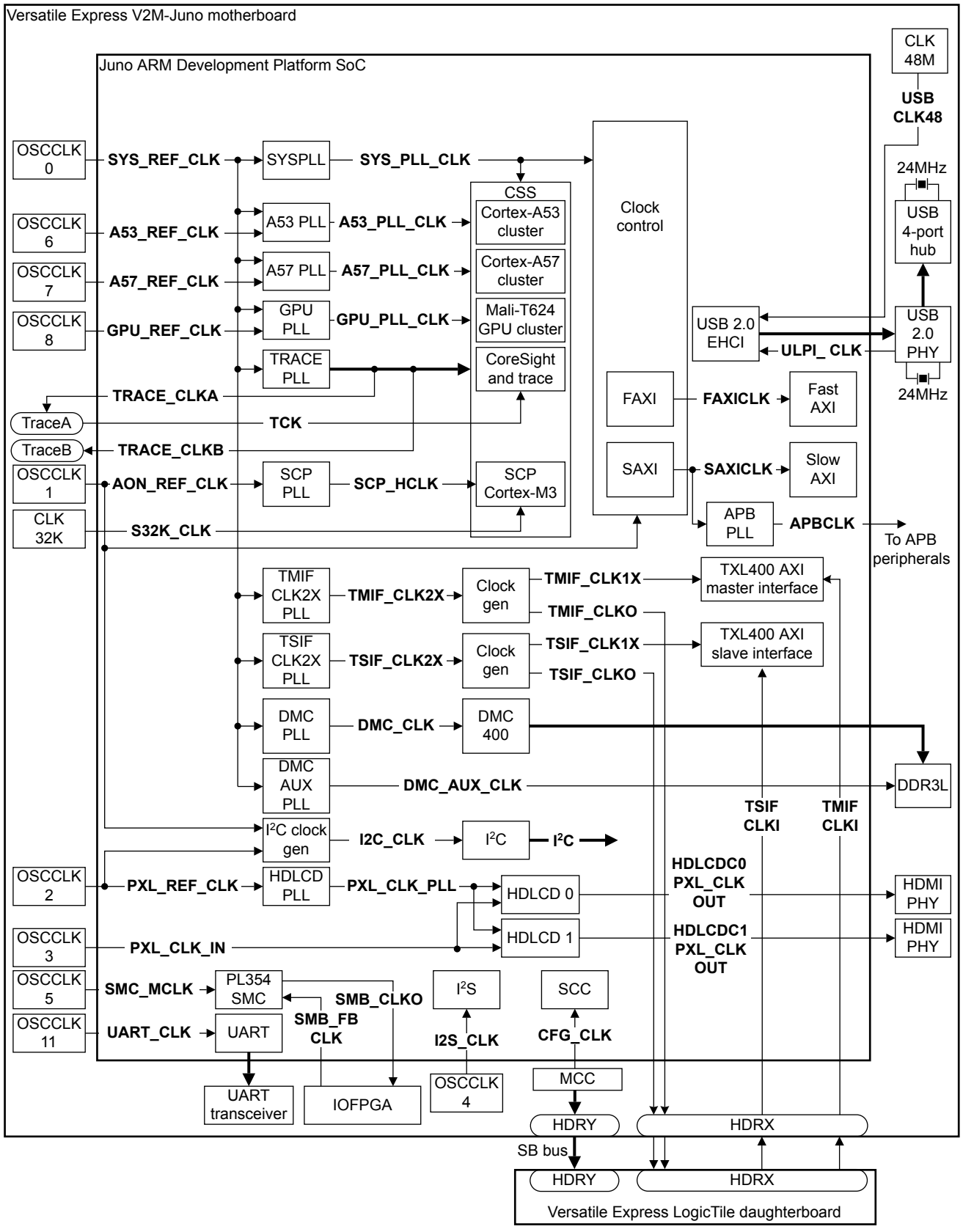

Figure 2-4 Juno ARM Development Platform SoC system clocks

The *Compute Subsystem* (CSS) is the subsystem that contains the clusters and System Control Processor (SCP).

The following table shows the internal Juno SoC and V2M-Juno motherboard clocks and their sources.

Table 2-1 Juno SoC clocks and their sources on the V2M-Juno motherboard.

Juno SoC clock	Source	Default frequency	Description
SYS_REF_CLK	OSCCLK 0	50MHz	Main system clock for the Juno SoC. Source clock for the following PLLs and clocks inside the Juno SoC: **SYS_PLL_CLK**: CSS main system clock. 1600MHz. **A57_PLL_CLK**: Cortex-A57 clock. 600MHz-1.2GHz. **A53_PLL_CLK**: Cortex-A53 clock. 500MHz-1GHz. **GPU_PLL_CLK**: Mali-T624 GPU clock. 450-900MHz. **DMC_CLK**: DMC-400 clock. 400MHz. **DMC_AUX_CLK**: External DMC interface on V2M-Juno motherboard clock. 800MHz. **FAXICLK**: Fast AXI clock. 533MHz. **SAXICLK**: Slow AXI clock. 400MHz. **USBHCLK**: Primary clock for the BIU of the USB EHCI and OHCI host controllers. 160MHz. **TMIF_CLK2X**: AXI master interface reference clock in the forward direction. 123MHz. **TSIF_CLK2X**: AXI slave interface reference clock in the reverse direction. 123MHz. **APBCLK**: Clocks the SMB_CLK domain in the IOFPGA. 100MHz. **TRACE_CLKA, TRACE_CLKB**: 145.45MHz.
AON_REF_CLK	OSCCLK 1	50MHz	Reference clock for the SCP PLL inside the Juno SoC. This derives the following clock: **SCPHCLK**: SCP subsystem and AHB expansion area clock. 25MHz-100MHz.Alternative source for **FAXICLK** and **SAXICLK**.

Table 2-1 Juno SoC clocks and their sources on the V2M-Juno motherboard. (continued)

Juno SoC clock	Source	Default frequency	Description
PXL_CLK_IN	OSCCLK 3	50MHz	Default source clock for HDLCD0 and HDLCD1. Used for low resolution displays.
PXL_REF_CLK	OSCCLK 2	50MHz	Reference clock for the HDLCD PLL inside the Juno SoC. This generates the following clock: **PXL_CLK_PLL**: 25-100MHz. This is the alternative source clock for the HDLCDs. ——— **Note** ——— You can independently select **PXL_CLK_PLL** as the source clock to HDLCD0, HDLCD1, or both. ———
HDLCDC0_PXL_CLK_OUT	HDLCD0 in Juno SoC	165MHz	Pixel clock to HDMI PHY 0 on the V2M-Juno motherboard. The maximum operating frequency of the PHY is 165MHz.
HDLCDC1_PXL_CLK_OUT	HDLCD1 in Juno SoC	165MHz	Pixel clock to HDMI PHY 1 on the V2M-Juno motherboard. The maximum operating frequency of the PHY is 165MHz.
A57_REF_CLK	OSCCLK 7	50MHz	Alternative reference clock for the A57PLL inside the Juno SoC. This PLL generates the following Cortex-A57 cluster clock: **A57_PLL_CLK** 800MHz nominal, 1.1GHz overdrive.
A57_REF_CLK	OSCCLK 7	50MHz	Alternative reference clock for the A57PLL inside the Juno SoC. This PLL generates the following Cortex-A57 cluster clock: **A57_PLL_CLK** 800MHz nominal, 1.1GHz overdrive.
A53_REF_CLK	OSCCLK 6	50MHz	Alternative reference clock for the A53PLL inside the Juno SoC. This generates the following Cortex-A53 cluster clock: **A53_PLL_CLK**: 700MHz nominal, 850MHz overdrive.
GPU_REF_CLK	OSCCLK 8	50MHz	Alternative reference clock for the GPUPLL inside the Juno SoC. This derives the following Mali-T624 GPU cluster-specific clock: **GPU_PLL_CLK**: 600MHz nominal. No overdrive.
S32K_CLK	CLK_32K clock generator	32.768kHz	Fixed frequency real-time clock. Provides a real-time private time domain for the SCP that uses it to implement very low-power sleep modes.

Table 2-1 Juno SoC clocks and their sources on the V2M-Juno motherboard. (continued)

Juno SoC clock	Source	Default frequency	Description
I2S_CLK	OSCCLK 4	75MHz	Integrated-IC sound clock. Clocks the I^2S audio bus.
I2C_CLK	OSCCLK 1 or OSCLK 2	50MHz	Clocks the I^2C control bus. ——— **Note** ——— The default input to the I^2C clock generator is OSCCLK 1. ———
UART_CLK	OSCCLK 11	7.2738MHz	Clocks the UART interface.
TCK	Trace connector	25MHz	From external trace port analyzer. Clocks the Trace debug system.
ULPI_CLK	USB2 2.0 xtal clock generator.	60MHz	Fixed frequency clock. Clocks the *USB 2.0 Transceiver Macrocell Interface Low-Pin Interface* (ULPI) from the off-chip PHY.
USB_CLK48	CLK_48M clock generator.	48MHz	Primary clock input to the USB controller.
SMC_MCLK	OSCLK 5	50MHz	Clocks the PL354 *Static Memory Controller* (SMC) interface.
SMB_FB_CLK	IOFPGA	50MHz	Feedback clock from IOFPGA to read data back into PL354 in synchronous mode. SMC uses this to adjust timing.
SMB_CLKO	OSCLK 5	50MHz	Derived from **SMC_MCLK**. Exported out of Juno SoC to SMB timing adjust block in IOFPGA.
CFG_CLK	MCC.	10MHz	Serial Configuration Controller (SCC) serial interface clock.
TMIF_CLKI	TLX400 Thin Links AXI slave interface in FPGA on LogicTile fitted in daughterboard site.	61.5MHz	Clock in the receive direction to the TLX400 Thin Links AXI master interface on the Juno SoC.
TMIF_CLKO	TLX400 Thin Links AXI master interface reference clock generator in Juno SoC.	61.5MHz	Clock in the transmit direction from the TLX400 Thin Links AXI master interface on the Juno SoC.

Table 2-1 Juno SoC clocks and their sources on the V2M-Juno motherboard. (continued)

Juno SoC clock	Source	Default frequency	Description
TSIF_CLKI	TLX400 Thin Links AXI master interface in FPGA on LogicTile fitted in daughterboard site.	61.5MHz	Clock in the receive direction to the TLX400 Thin Links AXI slave interface on the Juno SoC.
TSIF_CLKO	TLX400 Thin Links AXI slave interface reference clock generator in Juno SoC.	61.5MHz	Clock in the transmit direction from the TLX400 Thin Links AXI slave interface on the Juno SoC.

The MCC uses the `board.txt` configuration file in the microSD card to set the frequency of the board clock generators. You can adjust these default clock frequencies by editing this file. You can also adjust the board clocks during runtime by using the SYS_CFG register interface.

The Juno SoC has internal PLLs and clock generators that generate clocks to drive the Juno SoC internal systems.

See the *Juno ARM® Development Platform SoC Technical Reference Manual* for more information on the following:

- The Juno SoC internal clocks and their default values.
- Selecting alternative source clocks.

2.5.3 IOFPGA clocks

The following figure shows the IOFPFA clocks and clock domains.

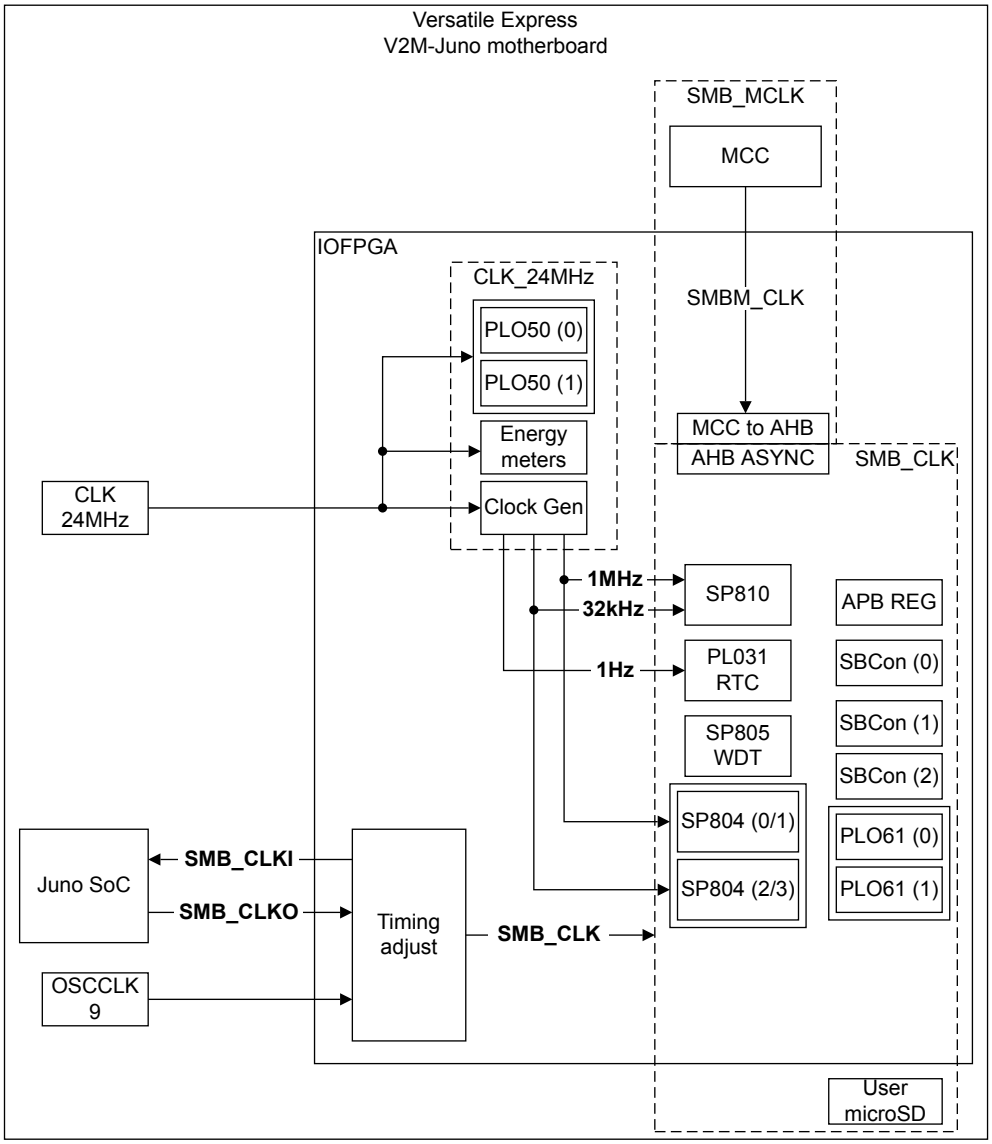

Figure 2-5 IOFPGA clocks

The bootup clock for the peripherals in the *SMB_CLK* domain during powerup and configuration is *OSCCLK 9* on the V2M-Juno motherboard. The clock source then switches to **SMB_CLKO** from the Juno SoC that becomes the master clock for the *SMB_CLK* domain during runtime.

Table 2-2 V2M-Juno motherboard OSCCLK clock sources

Clock name	Source	Default Frequency	Description
SMB_CLK	OSCCLK 9 during powerup and configuration **SMB_CLKO** during runtime	50MHz	Reference clock for the *SMB_CLK* domain. This domain contains the following IOFPGA peripherals and subsystems: • AHB subsystem. • APB subsystem. • PL031 Real-Time Clock. • APB system registers. • System Bus Controllers (SBCon). • SP805 Watchdog Timer. • SP804 Dual-Timers. • PL061 GPIO. • SP810 System Controller.
CLK_24MHZ	CLK_24MHZ clock generator.	24MHz fixed frequency	Reference clock for the following blocks inside the *SMB_CLK* clock domain: • PL050 Keyboard and mouse interfaces. • Energy meters, that is the voltage, current, power and accumulated energy meters. • The clock generator that generates the source clocks **32kHz** and **1MHz** for the SP810 System controller and the **1Hz** clock for the PL031 Real-Time Clock. **Note** — The SP810 System Controller selects **32kHz** or **1MHz** as the clock source for the SP805 and the SP804 blocks. — The frequency of the clock **32kHz** is 32.768kHz.
SMB_MCLK	MCC	50MHz	Master clock for the *SMB_MCLK* domain. The *SMB_MCLK* domain includes the MCC and the MCC to AHB fabric in the IOFPGA.

2.6 Resets

This section describes the reset push buttons, the reset architecture, and the reset timing sequence.

This section contains the following subsections:

2.6.1 Reset push buttons

The V2M-Juno motherboard provides two reset push buttons.

Hardware Reset push button

- Pressing the *Hardware Reset* button during runtime generates **nPBRESET**, performs a hardware reset and puts the system into standby state.

Note

The *Hardware Reset* push button is the black push button. The V2M-Juno motherboard labels it as *nPBRESET*.

ON/OFF/Soft Reset push button

- Pressing the *ON/OFF/Soft Reset* button briefly during runtime performs a software reset of the system.
- Pressing the *ON/OFF/Soft Reset* for more than two seconds puts the system into the standby state in the same way as pressing the *Hardware Reset* button.

Note

The *ON/OFF/Soft Reset* push button is the red push button. The V2M-Juno motherboard labels it as *nPBON*.

Related concepts

3.5.1 ON/OFF/Soft Reset button on page 3-75.

3.5.2 Hardware Reset button on page 3-75.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

2.6.2 Reset architecture

The following figure shows an overview of the V2M-Juno motherboard reset system.

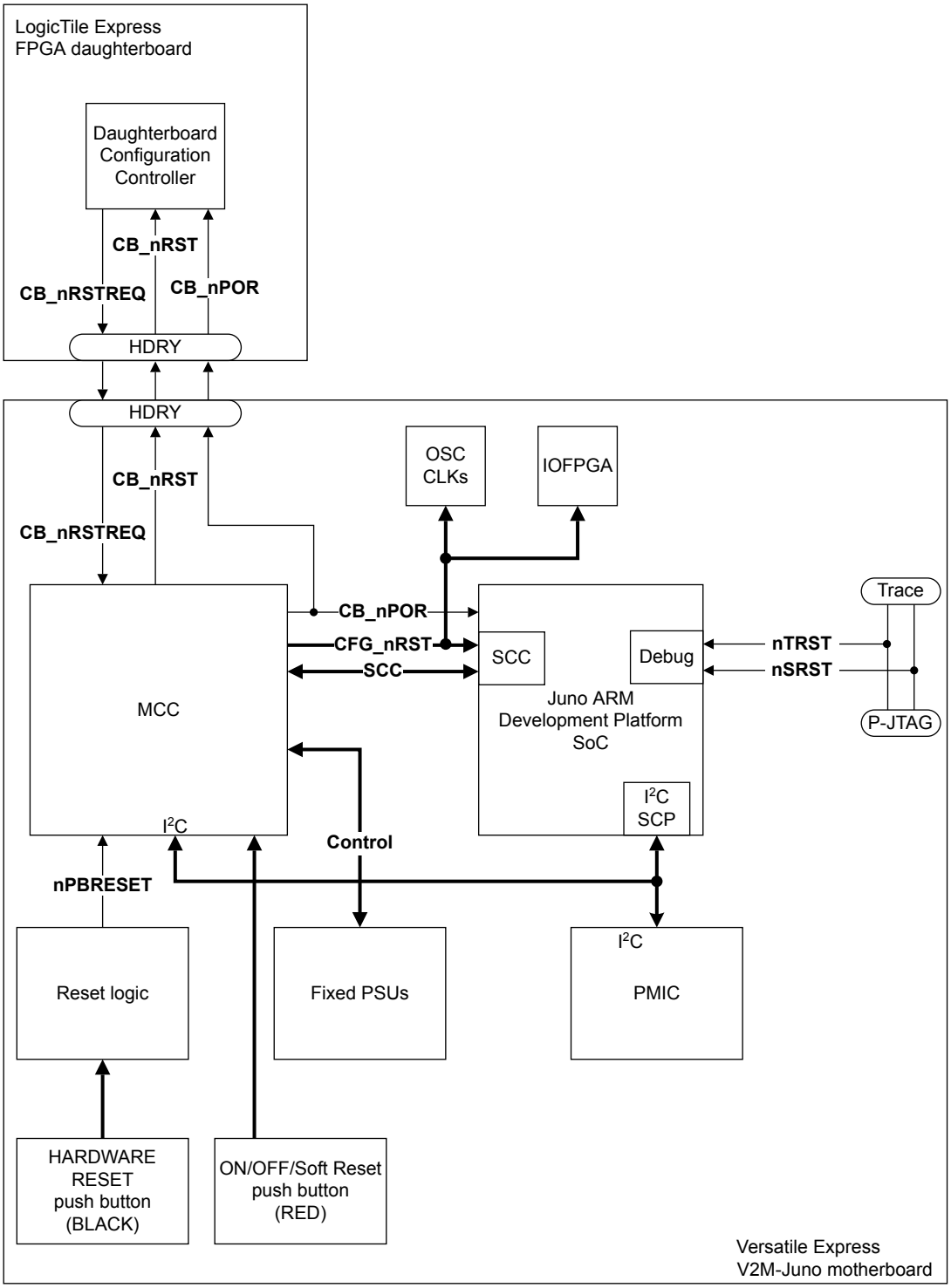

Figure 2-6 V2M-Juno motherboard resets

CB_nPOR

This is the main powerup reset for the Juno ARM Development Platform SoC, and the devices and peripherals on the V2M-Juno motherboard including the IOFPGA. Signal **CB_nPOR** drives signal **nPORESET** inside the Juno ARM Development Platform SoC.

nTRST

This resets the CoreSight DAP and the TAP controllers inside theJuno SoC.

CFG_nRST

This is the reset signals for the serial interface to the SCC registers in the Juno ARM Development Platform SoC. It resets the SCC registers to their default values. It also resets the IOFPGA peripherals and the clock generators on the V2M-Juno motherboard.

2.6.3 Reset sequence

The following figure shows the reset and configuration timing sequence.

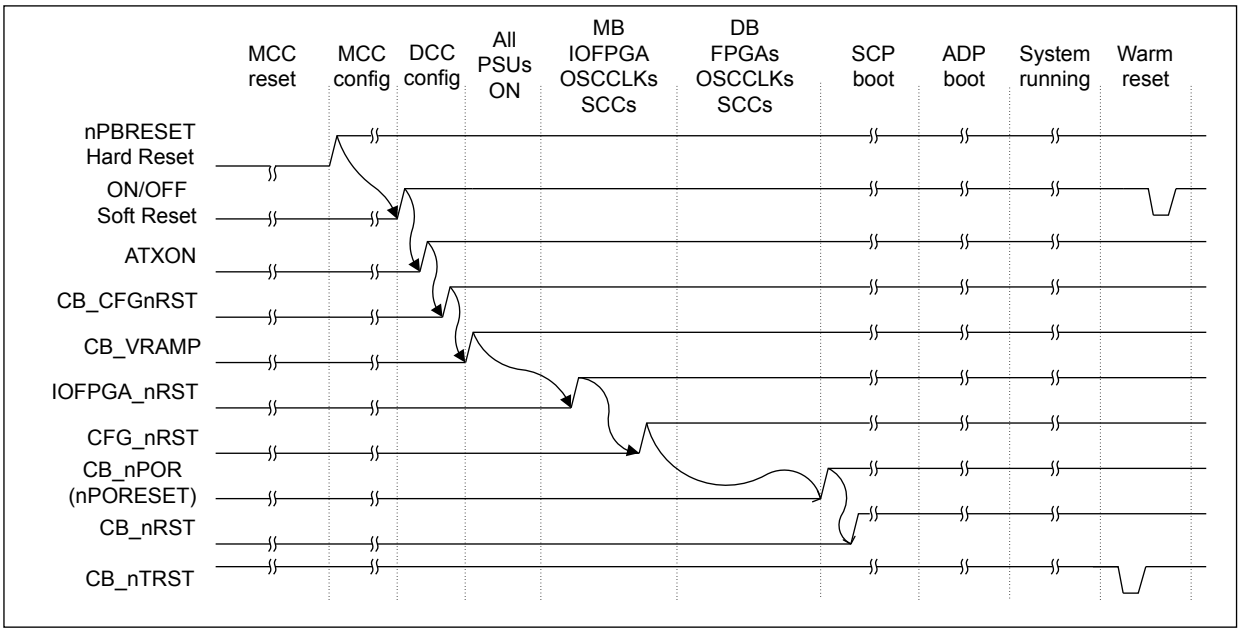

Figure 2-7 V2M-Juno motherboard reset and configuration timing cycle

2.7 Thin Links AXI master and slave interfaces

The Juno ARM Development Platform SoC contains one AXI master interface and one slave AXI interface that connect to the FPGA in the LogicTile Express daughterboard. A Thin Links TLX-400 interface compresses the AXI master and slave interfaces to reduce the pin count.

The width of the TLX-400 slave interface on the Juno ARM Development Platform SoC is greater than the width of the master interface.

The default Thin Links clock frequency of 61.5MHz gives the following operating speeds:

- Juno SoC master interface:
  - Forward direction, that is, from the Juno SoC to the FPGA: 68Mbps.
  - Reverse direction, that is, from the FPGA to the Juno SoC: 78Mbps.
- Juno SoC slave interface:
  - Forward direction, that is, from FPGA to Juno SoC: 246Mbps.
  - Reverse direction, that is, from Juno SoC to FPGA: 305Mbps.

Note

ARM recommends that you operate the Thin Links interfaces at the default speeds. See *3.3.4 Contents of the SITE1 directory* on page 3-71 for an example `board.txt` configuration file that sets the Thin Links clocks to 61.5MHz.

The following figure shows the Thin Links TXL-400 master interface on the Juno ARM Development Platform SoC and its connection to the Think Links TXL-400 slave interface on the LogicTile Express daughterboard.

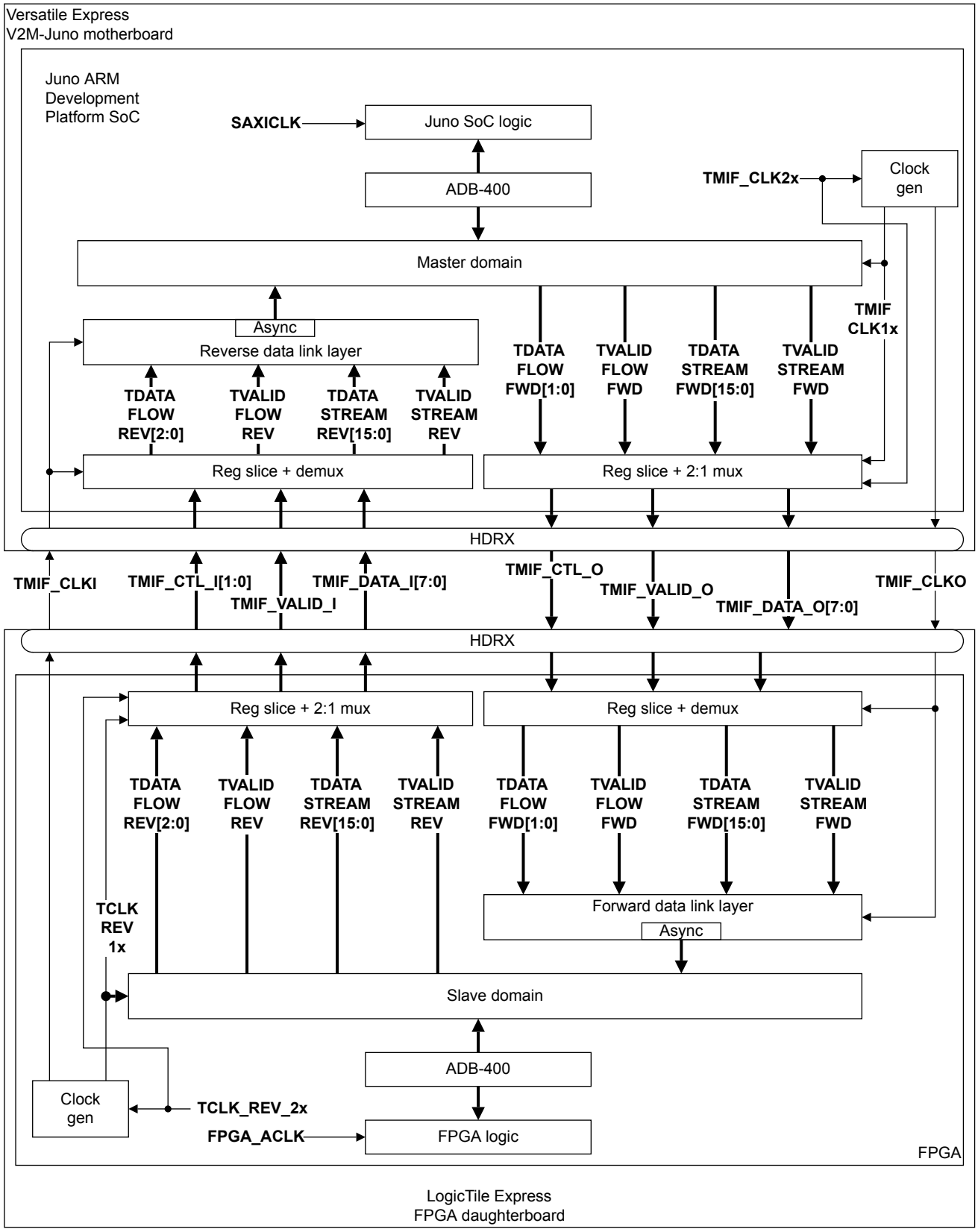

Figure 2-8 Thin Links AXI master interface

The following figure shows the Thin Links TXL-400 slave interface on the Juno ARM Development Platform SoC and its connection to the Think Links TXL-400 master interface on the LogicTile daughterboard.

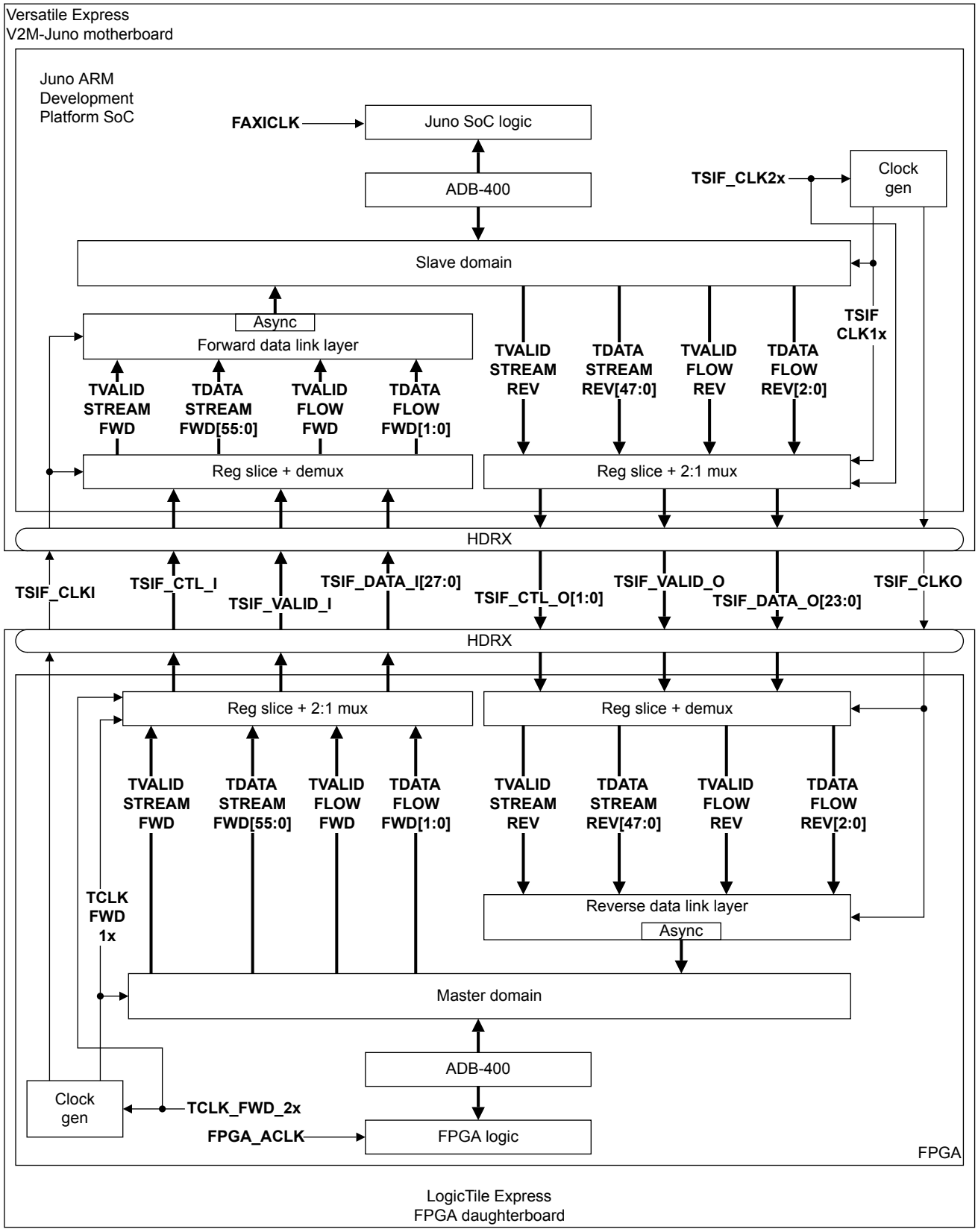

Figure 2-9 Thin Links AXI slave interface

2.8 IOFPGA

The IOFPGA provides access to low bandwidth peripherals that the Juno ARM Development Platform SoC does not provide. The Juno ARM Development Platform SoC provides access to the IOFPGA through an SMC interface.

The following figure shows the internal architecture of the IOFPGA and its connectivity to external peripherals, including the external interrupts to the GIC-400 interrupt controller in the Juno ARM Development Platform SoC.

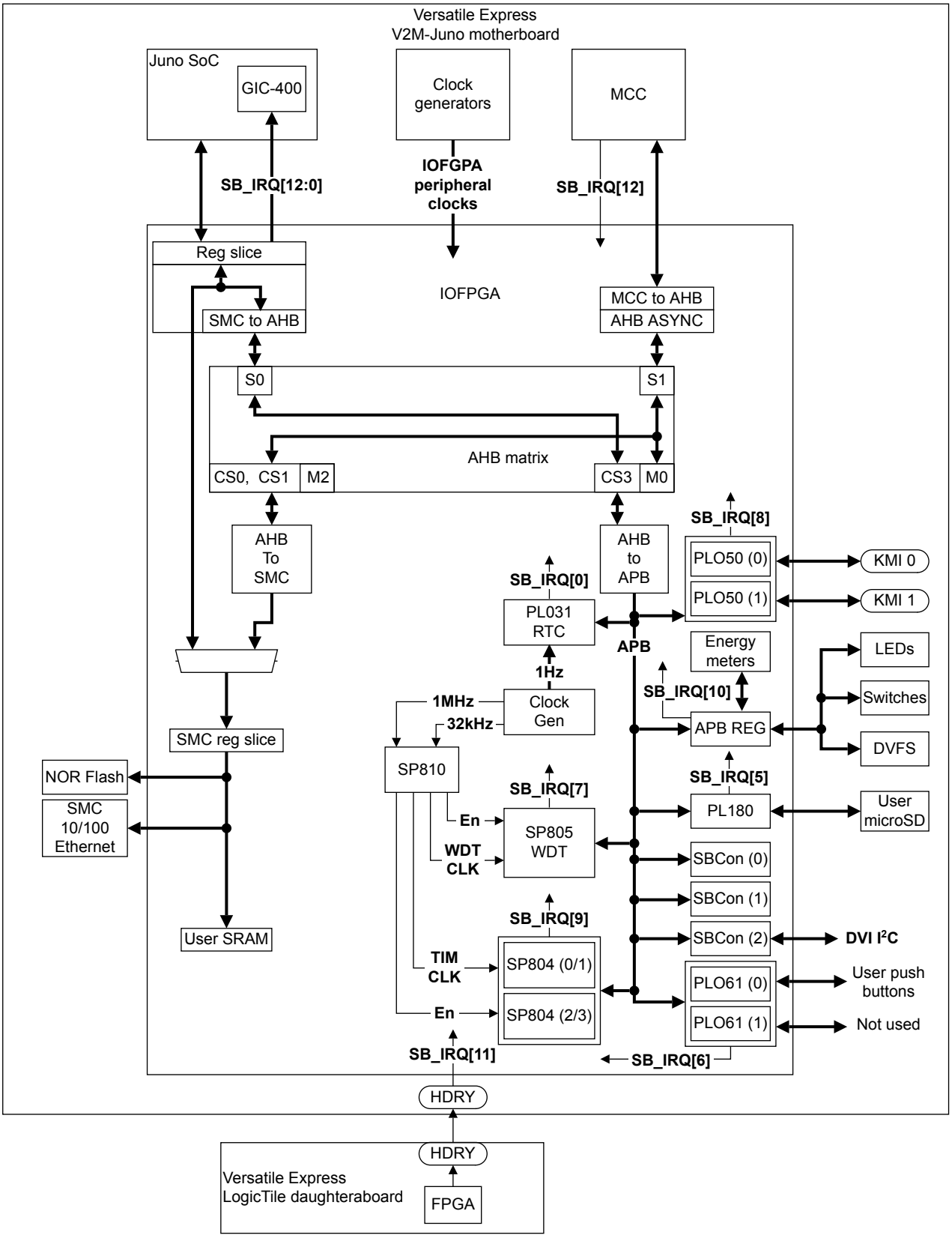

Figure 2-10 IOFPGA internal architecture

The following table shows the peripherals and buses inside the IOFPGA.

Peripheral	Interface or application	Release version
PL031	RTC.	r1p0.
PL050	Keyboard and mouse interfaces.	r1p0.
PL061	GPIO for additional user key entry and trusted keyboard entry.	r1p0.
SP804	Dual-timer.	r1p2.
SP805	Watchdog Timer.	r2p0.
PL350 Series	SMC Controller.	r1p0.
AHB bus	-	AMBA 3 AHB-Lite Protocol Specification v1.0.
APB bus	-	AMBA 3 APB Protocol Specification v1.0.

Note

The peripheral versions apply to the Revision B V2M-Juno motherboard.

Related concepts

4.2.2 IOFPGA system peripherals memory map on page 4-83.

2.9 HDLCD interface

Two HDMI PHYs on the V2M-Juno motherboard provide video graphics.

Two HDLCD controllers in the Juno ARM Development Platform SoC support all common 24-bit RGB formats. These are simple frame buffers whose RGB video connects to IO drivers that drive the PHYs. The PHYS can operate at a maximum pixel clock frequency of 165MHz. This interface supports HDMI 1.4a up to 1080p.

There are two clock sources for the pixel clocks on the V2M-Juno motherboard:

- OSCCLK 2 is the source clock for HDLCD PLL that generates **PXL_CLK_PLL**.
- OSCCLK 3 is the source clock for **PXL_CLK_IN**.

Note

You can independently select **PXL_CLK_IN** or **PXL_CLK_PLL** during runtime as the clock source for HDLCD 0 or HDLCD 1.

A typical use of HDLCD0 is for lower resolution video than HDLCD1 and to be clocked directly from **PXL_CLK_IN** without using the PLL.

The HDLCD 24-bit data connects directly between the Juno ARM Development Platform SoC and the HDMI controllers on the V2M-Juno motherboard. The HDMI controllers drive the HDMI connectors. The Juno ARM Development Platform SoC configures the HDMI controllers at powerup or reset over the AP I^2C bus.

The HDMI controllers support I^2S audio from the Juno ARM Development Platform SoC. They drive the audio to the HDMI connectors.The same audio stream connects to both HDMI connectors.

Note

Software that ARM supplies with the V2M-Juno motherboard configures the Juno SoC and board to enable correct operation of the HDLCD interface and correct HDMI output.

The following figure shows the HDLCD video system on the V2M-Juno motherboard.

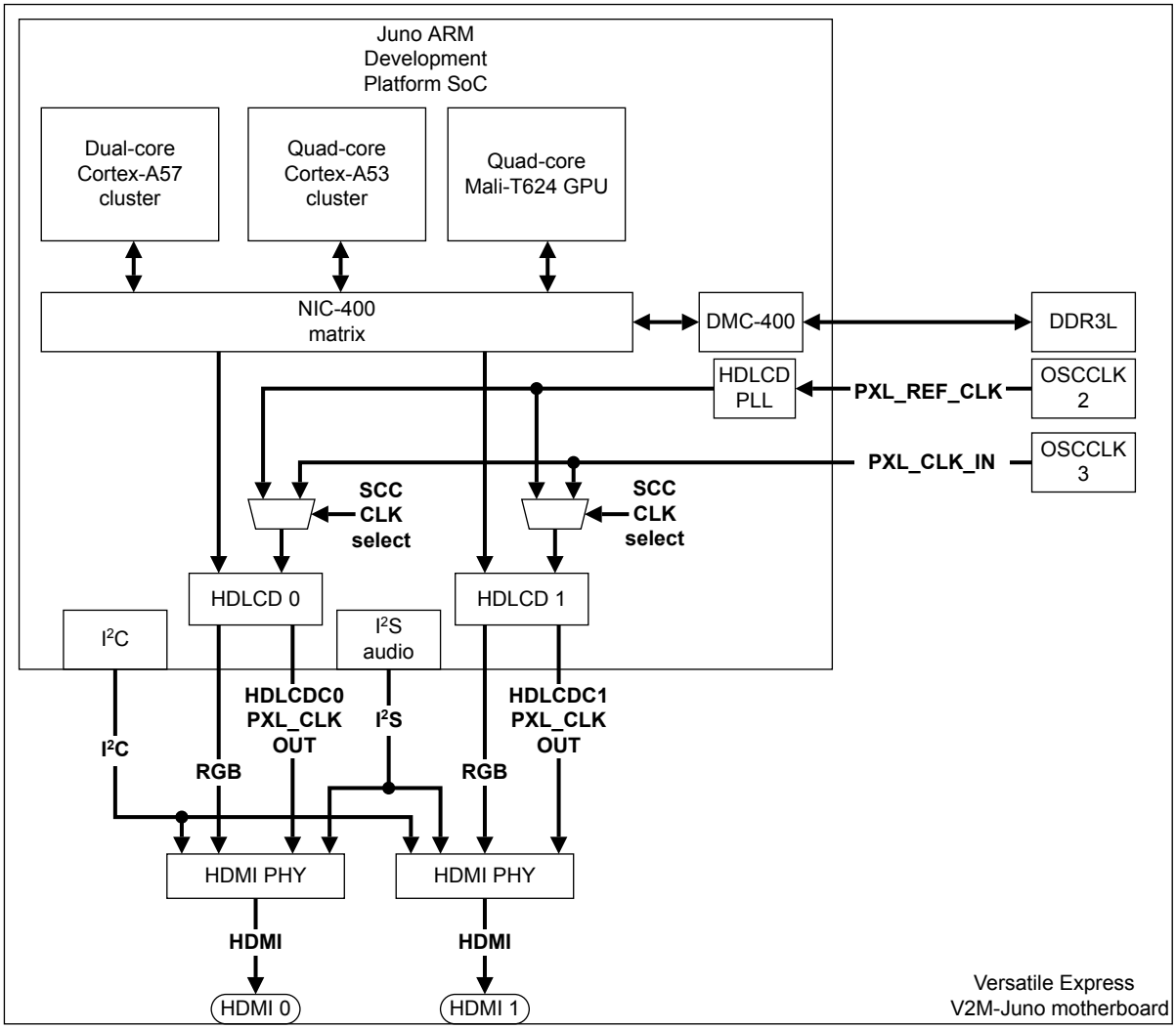

Figure 2-11 V2M-Juno motherboard HDLCD interface

The default clock for the HDLCD controllers is **PXL_CLK_IN**. See the Juno ARM Development Platform SoC Technical Reference Manual for information on the following:

- The Juno SoC internal clocks and their default values.
- Selecting alternative source clocks.

Related references

A.1.8 HDMI connectors on page Appx-A-125.

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

2.10 Interrupts

The Juno ARM Development Platform SoC implements a GIC-400 generic interrupt controller with 13 external interrupts.

•

Seven of the external interrupts connect to IOFPGA peripherals, one connects to the SMC 10/100 Ethernet, one connects to the MCC, and one connects to the LogicTile daughterboard site. The other three external interrupts are reserved.

Note

The prototype board provides an SMC USB 2.0 interface that the production board does not provide. The SMC USB 2.0 uses one of the reserved interrupts leaving two external interrupts as reserved on the prototype board.

The MCC generates its interrupt when you press the *ON/OFF/Soft Reset* push button. All interrupts connect to the GIC-400 interrupt controller in the Juno ARM Development Platform SoC through the IOFPGA.

The following figure shows an overview of the external interrupt signals from the V2M-Juno motherboard peripherals to the GIC-400 interrupt controller in the Juno ARM Development Platform SoC.

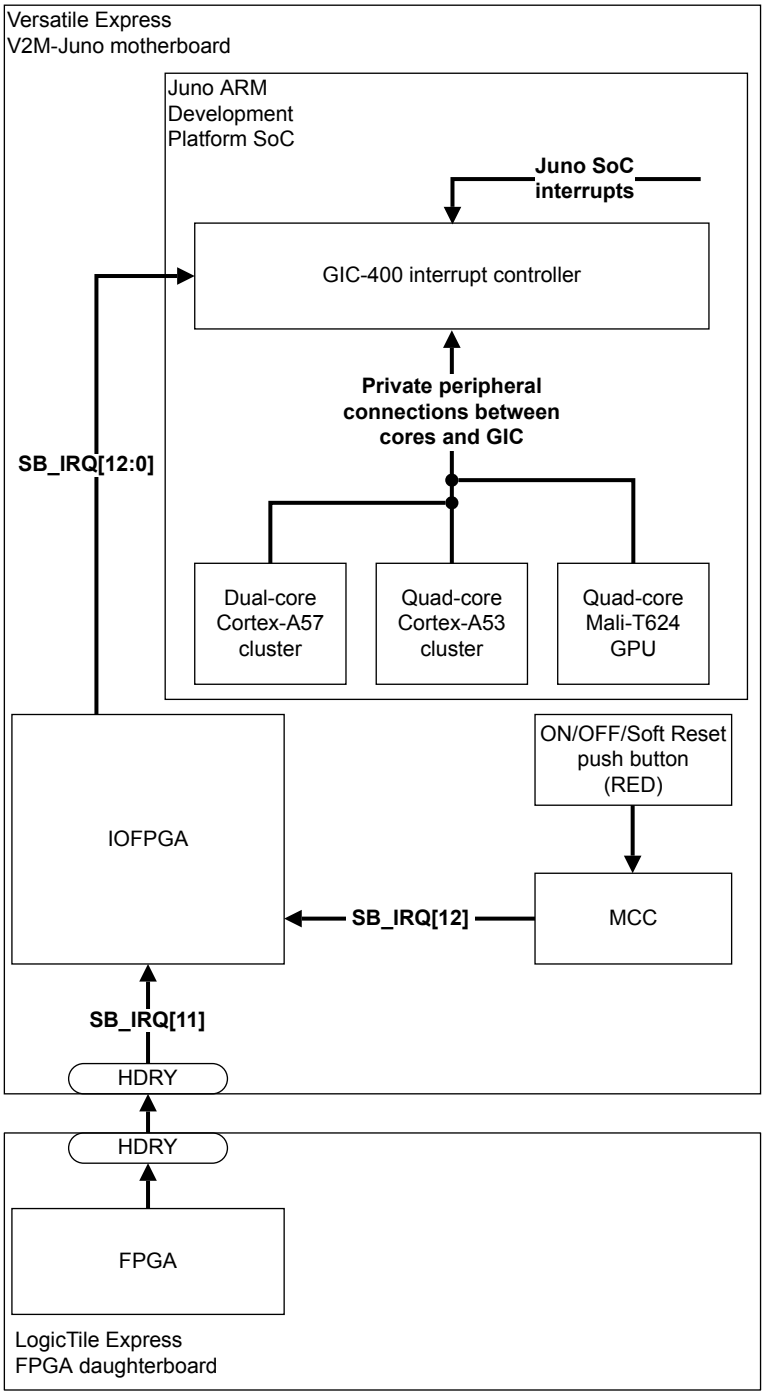

Figure 2-12 Juno ARM Development Platform SoC interrupts overview

The following table shows the mapping of the external interrupt signals to the GIC-400 controller in the Juno ARM Development Platform SoC. It lists the sources of the interrupts that originate in the V2M-Juno motherboard or the LogicTile Express fitted in the daughterboard site.

Table 2-3 External interrupt signals to V2M-Juno Arm Development Platform

Interrupt ID	GIC IRQ ID	Motherboard signal name	Source
99-96	67-64	-	Juno ARM Development Platform SoC internal peripherals and systems.
100	68	**SB_IRQ[0]**	IOFPGA-PL031 RTC.
102-101	70-69	**SB_IRQ[2:1]**	IOFPGA-Reserved interrupts.
191-103	159-71	-	Juno ARM Development Platform SoC internal peripherals and systems.
192	160	**SB_IRQ[3]**	IOFPGA-SMC 10/100 Ethernet.
193	161	**SB_IRQ[4]**	• Prototype board: — IOFPGA-SMC USB 2.0. • Production board: — IOFPGA-Reserved interrupt.
194	162	**SB_IRQ[5]**	IOFPGA-PL180 user microsSD card.
195	163	**SB_IRQ[6]**	IOFPGA-PL061 GPIO (0) and GPIO (1) used for additional user key entry.
196	164	**SB_IRQ[7]**	IOFPGA-SP805 WDT.
197	165	**SB_IRQ[8]**	IOFPGA-PL050 KMI interface.
198	166	**SB_IRQ[9]**	IOFPGA-SP804 Dual-timer (0-1) and SP804 dual-timer (2-3).
199	167	**SB_IRQ[10]**	IOFPGA:APB system registers from SYS_MISC[SWINT] Register.
200	168	**SB_IRQ[11]**	LogicTile FPGA daughterboard. Interrupt from FPGA on LogicTile daughterboard.
201	169	**SB_IRQ[12]**	MCC-Interrupt generated by pressing the *ON/OFF/Soft Reset* push button.
223-202	191-170	-	Juno ARM Development Platform SoC internal peripherals and systems.

Note

See the *Juno ARM® Development Platform SoC Technical Reference Manual* for information on the interrupts from the systems in the Juno ARM Development Platform SoC.

See *B.2.1 Overview of the prototype V2M-Juno motherboard* on page Appx-B-131 for information on interrupts **SB_IRQ[4:3]** on the prototype V2M-Juno motherboard.

2.11 USB 2.0 interface

The Juno ARM Development Platform SoC provides a USB 2.0 interface. The interface is capable of 480Mbps.

The host controller on the Juno ARM Development Platform SoC connects to an external PHY on the V2M-Juno motherboard. This PHY connects to a four-port hub that connects to four USB 2.0 user ports.

Each port can supply one amp to an external load.

The following figure shows the USB 2.0 system, the host controller, PHY, and hub.

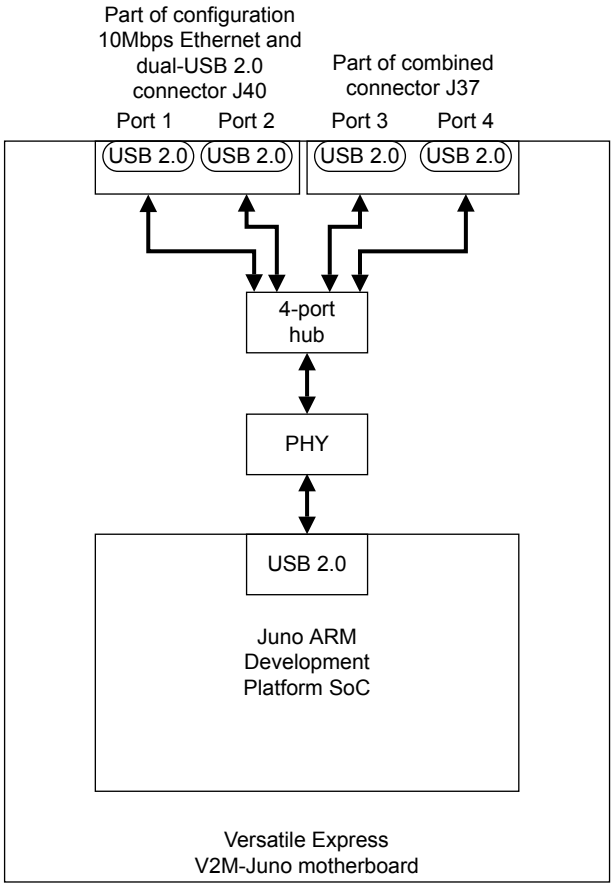

Figure 2-13 V2M-Juno motherboard USB 2.0 interface

Related references

A.1.2 Configuration 10Mbps Ethernet and dual-USB connector on page Appx-A-119.

A.1.3 Dual-USB connector on page Appx-A-120.

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

2.12 SMC 10/100 Ethernet interface

The Juno ARM Development Platform SoC provides a 10/100 Ethernet port.

The 10/100 Ethernet port connects to the *Static Memory Controller* (SMC) bus through the IOFPGA.

The following figure shows the SMC 10/100 Ethernet interface.

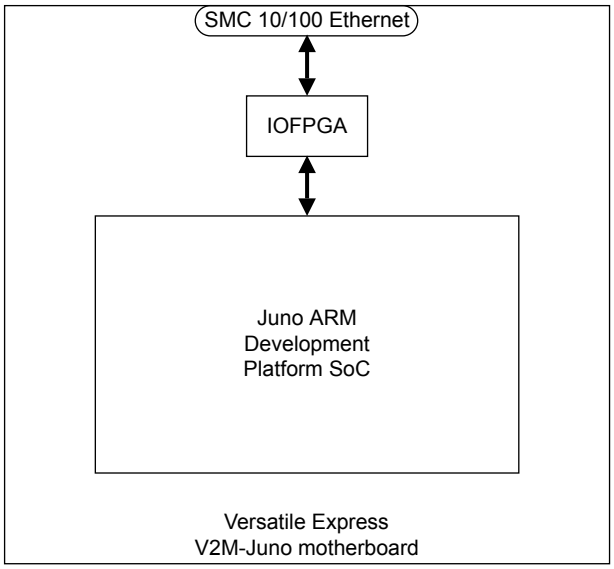

Figure 2-14 V2M-Juno motherboardSMC 10/100 Ethernet interface

2.13 UART interface

The Juno ARM Development Platform SoC provides a dual-port UART interface.

The connection of the UART 0 transceiver can be to the MCC or to the UART interface on the Juno ARM Development Platform SoC. The default connection is to the MCC at powerup and then it switches to the Juno ARM Development Platform SoC UART 0 interface.

The connection of the UART 1 transceiver can be to the Daughterboard Configuration Controller on the LogicTile daughterboard or to the UART interface on the Juno ARM Development Platform SoC. The default connection is to the Daughterboard Configuration Controller at powerup and then it switches to the Juno ARM Development Platform SoC UART 1 interface.

You can change the default UART connections by editing the `config.txt` file in the configuration microSD card. Changes to the configuration files take affect after the next reset. You set the UART 0 connection by setting the *`MBLOG`* option in the `config.txt` file to the appropriate value. You set the UART 1 connection by setting the *`DBLOG`* option in the `config.txt` file to the appropriate value.

The following figure shows the UART interface to the V2M-Juno motherboard.

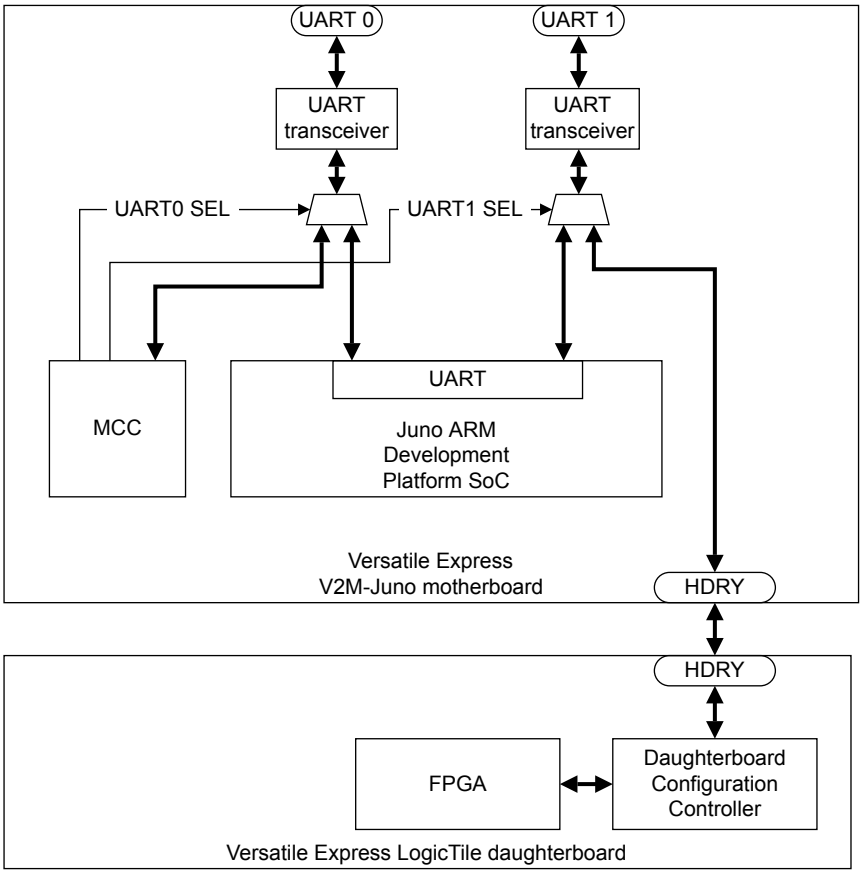

Figure 2-15 V2M-Juno motherboard UART interface

Related concepts

3.3.2 `config.txt` generic motherboard configuration file on page 3-70.

Related references

A.1.9 Dual UART connector on page Appx-A-126.

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

2.14 Keyboard and mouse interface

The V2M-Juno motherboard provides two KMI ports for PS/2 keyboard and mouse input to the system.

The keyboard and mouse inputs connect to PL050 interfaces in the IOFPGA.

The following figure shows the V2M-Juno motherboard KMI interface.

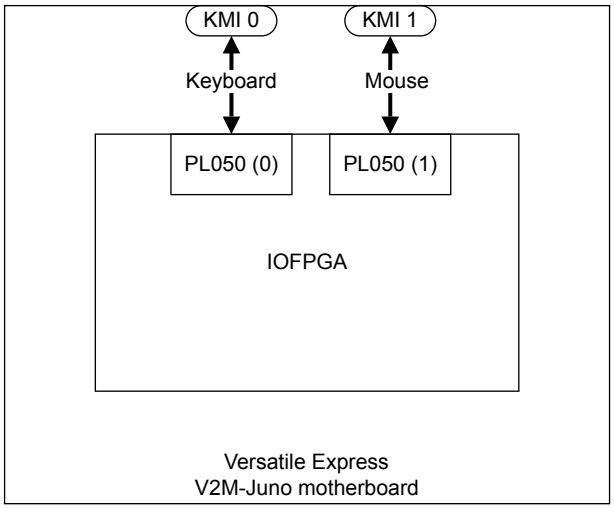

Figure 2-16 V2M-Juno motherboard KMI interface

Related references

A.1.7 Keyboard and Mouse (KMI) connector on page Appx-A-124.

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

2.15 Additional user key entry

The V2M-Juno motherboard provides two methods of additional user key entry:

- Trusted keyboard entry using the secure keyboard entry port on the Juno ARM Development Platform SoC:
  - This method requires a custom external device with decode circuitry for key entry.
  - The Juno ARM Development Platform SoC controls the trusted keyboard over a secure I^2C bus.
  - Supports touch screen display. A touch screen secure keyboard interface board with a built-in controller enables use of a resistive touch screen.
- User push buttons on the V2M-Juno motherboard that emulate hand-held devices:
  - Six push buttons. Access through IOFPGA GPIO.

A single 9-pin Mini-Din socket on the top face of the V2M-Juno motherboard provides a secure keyboard entry port for entry using an external keyboard. The following figure shows the additional user key interface and its connections to the user push buttons on the V2M-Juno motherboard.

Note

One user push button input, *NU/NMI*, to the FPGA is not available to the external secure keyboard custom device.

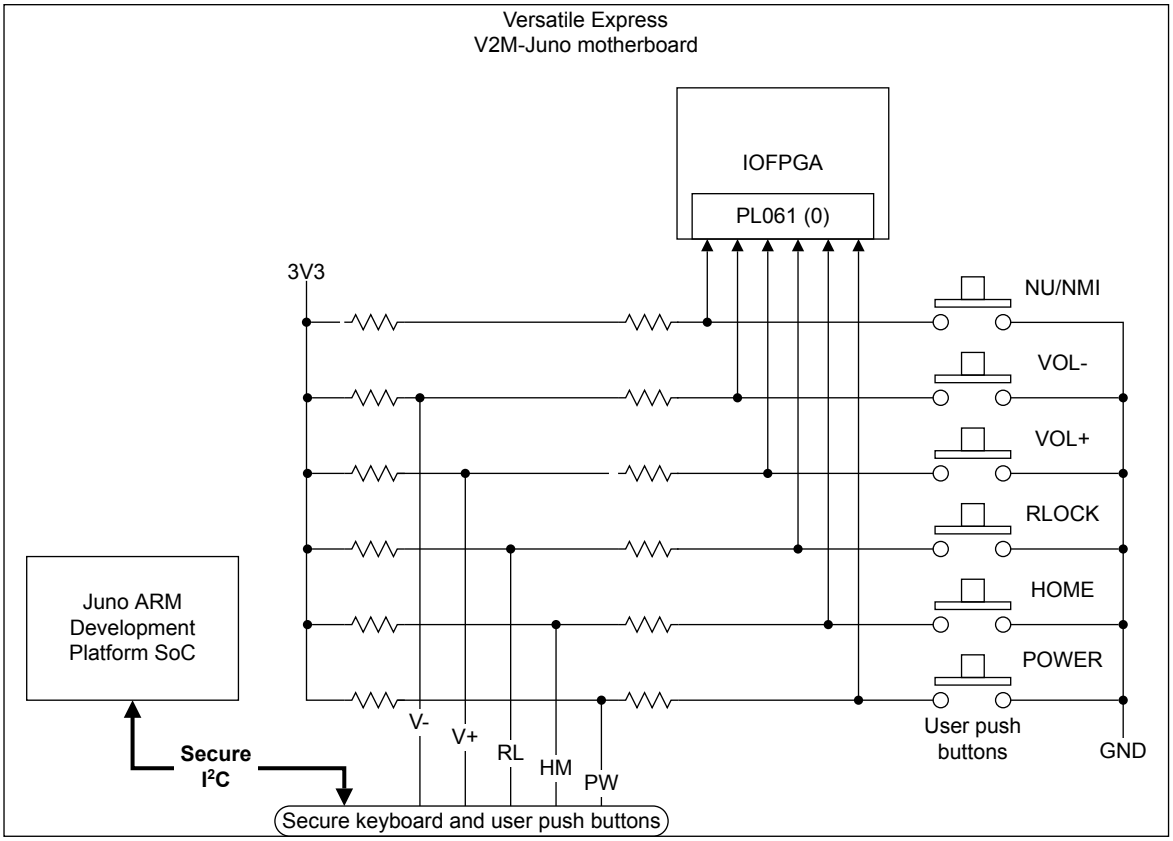

Figure 2-17 Additional user key entry interface

The following figure shows an example trusted keyboard design using an external custom device that connects to the secure keyboard entry port.

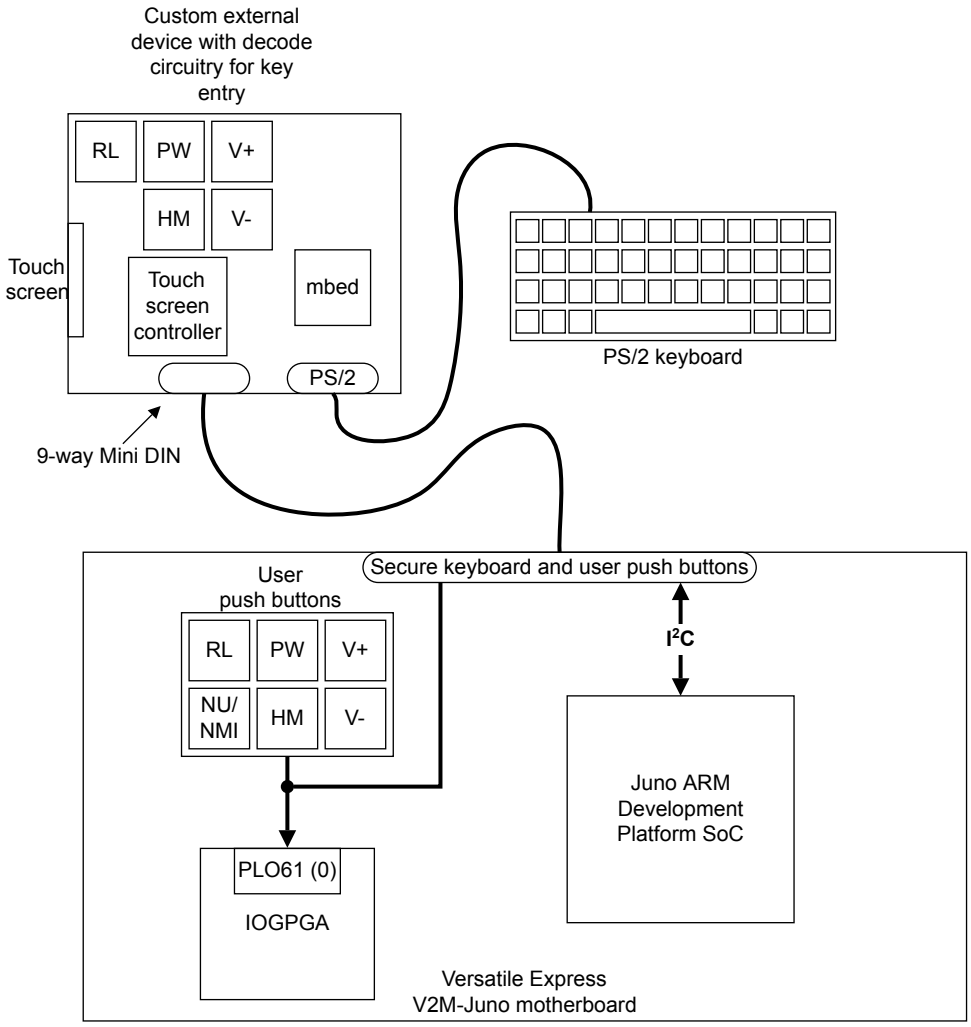

Figure 2-18 Example trusted keyboard design

Related references

A.1.10 Secure keyboard and user push buttons connector on page Appx-A-128.
1.3 Location of components on the V2M-Juno motherboard on page 1-15.

2.16 Debug and trace

The V2M-Juno motherboard supports processor debug, P-JTAG, 16-bit and 32-bit trace to enable sofware debug and trace in the Juno ARM Development Platform SoC.

You connect a debug unit to the P-JTAG connector on the V2M-Juno motherboard to run processor debug, P-JTAG.

Note

The processor debug device can be any compatible debug unit, for example DSTREAM or a compatible third-party debugger.

You connect a compatible trace port analyzer, for example DSTREAM or a compatible third-party debugger, to the *TRACEA-SINGLE* connector to run 16-bit trace or to both the *TRACEA-SINGLE* and *TRACEB-DUAL* connector to run 32-bit trace.

The following figure shows an overview of the V2M-Juno motherboard debug and trace architecture.

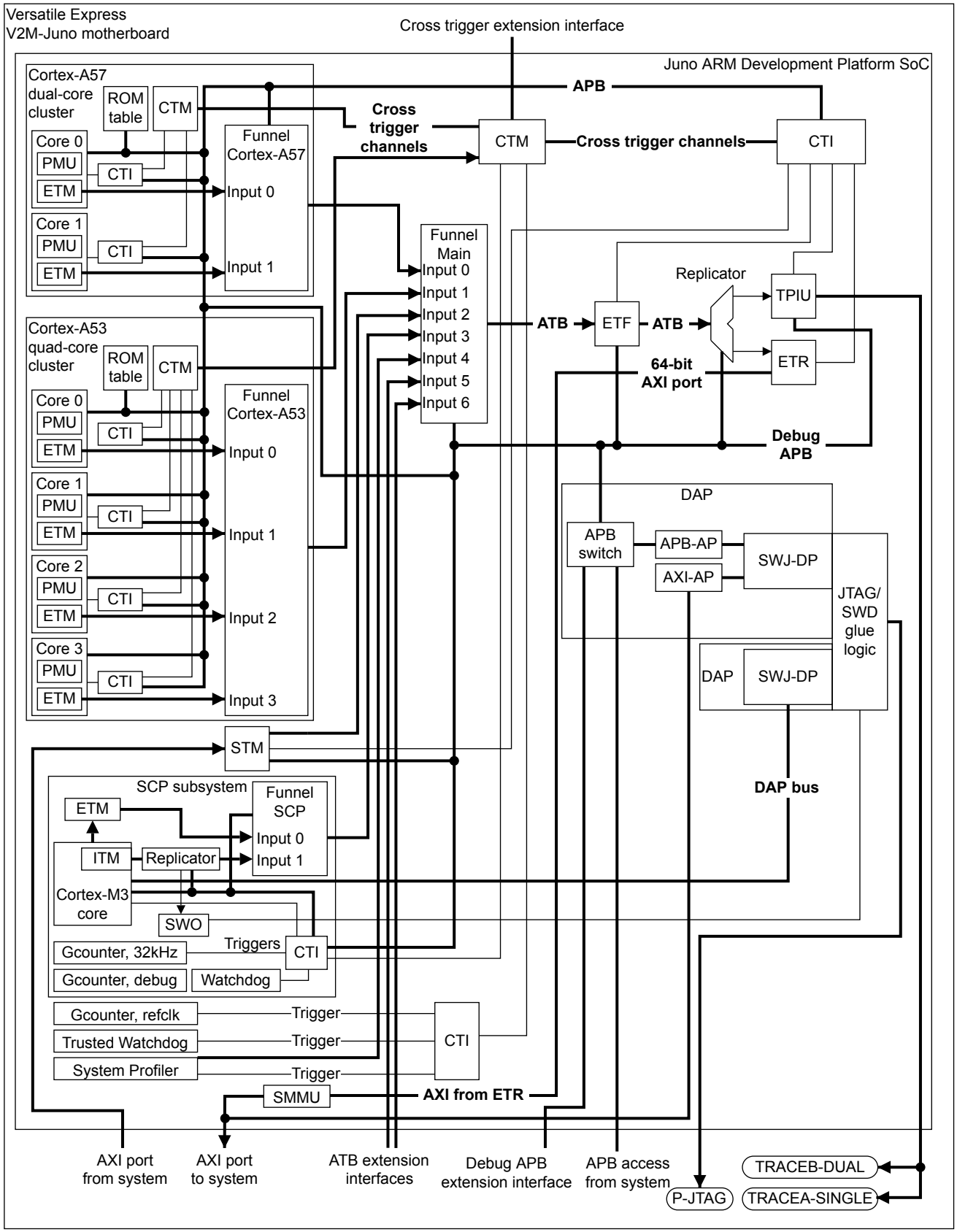

Figure 2-19 V2M-Juno motherboard debug architecture

See the *Juno ARM® Development Platform SoC Technical Reference Manual* for more information on the Juno ARM Development Platform SoC debug architecture.

Related references

P-JTAG connector on page Appx-A-115.

Trace connectors on page Appx-A-116.

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

Chapter 3
Configuration

This chapter describes the powerup and configuration process of the Versatile Express V2M-Juno motherboard.

It contains the following sections:

3.1 Overview of the V2M-Juno motherboard configuration system

The V2M-Juno motherboard provides hardware infrastructure to enable board configuration during powerup or reset. The MCC, in association with the configuration microSD card, configures the V2M-Juno motherboard during powerup or reset.

When the configuration process starts after application of power or a press of the *ON/OFF/Soft Reset* button, the configuration process completes without further intervention from the user.

The MCC controls the transitions of the V2M-Juno motherboard between the operating states in response to presses of the reset buttons or powerdown requests from the operating system.

The following figure shows the V2M-Juno motherboard configuration system.

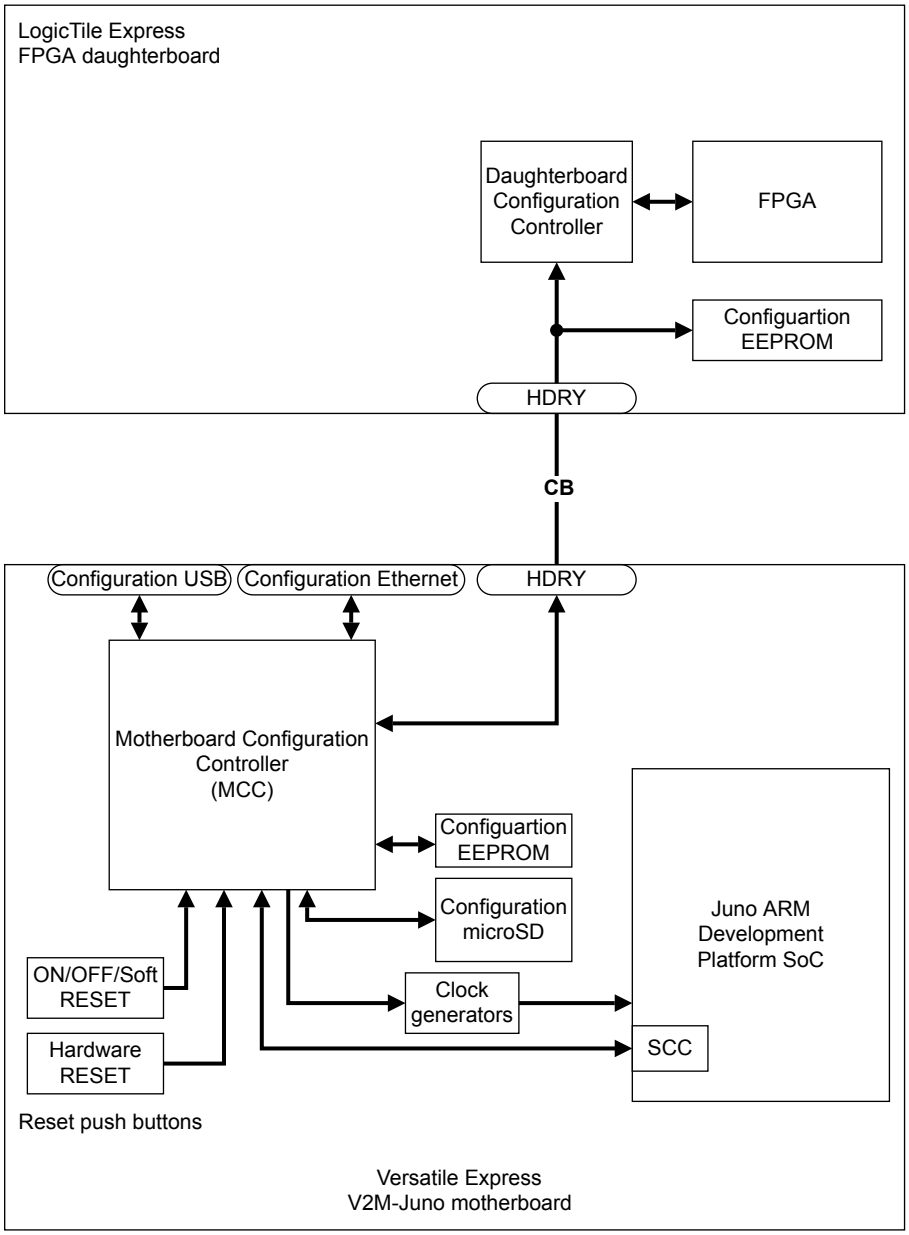

Figure 3-1 V2M-Juno motherboard configuration system

The configuration microSD card stores the V2M-Juno motherboard configuration files, including the `board.txt` file. You can access the microSD card as a *Universal Serial Bus Mass Storage Device* (USBMSD).

The MCC:

At the start of the configuration process, the MCC reads the contents of the configuration EEPROM. The EEPROM contains the following information:

- Board HBI number.
- Board revision.
- Board variant.
- Number of FPGAs.
- Names of the current images in 8.3 format and the file creation dates.
- Juno ARM Development Platform SoC calibration data.

Note

- The HBI number is a unique code that identifies the board. The root directories of the microSD card contain sub-directories in the form *HBI<BoardNumber><Boardrevision>*, for example HBI0262B. HBI0262 is the HBI number of the V2M-Juno motherboard.
- If the MCC does not find a configuration directory that matches the HBI number of the board, the configuration process fails and the board enters the standby state.

3.2 Configuration process and operating modes

This section describes the powerup and configuration process, the powerdown process and the transitions between the operating-state and the sleep-state.

This section contains the following subsections:

3.2.1 Transitions between operating modes

The power reset push buttons and configuration files control the sequence of events of the powerup and configuration process and the transitions between the different states of the V2M-Juno motherboard.

The V2M-Juno motherboard has the following operating modes:

Standby-state
: The V2M-Juno motherboard and Juno ARM Development Platform SoC are mostly powered down. The powerup and configuration sequence takes them to the operating-state.

Operating-state
: This is the full operating mode. All peripherals and clock function and application code runs. The powerdown sequence takes the board to the standby-state and the sleep-mode sequence takes it to the sleep-mode.

Sleep-state
: This state powers down the Juno ARM Development Platform SoC clusters and preserves operating data and the application code start-point. Application codes resumes when the Juno ARM Development Platform SoC returns to the operating-state.

——— **Note** ———

The system cannot return directly to the standby-state from the sleep-state. It must return to the operating-state before the powerdown sequence can begin.

———————————

The following figure shows the configuration process and the transitions between the standby-state, operating-state, and sleep-state of the V2M-Juno motherboard.

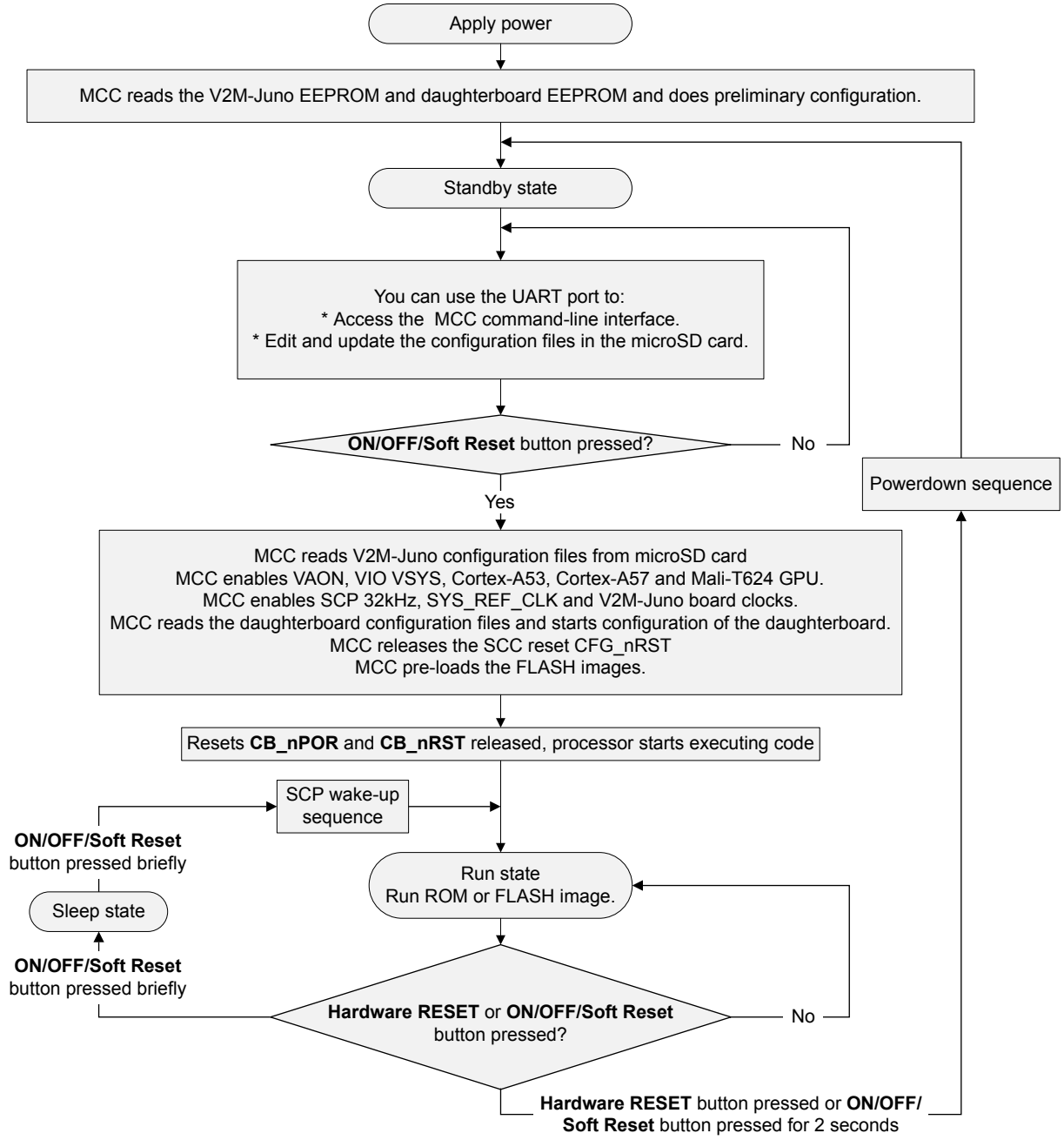

Figure 3-2 Transitions between standby-state, operating-state, and sleep-state

3.2.2 Powerup and configuration sequence

Pressing the Hardware Reset button initiates the powerup and configuration sequence and takes the V2M-Juno motherboard from the standby-state to the operating-state.

The V2M-Juno motherboard powerup and configuration sequence is:

1. The board applies power to the system.
2. The MCC powers the EEPROM on the V2M-Juno motherboard and the EEPROM on any fitted LogicTile daughterboard and reads them to determine the HBI identification codes for the boards.
3. The system enters standby-state.
4. The system enables the MCC command-line interface on the UART.

5. The system enables the configuration microSD memory card and you can connect a workstation to the configuration USB port or configuration Ethernet port to edit existing configuration files or *Drag-and-Drop* new configuration files.
6. The system stays in standby-state until you press the *ON/OFF/Soft Reset* push button or you send the `REBOOT` command to the MCC command-line interface.
7. The system loads the board configuration file:
   - The MCC reads the generic `config.txt` file.
   - The MCC searches the configuration microSD card MB directory for the V2M-Juno motherboard HBI0262x subdirectory that matches the HBI code in the EEPROM.
   - If a LogicTile daughterboard is fitted, the MCC searches the configuration microSD card SITE2 directory for a subdirectory that matches the HBI code in the fitted LogicTile EEPROM.
8. The next steps depend on the configuration files:
   - If the MCC finds configuration subdirectories that match the HBI code of the V2M-Juno motherboard and any fitted LogicTile daughterboard, configuration continues and the MCC reads the daughterboard `board.txt` file.
   - If the MCC does not find the correct configuration files, it records the failure to a log file on the configuration microSD card. Configuration stops and the system re-enters standby-state.
9. The MCC switches on the ATX PSU and power domains in the Juno SoC using the board power controller PMIC.
10. The MCC enables the SCP 32kHz clock, **SYS_REF_CLK** on the Juno SoC and clock generators on the V2M-Juno motherboard.
    - The SCP in the Juno SoC boots from internal ROM and then performs the basic setup of the Juno SoC including the PLLs, internal clocks and peripherals inside the Juno SoC.
    - The SCP releases the *Power Policy Units* (PPUs) to start the cluster boot sequences.
11. The MCC measures the board power supplies.
12. The MCC reads the IOFPGA image from the configuration microSD card and loads it into the IOFPGA.
13. The MCC sets the board oscillator frequencies using values from the `board.txt` file.
14. If the MCC finds new software images, it loads them into the FLASH through the IOPGA.
15. The MCC releases the SCC reset **CFG_nRST**.
16. The MCC configures the Juno ARM Development Platform SoC SCC registers using values from the `board.txt` file.
17. The MCC releases the system resets **CB_nPOR** and **CB_nRST** and the system enters the RUN state.

    Note

    The **CB_nPOR** signal drives the **nPORESET** signal inside the Juno SoC.

18. The application code runs. Normal operation continues until a reset occurs:
    - Any of the following initiates the powerdown sequence and puts the V2M-Juno motherboard into the standby-state:
      - Pressing the *Hardware Reset* button.
      - Pressing and holding the *On/Off/Soft Reset* button.
      - A powerdown request from the operating system.
    - A short press of the *On/Off/Soft Reset* button initiates the sleep-state sequence and puts the V2M-Juno motherboard into the sleep-state.

3.2.3 Powerdown sequence

The powerdown sequence takes the V2M-Juno motherboard from the operating state to the standby state.

The powerdown sequence is:

1. The powerdown sequence begins with one of the following:

- Pressing the *Hardware Reset* button.
- Pressing and holding the *On/Off Soft Reset* button for two seconds.
- A powerdown request from the operating system.

2. The *System Control Processor* (SCP) signals powerdown request to the application cluster, that is, either the Cortex-A57 or the Cortex-A53.
3. The application cluster goes through its cleanup and shutdown sequence. The application cluster goes to the *Wait for Interrupt* (WFI) state.
4. The *Power Policy Unit* (PPU) sees the WFI state and powers down.

Note

The SCP waits for this sequence to complete.

5. The SCP powers down the Cortex-A53, Cortex-A57, VSYS and Mali-T624 GPU.
6. The SCP signals to the MCC, using the *Power Management IC* (PMIC), *Ready for Shutdown*.
7. The MCC applies **CB_nPOR** and disables the board clocks and the PMIC.

Note

Signal **CB_nPOR** drives signal **nPORESET** inside the Juno ARM Development Platform SoC.

8. The V2M-Juno motherboard is in the standby state until a press of the *On/Off/Soft Reset* button initiates the powerup and configuration sequence.

3.2.4 Sleep-mode sequence

The sleep state is a low power mode of the Juno ARM Development Platform SoC that preserves operating data and the application code state. The sleep mode sequence takes the Juno ARM Development Platform SoC from the operating state to the sleep state.

The operating state to sleep state sequence is:

1. A short press of the *On/OffSoft Reset* button, less than two seconds.

Warning

Pressing and holding the *On/Off/Soft Reset* button for more than two seconds initiates the powerdown sequence and puts the V2M-Juno motherboard into the standby state. This might result in loss of data.

2. The *System Control Processor* (SCP) sends the *Message Handling Unit* (MHU) sleep command to the application cluster, that is, either the Cortex-A57 or Cortex-A53.
3. The application cluster goes through its cleanup and shutdown sequence. The application cluster goes to the *Wait for Interrupt* (WFI) state.
4. The *Power Policy Unit* (PPU) sees the WFI state and powers down.

Note

The SCP waits for this sequence to complete.

5. The SCP powers down the Cortex-A53, Cortex-A57, VSYS and Mali-T624 GPU.
6. The SCP maintains on-chip RAM and secure RAM data. This data is available when the Juno ARM Development Platform SoC returns to the operating state.
7. The Juno ARM Development Platform SoC is in the sleep state until a press of the *On/Off/Soft Reset* button initiates the wake up sequence and returns it to the operating state.

3.2.5 Wake-up sequence

The wake-up sequence takes the Juno ARM Development Platform SoC from the sleep-state to the operating-state. Operation application software resumes from the previous operating point with all data restored.

The sleep state to operating state sequence is:

1. A short press of the *On/Off/Soft Reset* button, less than two seconds.
2. The *System Control Processor* (SCP) enables the Cortex-A57, Cortex-A53, VSYS and the Mali-T624 GPU.
3. The SCP performs basic Juno ARM Development Platform SoC setup, PLLs, internal clocks and test chip peripherals.
4. The SCP writes state data to on-chip secure RAM and so that the application cluster, that is, either the Cortex-A57 or Cortex-A53, resumes in the correct state and does not boot up from standby.
5. The SCP releases the *Power Policy Unit* (PPU) to start the application cluster boot sequence.
6. The application code resumes from the point when the Juno ARM Development Platform SoC went into the sleep state.

3.3 Configuration files

This section describes the V2M-Juno motherboard configuration files in the configuration microSD card that control the board powerup and configuration process.
This section contains the following subsections:

3.3.1 Overview of configuration files and microSD card directory structure

Because the V2M-Juno motherboard configuration microSD card is flash memory, it is only necessary to load new configuration files if you change the system configuration. The V2M-Juno motherboard contains default configuration files.

If you connect a workstation to the configuration USB port or configuration Ethernet port, the configuration memory device, the configuration microSD card, appears as a *USB Mass Storage Device* (USBMSD) and you can add, edit, or delete files.

You can use a standard text editor that produces DOS line endings to read and edit the board configuration files.

The following figure shows a typical example of the directory structure in the microSD card memory.

Caution

Files names and directory names are in 8.3 format:

- File names that you generate must be in lower case.
- Directory names must be in upper case.
- All configuration files must end in DOS line endings, `0x0D`/`0x0A`.

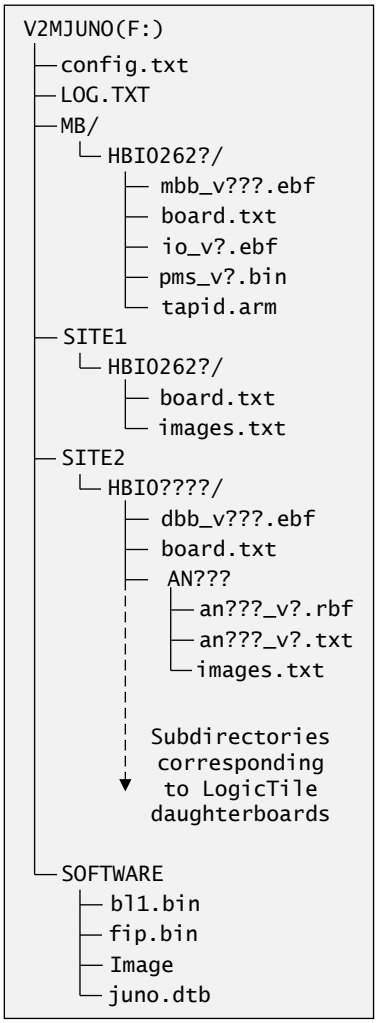

Figure 3-3 Example configuration microSD card directory structure

The directory structure and file name format ensure that each image is matched to the correct target device defined in the V2M-Juno motherboard configuration EEPROM and in the daughterboard EEPROM.

`config.txt`
: Generic configuration file for all motherboards. This file applies to all Versatile Express motherboards including the V2M-Juno motherboard.

`MB` directory
: This directory contains subdirectories for any motherboard variants that might be present in the system. The subdirectory names match the HBI codes for the specific motherboard variants. The files in these directories contain clock, register and, other settings for the boards.

`SITE1` directory
: This directory contains configuration files that relate to the Juno ARM Development Platform SoC and to external memory that the Juno ARM Development Platform SoC can acess.

`SITE2` directory
: This directory contains configuration files for any LogicTile daughterboard that you might fit to the V2M-Juno motherboard. The subdirectory names match the HBI codes for all possible daughterboards. The files in these directories contain clock, register, and other settings for the daughterboards.

`SOFTWARE` directory
: This directory contains application files that the MCC can load into SRAM or NOR Flash. The IMAGES section in the `config.txt` file defines the file that the MCC loads.

Related references

A.1.2 Configuration 10Mbps Ethernet and dual-USB connector on page Appx-A-119.

A.1.5 Configuration USB connector on page Appx-A-122.

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

3.3.2 `config.txt` generic motherboard configuration file

You can use the V2M-Juno motherboard configuration USB port or configuration Ethernet port to update the generic Versatile Express configuration file `config.txt` from your workstation to the root directory of the microSD card.

The following example shows a typical `config.txt` configuration file in the root directory of the configuration microSD card.

Note

- Colons (:) indicate the end of commands and must be separated by a space character (`0x20`) from the value fields.
- Semicolons (;) indicate comments.
- *`ASSERTNPOR`* must always have the value TRUE.

```
TITLE: Versatile Express V2M-Juno configuration file

[CONFIGURATION]
AUTORUN: FALSE                  ;Auto Run from power on
TESTMENU: FALSE                 ;MB Peripheral Test Menu

UPDATE: FALSE                   ;Force JTAG and FPGA update to DBs
VERIFY: FALSE                   ;Force FPGA verify to DBs

DVIMODE: VGA                    ;VGA or SVGA or XGA or SXGA or UXGA

MBLOG: TRUE                     ;LOG MB MICRO TO UART1 in run mode
DBLOG: TRUE                     ;LOG DB MICRO TO UART2 in run mode

USERSWITCH: 00000000            ;Userswitch[7:0] in binary
CONFSWITCH: 00000000            ;Configuration Switch[7:0] in binary
ASSERTNPOR: TRUE                ;External resets assert nPOR
WDTRESET: NONE                  ;Watchdog reset options NONE/RESETMB/RESETDB

PCIMASTER: DB1                  ;Port Failover DB1/SL3
MASTERSITE: DB1                 :Boot Master DB1/SL3
REMOTE: NONE                    ;Selects remote command options NONE/USB/FTP

SMCMACADDRESS: 0xFFFFFFFFFFFF   ;MAC Address for SMC Ethernet
MCCMACADDRESS: 0xFFFFFFFFFFFF   ;MAC Address for MCC configuration Ethernet

HOSTNAME: V2M_JUNO_01           ;User name to identify board via FTP over Configuration
Ethernet
```

3.3.3 Contents of the MB directory

The `MB` directory contains files that relate to the MCC and to other components on the V2M-Juno motherboard, but not the Juno ARM Development Platform SoC. The `MB` directory contains a configuration HBI subdirectory that matches the HBI code of the V2M-Juno motherboard.

The HBI subdirectory contains:

- A `board.txt` file. This file defines the BIOS image that the MCC loads during configuration.
- A file of the form `mbb_vxxx.ebf`. This is the MCC BIOS image that the `board.txt` file defines.
- A file of the form `io_bxxx.bit`. This is the IOFPGA image file.
- A file of the form `pms_vxxx.bin`. This is a binary configuration file for the *Power Management IC* (PMIC) on the V2M-Juno motherboard.
- A `tapid.arm` file. This file contains JTAG ID codes for the V2M-Juno motherboard and LogicTile daughterboards.

The following example shows a typical V2M-Juno motherboard configuration `board.txt` file.

```
BOARD: HBI0262
TITLE: Motherboard configuration file

[MCCS]
MBBIOS mbb_v100.ebf                 ;MB BIOS IMAGE

[FPGAS]
MBIOFPGA: io_b107.bit               ;MB IOFPGA

[PMIC]
MBPMIC: pms_v100.bin                ;MB PMIC

[OSCCLKS]
TOTALOSCCLKS: 11
OSC0: 50.0                          ;OSC0 Juno SYSREFCLK    (System clock)
OSC1: 50.0                          ;OSC1 Juno AONREFCLK    (Always on)
OSC2: 50.0                          ;OSC2 Juno PXLREFCLK    (HS pixel clock)
OSC3: 50.0                          ;OSC3 Juno PXLCLKIN     (LS pixel clock)
OSC4: 75.0                          ;OSC4 Juno I2SCLK       (Audio)
OSC5: 50.0                          ;OSC5 Juno SMCMCLK      (Static memory)
OSC6: 50.0                          ;OSC6 Juno CA53_REF_CLK (RSVD)
OSC7: 50.0                          ;OSC7 Juno CA57 REF_CLK (RSVD)
OSC8: 50.0                          ;OSC8 Juno GPU REF_CLK  (RSVD)
OSC9: 50.0                          ;OSC9 IOFPGA BOOT       (RSVD)
OSC10: 24.0                         ;OSC10 IOFPGA UART      (RSVD)
OSC11: 7.27                         ;OSC11 Juno UARTCLK     (UART clock)
```

Related concepts

2.5.1 Overview of clocks on page 2-27.

3.3.4 Contents of the SITE1 directory

The `SITE1` directory contains files that relate to the Juno ARM Development Platform SoC and to external memory on the V2M-Juno motherboard that the Juno ARM Development Platform SoC can access.

The `SITE1` subdirectory contains an `HBI0262` subdirectory that matches the HBI code of the V2M-Juno motherboard. The `HBI0262` subdirectory contains the following files:

A `board.txt` file
: Contains configuration information for the SCC registers in the Juno ARM Development Platform SoC.

An `images.txt` file
: Defines the files that the MCC loads into external memory during configuration.

The following example shows a typical V2M-Juno motherboard `board.txt` file in the `SITE1` directory that relates to the Juno SoC.

```
BOARD: HBI0262
TITLE: V2M-Juno DevChip Configuration File

[SCC REGISTERS]
TOTALSCCS: 6                         ;Total Number of SCC registers
SCC: 0x050 0x00000001                ;Enable Thin Links
SCC: 0x00C 0x000000C2                ;Clock Control, TMIF2XCLK, Register 0xC1=default
                                     ;[3:0] CLKSEL : 0 Output gated, 1 AON_REF_CLK, 2 SYSCLK
                                     ;[7:4] CLKDIV : Clock divider-1 (0 gives a division of
1)
SCC: 0x010 0x000000C2                ;Clock Control : TSIF2XCLK, Register 0xC1=default
                                     ;[3:0] CLKSEL : Output gated, 1, AON_REF_CLK, 2 SYSCLK
                                     ;[7:4] CLKDIV : Clock divider -1 (0 gives a division of
1)
SCC: 0x100 0x801F1000                ;A57 PLL Register 0 (800MHz)
SCC: 0x104 0x0000F100                ;A57 PLL Register 1
SCC: 0x108 0x801B1000                ;A53 PLL Register 0 (700MHz)
SCC: 0x10C 0x0000D100                ;A53 PLL Register 1
SCC; 0x0F8 0x0BEC0000                ;BL1 entry point
```

The following example shows a typical V2M-Juno motherboard `images.txt` file in the `SITE1` directory that relates to the Juno SoC.

```
TITLE: Versatile Express Images Configuration File

[IMAGES]
TOTALIMAGES: 4                      ;Number of Images (Max : 32)

NOR0UPDATE: AUTO                    ;Image Update:NONE/AUTO/FORCE
NOR0ADDRESS: 0x00000000             ;Image Flash Address
NOR0FILE: \SOFTWARE\fip.bin         ;Image File Name
NOR0LOAD: 00000000                  ;Image Load Address
NOR0ENTRY: 00000000                 ;Image Entry Point

NOR1UPDATE: AUTO                    ;Image Update:NONE/AUTO/FORCE
NOR1ADDRESS: 0x03EC0000             ;Image Flash Address
NOR1FILE: \SOFTWARE\bl1.bin         ;Image File Name
NOR1LOAD: 00000000                  ;Image Load Address
NOR1ENTRY: 00000000                 ;Image Entry Point

NOR2UPDATE: AUTO                    ;Image Update:NONE/AUTO/FORCE
NOR2ADDRESS: 0x00500000             ;Image Flash Address
NOR2FILE: \SOFTWARE\Image           ;Image File Name
NOR2LOAD: 00000000                  ;Image Load Address
NOR2ENTRY: 00000000                 ;Image Entry Point

NOR3UPDATE: AUTO                    ;Image Update:NONE/AUTO/FORCE
NOR3ADDRESS: 0x00F00000             ;Image Flash Address
NOR3FILE: \SOFTWARE\juno.dtb        ;Image File Name
NOR3LOAD: 00000000                  ;Image Load Address
NOR3ENTRY: 00000000                 ;Image Entry Point
```

3.3.5 Contents of the SITE2 directory

The `SITE2` directory contains configuration files for LogicTile daughterboards that you can fit in the V2M-Juno motherboard daughterboard site.

See the Technical Reference Manual for your fitted daughterboard for information about the daughterboard files in the `SITE2` directory.

3.3.6 Contents of the SOFTWARE directory

The `SOFTWARE` directory contains applications that you can load into external FLASH memory.

You can create new applications and load them into the FLASH on the V2M-Juno motherboard. Application images are typically boot images or demo programs and have a `.axf` extension.

Typical applications in this directory are:

- `bl1.bin` ARM Trusted Firmware.
- `fip.bin` Firmware Image Package:
  - Contains BL2, BL30, BL31, BL33.
- `Image` Linux kernel.
- `juno.dtb` Juno device tree.

3.4 Configuration switches

The V2M-Juno motherboard provides two configuration switches, SW0 and SW1. This section describes the use of those switches.

This section contains the following subsections:

3.4.1 Use of configuration switches

The switches SW0 and SW1 affect board initialization.

The configuration file `config.txt` contains *`USERSWITCH`* and *`CFGSWITCH`* entries for the virtual switch register bits SYS_SW[7:0] and SYS_CFGSW[7:0] in the IOFPGA. Configuration switch SW0 also modifies SYS_SW[0]. The configuration system does not use these virtual switches for system configuration, but they are available for the user application and boot monitor.

See the following for more information:

- *4.3.3 SYS_SW Register* on page 4-89.
- *4.3.7 SYS_CFGSW Register* on page 4-92.

Note

- The default setting for configuration switches SW0 and SW1 is OFF.
- If the switches are in the up position, they are OFF.

Bootscript switch SW0

SW0 in the ON position, or the `config.txt` entry for USERSWITCH[0] being set to 1, sets SYS_SW[0] to `0b1`.

If SYS_SW[0] is set to `0b1`, the boot loader runs the OS automatically at powerup. If the OS software supports this feature, under UEFI this boot process starts automatically irrespective of the switch setting.

SYS_SW[30] indicates the value of physical configuration switch SW0.

A user application can also modify SYS_SW[0] but the change does not take effect until the next reset.

Remote UART control switch SW1

SW1 in the ON position enables UART control and the flow-control signals on UART0 to control the standby state. This setting is typically used on test farms.

SYS_SW[31] indicates the value of physical configuration switch SW1.

3.4.2 Remote UART configuration

If SW1 is ON to enable remote UART control:

- An external controller can toggle UART0 **SER0_DSR**, pin 6, HIGH for 100ms to put the V2M-Juno motherboard into standby mode. This is equivalent to pressing the *Hardware Reset* button. Power cycling the board also places the system in standby mode.

  Note

  The duration of the **SER0_DSR** HIGH pulse must be greater than or equal to 100ms.

- An external controller can remotely select whether the MCC or the system application uses UART0 in run-mode. This overrides the `confix.txt` entry for MBLOG and eliminates the requirement to use the second serial port on UART1.

Set UART0 **SER0_CTS**, pin 8, LOW to select system mode, or set it HIGH to select MCC mode.

Remote UART0 control requires a full null modem cable that ARM supplies with the V2M-Juno motherboard. The following figure shows the cable wiring.

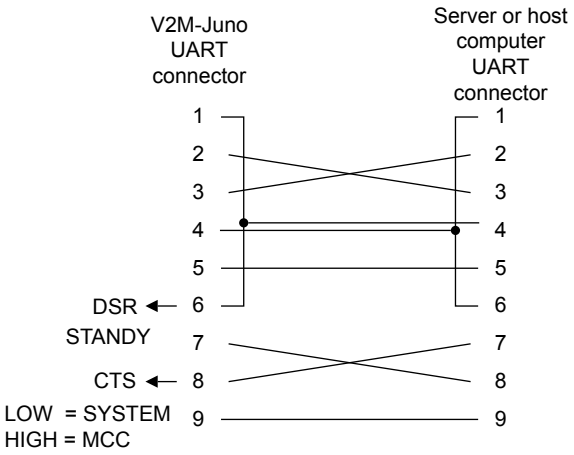

Figure 3-4 Modem cable wiring

You can control the **SER0_DSR** and **SER0_CTS** signals using control logic on the host computer.

Alternatively, you can use a custom terminal program such as `ARM VETerminal.exe` that ARM provides on the V2M-Juno motherboard DVD. This program integrates the terminal output and control buttons into a single application.

3.5 Use of reset push buttons

This section describes the use and functions of the reset push buttons on the V2M-Juno motherboard.

This section contains the following subsections:

3.5.1 ON/OFF/Soft Reset button

This push button enables you to perform a software reset of the system.

You initiate a software reset of the system by briefly pressing the *ON/OFF/Soft Reset* button during run time. The MCC performs a software reset of the Juno ARM Development Platform SoC and resets the devices on the board.

The software reset sequence is as follows:

1. Briefly press the *ON/OFF/Soft Reset* button.

   Caution

   If you press and hold the *ON/OFF/Soft Reset* button for more than two seconds, the system enters the Standby State in the same way as pressing the *Hardware Reset* button.

2. The MCC asserts the **CB_nRST** reset signal.
3. The MCC releases **CB_nPOR**.
4. The MCC releases **CB_nRST**.
5. The V2M-Juno motherboard enters the run state.

Note

- The MCC does not read the configuration files or perform a board reconfiguration as a result of a software reset.
- Signal **CB_nPOR** drives signal **nPORESET** inside the Juno ARM Development Platform SoC.

Related concepts

2.6.1 Reset push buttons on page 2-36.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

3.5.2 Hardware Reset button

This push button enables you to perform a hardware reset of the system.

You can change the operation of the board from ON to Standby by briefly pressing the *Hardware Reset* button. This switches off the power to the board and resets the system to the default values.

If you then press the *ON/OFF/Soft Reset* push button, the system performs a full configuration and enters the run state.

Related concepts

2.6.1 Reset push buttons on page 2-36.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

3.6 Command-line interface

This section describes the V2M-Juno motherboard command-line interface that supports system command-line input to the MCC and to the Daughterboard Configuration Controller on the LogicTile daughterboard.

This section contains the following subsections:

3.6.1 Overview of the V2M-Juno motherboard MCC command-line interface

You must connect a workstation to UART0 to enter MCC system commands.

You must set the *MBLOG* option in the `config.txt` to TRUE to enter MCC system commands at the UART0 port.

The workstation settings must be:

- 115.2kBaud.
- 8N1 representing 8 data bits, no parity, one stop bit.
- No hardware or software flow control.

3.6.2 Overview of the LogicTile daughterboard command-line interface

You must connect a workstation to UART1 to input system commands to the Daughterboard Configuration Controller on the LogicTile daughterboard.

You must set the *DBLOG* option in the `config.txt` to TRUE to enter LogicTile daughterboard system commands at the UART1 port. The setting takes effect after the next reset.

The workstation settings must be:

- 115.2kBaud.
- 8N1 representing 8 data bits, no parity, one stop bit.
- No hardware or software flow control.

See the appropriate Technical Reference Manual for your LogicTile daughterboard for information on the daughterboard command-line interface.

3.6.3 MCC main command menu

This section shows the V2M-Juno motherboard MCC main menu system commands.

The following table shows the MCC main menu system commands.

Table 3-1 V2M-Juno motherboard MCC main command menu

Command	Description
`CAP` *`file_name`* `[/A]`	Capture serial data to the file *file_name*. Use the `/A` option to append data to an existing file.
`COPY` *`input_filename_1`* [*`input_filename_2`*] *`output_filename`*	Copy a file *input_filename_1* to *output_filename*. Option *input_filename_2* merges *input_filename_1* and *input_filename_2*.
`DEBUG`	Change to the debug menu.

Table 3-1 V2M-Juno motherboard MCC main command menu (continued)

Command	Description
`DEL` *filename*	Delete file *filename*.
`DIR` [*mask*]	Display a list of files in the directory.
`EEPROM`	Change to the EEPROM menu.
`FILL` *filename* [*nnnn*]	Create a file *filename* filled with text. *nnnn* specifies the number of lines to create. The default is 1000.
`FTP_ON`	Enable MCC FTP Server.
`FTP_OFF`	Disable MCC FTP Server.
`HELP` or `?`	Display this help.
`REBOOT`	Cycle system power and reboot.
`REN` *filename_1 filename_2*	Rename a file from *filename_1* to *filename_2*.
`RESET`	Reset the V2M-MPS2 board using the **nRST** reset signal.
`SHUTDOWN`	Shutdown the power supply but leave the MCC running. The board returns to Standby mode.
`TYPE` *filename*	Display the contents of text file *filename*.
`USB_ON`	Enable MCC USB configuration port.
`USB_OFF`	Disable MCC USB configuration port.

3.6.4 MCC debug menu

Enter DEBUG at the main menu to switch to the debug submenu. The debug submenu is valid only in run mode.

The following table shows the debug commands.

Table 3-2 V2M-Juno motherboard MCC debug command menu

Command	Description
`DATE`	Display current date.
`DEBUG [0|1]`	Enable or disable debug printing: 0 Disable 1 Enable
`DEPOSIT` *address data*	Write word to system memory address.
`EXAM` *address* [*nnnn*]	Examine system memory address at *address*. *nnnn* is number, in Hex, of words to read.
`EXIT` or `QUIT`	Return to main menu.
`HELP` or `?`	Display this help.
`TIME`	Display current time.

3.6.5 EEPROM menu

Enter EEPROM at the main menu to switch to the EEPROM submenu. The contents of the V2M-Juno motherboard EEPROMs identify the specific board variant and might contain data to load to the other devices on the board.

The following table shows the EEPROM commands.

Caution

You must not modify the EEPROM settings. The settings are programmed with unique values during production and changing them might compromise the function of the board.

Table 3-3 V2M-Juno motherboard EEPROM commands

Command	Description
`CONFIG 0` *filename*	Write configuration file to EEPROM.
`EXIT` or `QUIT`	Return to main menu.
`ERASECON [0]`	Erase configuration section of EEPROM.
`ERASEDEV [0]`	Erase device section of EEPROM.
`ERASERANGE [0]` *start end*	Erase EEPROM between *start* and *end*.
`ERASEIMAGE` *image_id*	Erase image stored in Motherboard EEPROM.
`ERASEIMAGES`	Erase images stored in Motherboard EEPROM.
`HELP` or `?`	Display this help.
`READIMAGES`	Read images stored in Motherboard EEPROM.
`READCF [0]`	Read configuration EEPROM.
`READRANGE [0]` [*start*] [*end*]	Read EEPROM between *start* and *end*.

Chapter 4
Programmers Model

This chapter describes the programmers model of the Versatile Express V2M-Juno motherboard.

It contains the following sections:

4.1 About this programmers model

The Juno ARM Development Platform SoC programmers model derives from the ARMv8 compute subsystem architecture that supports ARMv8 AARch64 software and tooling.

The following information applies to the SCC registers and to the system configuration registers or SYS_CFG registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or powerup reset.
  - *Table 1* describes register access type as follows:

    RW Read and write.

    RO Read only.

    WO Write only.

4.2 V2M-Juno motherboard memory maps

This section describes the memory map of the V2M-Juno motherboard.
This section contains the following subsections:

4.2.1 Juno SoC top-level application and SMC interface memory maps

The Juno SoC SMC occupies the expansion AXI memory at `0x00_0800_0000` and supports chip-selects that access components, systems and memory on the V2M-Juno motherboard. The security status is exported security.

Chip select CS3 inside SMC accesses the low-bandwidth system peripherals inside the IOFPGA and is at `0x00_1C00_0000`.

The following figure shows the mapping of the SMC memory map into the Juno SoC top-level application memory map. It shows the SMC memory map of the production V2M-Juno motherboard.

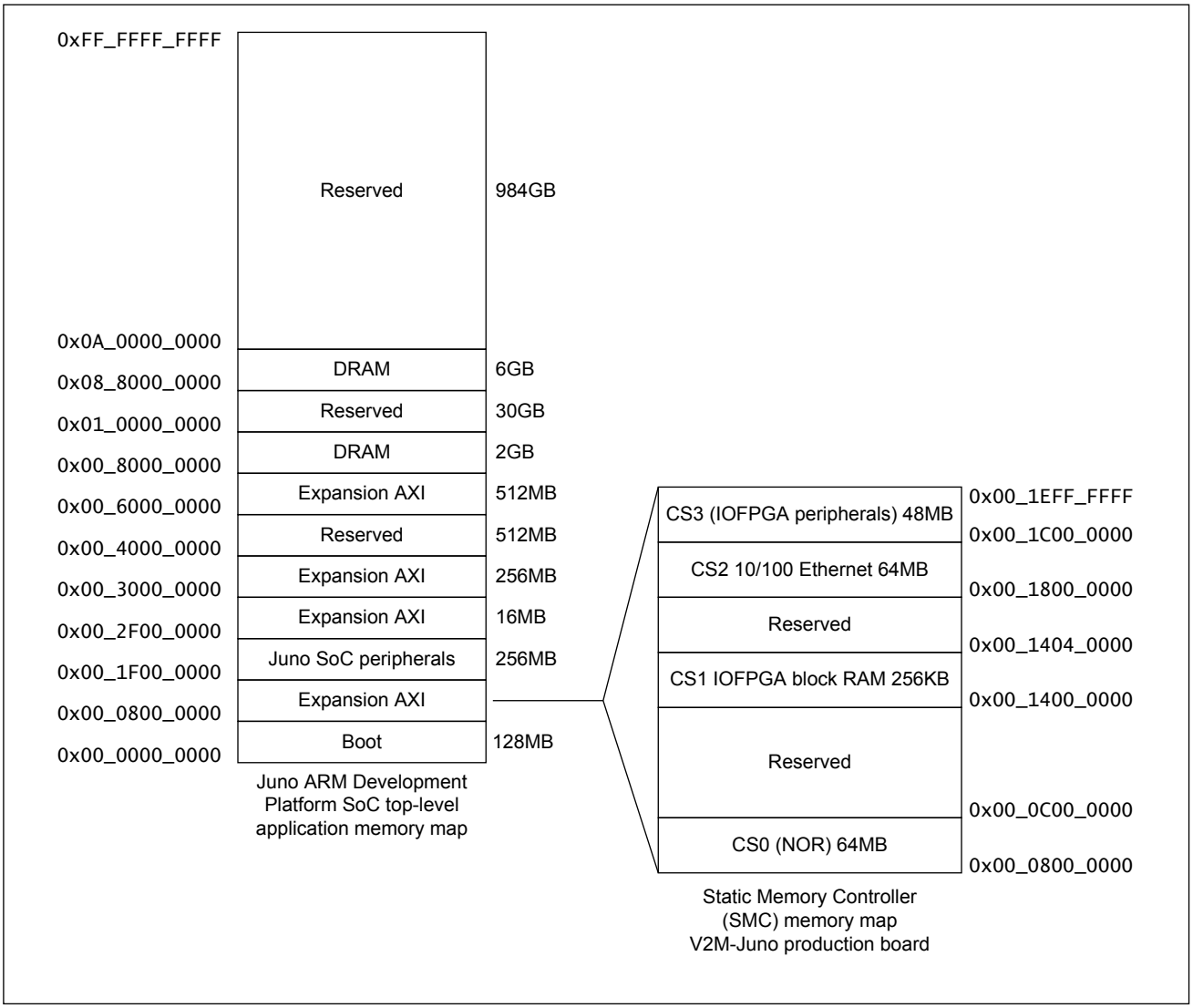

Figure 4-1 Juno SoC top-level application and SMC interface memory maps

The following table shows the SMC memory map of the production V2M-Juno motherboard.

Table 4-1 SMC interface memory map of production V2M-Juno motherboard

Address range	Size	Description
`0x00_0800_0000 - 0x00_0BFF_FFFF`	64MB	CS0-Motherboard NOR Flash.
`0x00_0C00_0000 - 0x00_13FF_FFFF`	128MB	Reserved. Do not write to or read from these addresses.
`0x00_1400_0000 - 0x00_1403_FFFF`	256KB	CS1-256KB internal IOFPGA block RAM.
`0x00_1404_0000 - 0x00_17FF_FFFF`	65535.75KB	Reserved. Do not write to or read from these addresses.
`0x00_1800_0000 - 0x00_1BFF_FFFF`	64MB	CS2-10/100 Ethernet.
`0x00_1C00_0000 - 0x00_1EFF_FFFF`	48MB	CS3-IOFPGA peripherals.

See the *Juno ARM® Development Platform SoC Technical Reference Manual* for:

- More information on the top-level memory map of the Juno ARM Development Platform SoC.
- Information on the *System Control Processor* (SCP) memory map in the Juno ARM Development Platform SoC. This is independent of the top-level application map and includes the SCC registers.

Note

The prototype version of the V2M-Juno motherboard provides chip select, CS5 at `0x00_1000_0000`, that supports SMC USB 2.0 access. See *B.2.4 SMC memory map of the prototype V2M-Juno motherboard on page Appx-B-135*. The production board does not provide CS5.

4.2.2 IOFPGA system peripherals memory map

This section describes the memory map of the IOFPGA system peripherals which is at chip select CS3 in the SMC interface.

The chip select CS3 is at `0x00_1C00_0000` and provides access to low-bandwidth system peripherals in the IOFPGA that the Juno SoC does not provide.

The following figure shows the mapping of the IOFPGA system peripherals memory map into the SMC memory map.

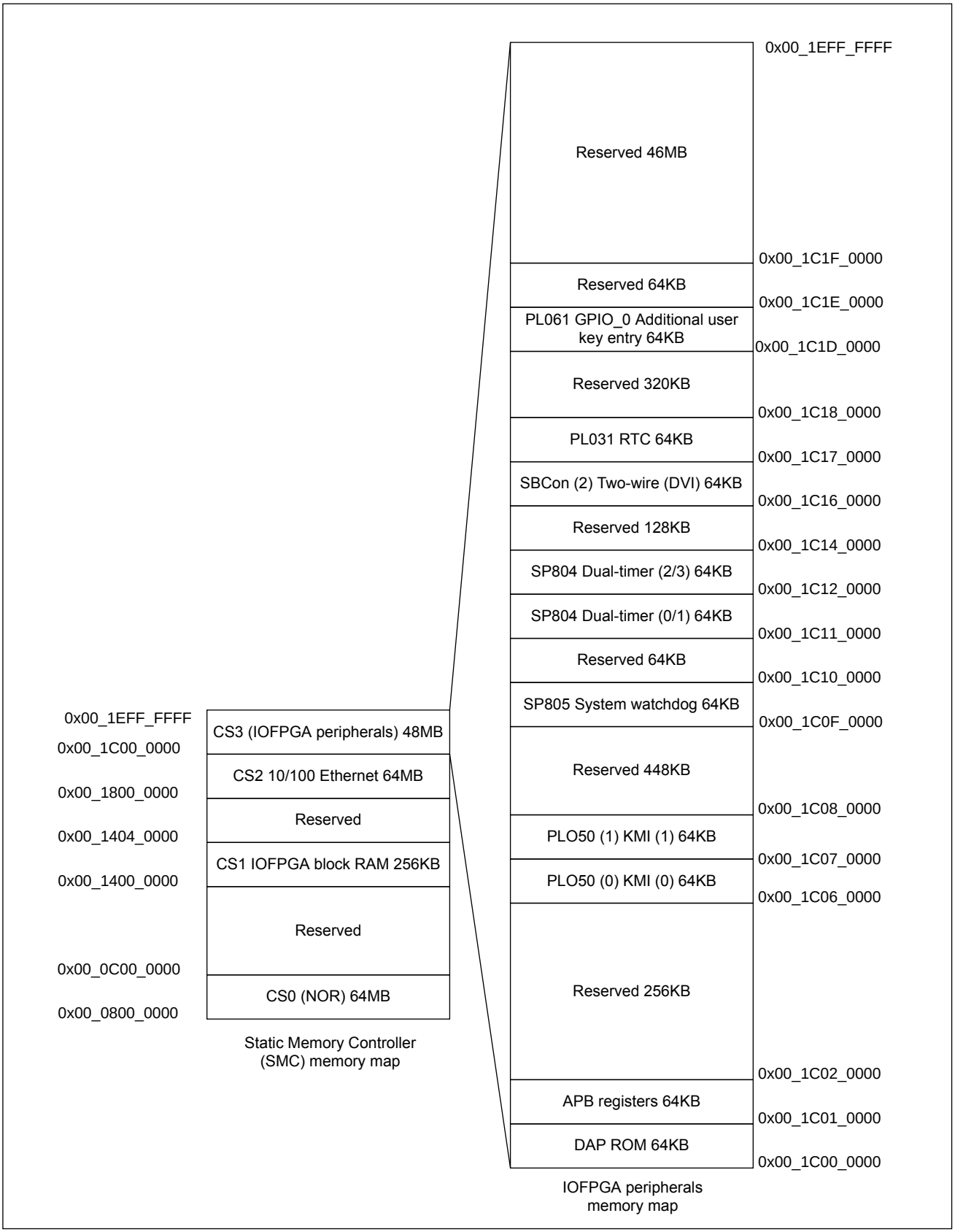

Figure 4-2 V2M-Juno motherboard IOFPGA system peripherals memory map

The following table shows the IOFPGA system peripherals memory map.

Table 4-2 V2M-Juno motherboard IOFPGA system peripherals memory map

Address range	Size	Description
0x00_1C00_0000 - 0x00_1C00_FFFF	64KB	CS3-DAP ROM.
0x00_1C01_0000 - 0x00_0C01_FFFF	64KB	CS3-APB registers. User LEDs.
0x00_1C02_0000 - 0x00_1C05_FFFF	256KB	Reserved. Do not write to or read from these addresses.
0x00_1C06_0000 - 0x00_1C06_FFFF	64KB	CS3-PL050 (0) KMI interface 0.
0x00_1C07_0000 - 0x00_1C07_FFFF	64KB	CS3-PL050 (1) KMI interface 1.
0x00_1C08_0000 - 0x00_1C0E_FFFF	448KB	Reserved. Do not write to or read from these addresses.
0x00_1C0F_0000 - 0x00_1C0F_FFFF	64KB	SP805 System watchdog.
0x00_1C10_0000 - 0x00_1C1F_FFFF	64KB	Reserved. Do not write to or read from these addresses.
0x00_1C11_0000 - 0x00_1C11_FFFF	64KB	CS3-SP804 Dual-timer (0/1).
0x00_1C12_0000 - 0x00_1C12_FFFF	64KB	CS3-SP804 Dual-timer (2/3).
0x00_1C14_0000 - 0x00_1C15_FFFF	128KB	Reserved. Do not write to or read from these addresses.
0x00_1C1D_0000 - 0x00_1C1D_FFFF	64KB	CS3-PL061 GPIO 0 Additional user key entry.
0x00_1C1E_0000 - 0x00_1C1E_FFFF	64KB	Reserved. Do not write to or read from these addresses.
0x00_1C1F_0000 - 0x00_1EFF_FFFF	46MB	Reserved. Do not write to or read from these addresses.

Related concepts

2.8 IOFPGA on page 2-42.

4.2.3 DDR3L memory map

The DDR3L memory map occupies two parts of the Juno SoC top-level application map, 2GB at 0x00_8000_0000, and 6GB at 0x08_8000_0000. The security is programmable access security.

The following figure shows the mapping of the DDR3L memory map into the Juno SoC top-level application memory map.

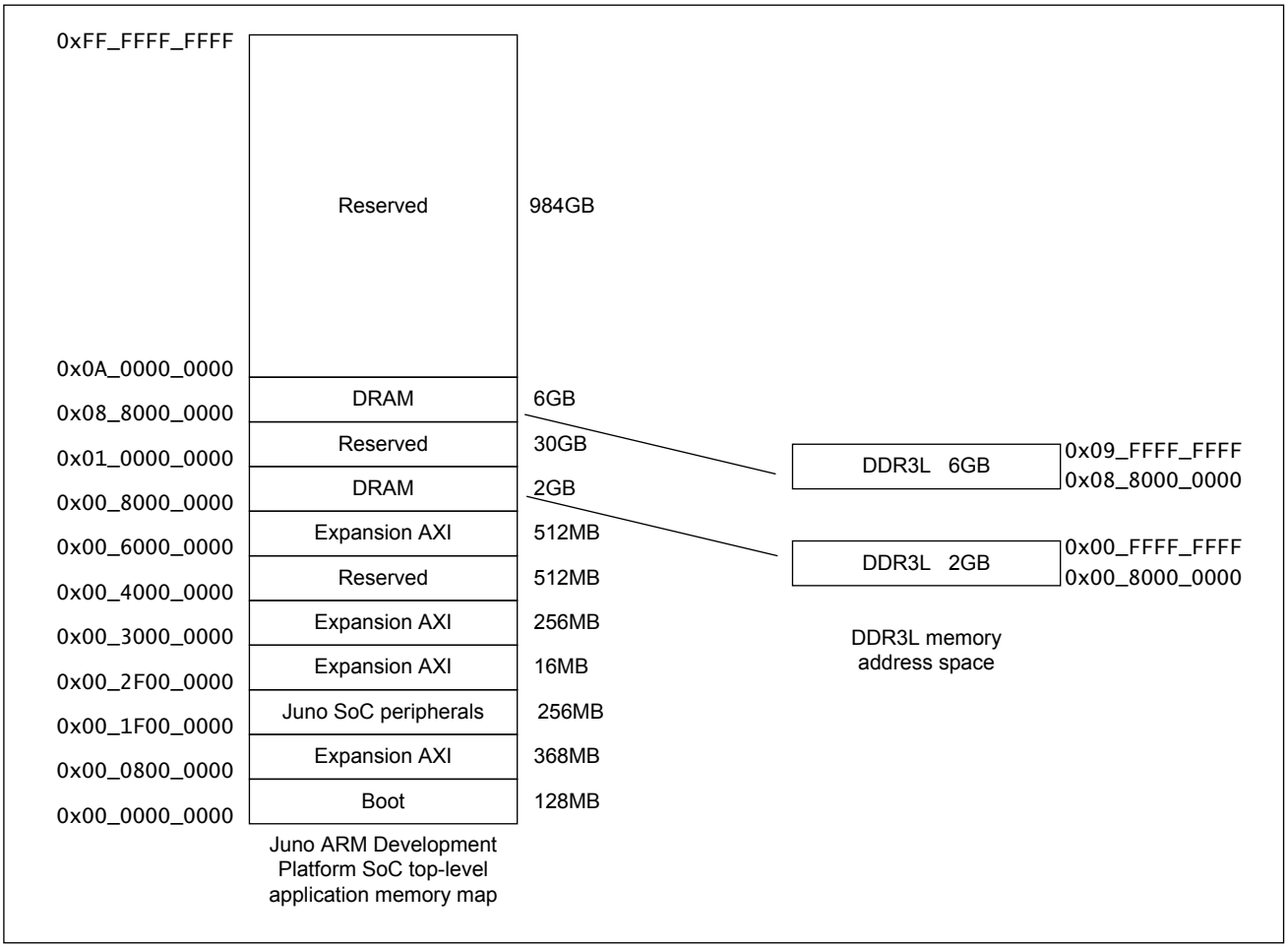

Figure 4-3 V2M-Juno motherboard DDR3L memory map

The following table shows the V2M-Juno motherboard DDR3L memory map.

Table 4-3 V2M-Juno motherboard DDR3L memory map

Address range	Size	Description
`0x00_8000_0000` - `0x00_FFFF_FFFF`	2GB	DDR3L
`0x08_8000_0000` - `0x09_FFFF_FFFF`	6GB	DDR3L

4.2.4 Other memory maps

See the for information on:

- Other areas of the top-level memory map of the Juno ARM Development Platform SoC
- Information on the System Control Processor (SCP) memory map in the Juno ARM Development Platform SoC. This is independent of the top-level application map and includes the SCC registers.

4.3 APB system registers

This section describes the APB system registers in the IOFPGA.

This section contains the following subsections:

4.3.1 APB system register summary

This section summarizes the characteristics of the V2M-Juno motherboard APB system registers in the IOFPGA.

The base memory address of the APB system registers is `0x1C010000`. The following table shows the registers in address offset order from the base memory address.

Table 4-4 V2M-Juno motherboard APB system register summary

Offset	Name	Type	Reset	Width	Comment
`0x0000`	SYS_ID	RO	`0xX00000XX`	32	Contains information about board, testchip, and bus revisions.
`0x0004`	SYS_SW	RO/RW	`0x00000XX`	32	Bits[7:0] are the soft user switches.
`0x0008`	SYS_LED	RO/RW	`0x000000XX`	32	Bits[7:0] map to the user LEDs.
`0x0024`	SYS_100HZ	RO/RW	`0xXXXXXXXX`	32	100Hz counter.
`0x0030`	SYS_FLAGS	RO	`0x00000000`	32	Flag register. Provides 32 user flag bits.
`0x0030`	SYS_FLAGSSET	WO	-	32	Flag register.
`0x0034`	SYS_FLAGSCLR	WO	-	32	Flag register.
`0x0038`	SYS_NVFLAGS	RO	`0x00000000`	32	Flag register.
`0x0038`	SYS_NVFLAGSSET	WO	-	32	Flag register
`0x003C`	SYS_NVFLAGSCLR	WO	-	32	Flag register
`0x0058`	SYS_CFGSW	RO/RW	`0x000000XX`	32	Bits[7:0] are the soft configuration switches.
`0x005C`	SYS_24MHZ	RO	`0xXXXXXXXX`	32	32-bit counter clocked at 24MHz.
`0x0060`	SYS_MISC	RW/RO	`0x00000000`	32	Miscellaneous control flags.
`0x0084`	SYS_PROC_ID0	RW	`0x0X000000`	32	Denotes active clusters in Juno SoC.

Table 4-4 V2M-Juno motherboard APB system register summary (continued)

Offset	Name	Type	Reset	Width	Comment
0x0088	SYS_PROC_ID1	RW	0x0X000XXX	32	Contains identification information about the LogicTile Express daughterboard and daughterboard FPGA image.
0x0120	SYS_FAN_DATA	RW	0x00000000	32	Contains a value that represents the operating temperature of the Juno SoC. The MCC uses this value to moderate the speed of the cooling fan on the V2M-Juno motherboard.

Related concepts

2.4 Power control and Dynamic Voltage and Frequency Scaling (DVFS) on page 2-25.

4.3.2 SYS_ID Register

The SYS_ID Register characteristics are:

Purpose
Contains information about the V2M-Juno motherboard and the bus and image versions inside the IOFPGA.

Usage constraints
The SYS_ID Register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

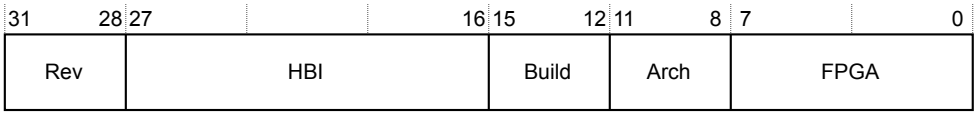

Figure 4-4 SYS_ID Register bit assignments

The following table shows the bit assignments.

Table 4-5 SYS_ID Register bit assignments

Bits	Name	Function
[31:28]	Rev	Board revision: • 0x0 - Rev A. • 0x1 - Rev B. • 0x2 - Rev C. • 0x3 - Rev D.
[26:16]	HBI	HBI board number in BCD: • 0x262 = HBI0262.
[15:12]	Build	Build variant of board: • 0xF - All builds.

Table 4-5 SYS_ID Register bit assignments (continued)

Bits	Name	Function
[11:8]	Arch	IOFPGA bus architecture: • `0x4` = AHB. • `0x5` = AXI.
[7:0]	FPGA	FPGA build in BCD. The actual value read depends on the FPGA build.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.3 SYS_SW Register

The SYS_SW Register characteristics are:

Purpose
Reads the *USERSWITCH* entry in the `config.txt` file. A bit set to `0b1` indicates that the switch is ON.

Usage constraints
Bits[31:8] are read-only. Bits[7:0] are read-write.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

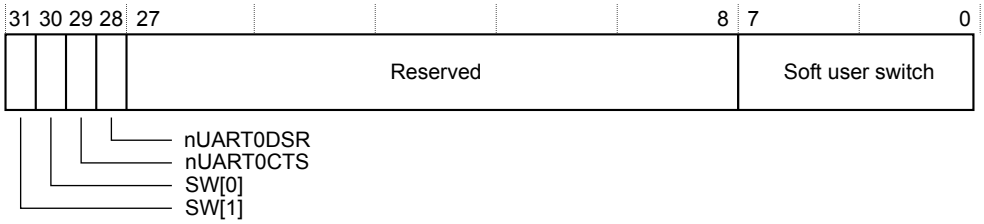

Figure 4-5 SYS_SW Register bit assignments

The following table shows the bit assignments.

Table 4-6 SYS_SW Register bit assignments

Bits	Name	Function
[31]	SW[1]	Indicates the value of the physical configuration switch SW[1]: • `0b1` = ON.
[30]	SW[0]	Indicates the value of the physical configuration switch SW[0]: • `0b1` = ON.
[29]	nUART0CTS	UART0 control signal.
[28]	nUART0DSR	UART0 control signal.
[27:8]	-	Reserved. Do not write to or read from these bits.
[7:0]	Soft user switch.	Application software can read these switch settings. If SYS[0] = `0b1`, the Boot Monitor runs its bootscript at powerup.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.4 SYS_LED Register

The SYS_LED Register characteristics are:

Purpose

Controls the eight user LEDs on the V2M-Juno motherboard. All LEDs are turned OFF at reset. The Boot Monitor updates the LED value.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

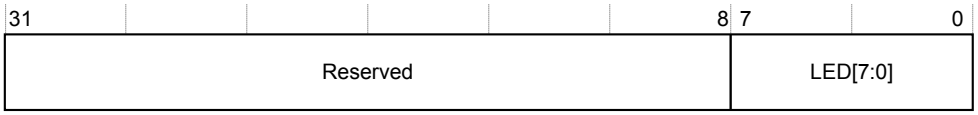

Figure 4-6 SYS_LED Register bit assignments

The following table shows the bit assignments.

Table 4-7 SYS_LED Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved. Do not write to or read from these bits.
[7:0]	LED[7:0]	Set or read the user LED states: • `0b0` = OFF. • `0b1` = ON.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.5 SYS_100HZ Register

The SYS_100HZ Register characteristics are:

Purpose

A 32-bit counter that updates at 100Hz. The input clock derives from the 24MHz clock generator on the V2M-Juno motherboard.

Usage constraints

The SYS_100HZ Register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

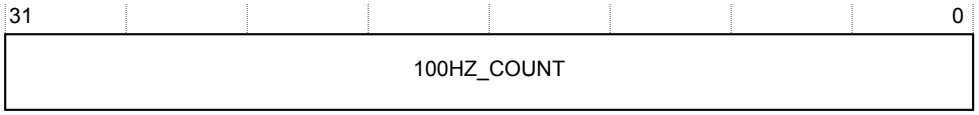

Figure 4-7 SYS_100HZ Register bit assignments

The following table shows the bit assignments.

Table 4-8 SYS_100HZ Register bit assignments

Bits	Name	Function
[31:0]	100HZ_COUNT	Contains the count, at 100Hz, since the last **CB_nRST** reset.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.6 SYS_FLAG Registers

The Flag Register characteristics are:

Purpose

Provide two 32-bit registers SYS_FLAGS and SYS_NVFLAGS, that contain general-purpose flags. The applicatoin software defines the meaning of the flags. You use the Registers, SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET and SYS_NVFLAGSCLR to set and clear the bits in the Flag Registers.

Usage constraints

The SYS_FLAGS and SYS_NVFLAGS Registers are read-only.

The SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET and SYS_NVFLAGSCLR Registers are write-only.

Configurations

Available in all V2M-Juno motherboard configurations.

SYS_FLAGS Register

The SYS_FLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_FLAGS Register is volatile, that is, a reset signal from the reset push button resets the SYS_FLAGS Register.

You use the SYS_FLAGSSET Register to set bits in the SYS_FLAGS Register. Write 1 to set the associated flag. Write 0 to leave the associated flag unchanged.

You use the SYS_FLAGSCLR Register to clear bits in the SYS_FLAGS Register. Write 0 to clear the associated flag. Write 1 to leave the associated flag unchanged.

SYS_NVFLAGS Register

The SYS_NVFLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_NVFLAGS Register is non-volatile, that is, a reset signal from the reset push button does not reset the SYS_FLAGS Register. Only **CB_nPOR** resets the SYS_NVFLAGS Register.

You use the SYS_NVFLAGSSET Register to set bits in the SYS_NVFLAGS Register. Write 1 to set the associated flag. Write 0 to leave the associated flag unchanged.

You use the SYS_NVFLAGSCLR Register to clear bits in the SYS_NVFLAGS Register. Write 0 to clear the associated flag. Write 1 to leave the associated flag unchanged.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.7 SYS_CFGSW Register

The SYS_CFGSW Register characteristics are:

Purpose
Contains the value of *CONFSWITCH* in the `config.txt` file.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

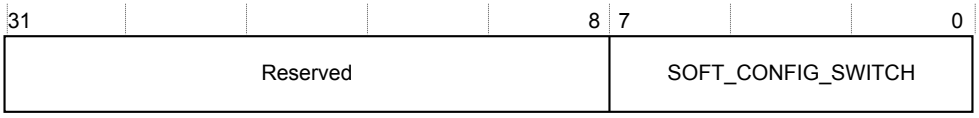

Figure 4-8 SYS_CFGSW Register bit assignments

The following table shows the bit assignments.

Table 4-9 SYS_CFGSW Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved. Do not write to or read from these bits.
[7:0]	SOFT_CONFIG_SWITCH	Software applications can read these switch settings. The application software defines the meanings of the switch settings. The reset signals sets these bits to the value of *CONFSWITCH* in the `config.txt` file. ——— **Note** ——— The configuration system does not use the contents of this register for board configuration. ———————————

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.8 SYS_24MHZ Register

The SYS_24MHZ Register characteristics are:

Purpose
A 32-bit counter that updates at 24MHz. The clock source is the 24MHz clock generator on the V2M-Juno motherboard.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

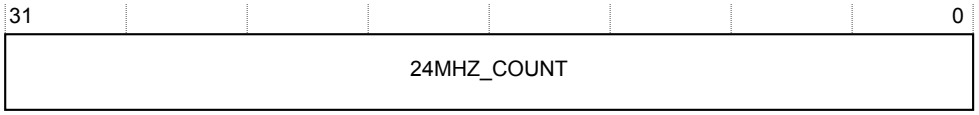

Figure 4-9 SYS_24MHZ Register bit assignments

The following table shows the bit assignments.

Table 4-10 SYS_24MHZ Register bit assignments

Bits	Name	Function
[31:0]	24MHZ_COUNT	Contains the count, at 24MHz, from the last **CB_nRST** reset. **CB_nRST** sets the register to zero and then the count resumes.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.9 SYS_MISC Register

The SYS_MISC Register characteristics are:

Purpose
Denotes presence or absence of LogicTile Express daughterboard fitted in daughterboard site.

Usage constraints
Bit[19] is read-write. Bit[13] is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

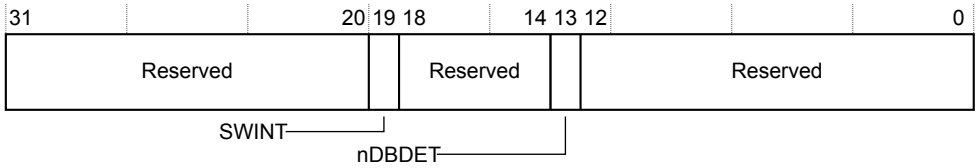

Figure 4-10 SYS_MISC Register bit assignments

The following table shows the bit assignments.

Table 4-11 SYS_MISC Register bit assignments

Bits	Name	Function
[31:20]	-	Reserved. Do not write to or read from these bits.
[19]	SWINT	Event output to daughterboard. See your daughterboard documentation for more information specific to your board.
[18:14]	-	Reserved. Do not write to or read from these bits.
[13]	nDBDET	Detect fitted daughterboard: • `0b0` Daughterboard not present. • `0b1` Daughterboard present.
[12:0]	-	Reserved. Do not write to or read from these bits.

4.3.10 SYS_PROC_ID0 Register

The SYS_PROC_ID0 Register characteristics are:

Purpose
Identifies the active clusters in the Juno SoC.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

Figure 4-11 SYS_PROC_ID0 Register bit assignments

The following table shows the bit assignments.

Table 4-12 SYS_PROC_ID0 Register bit assignments

Bits	Name	Function
[31:24]	PROC_ID0	Denotes active clusters, Cortex-A57, Cortex-A53 and Mali-T624 GPU.
[23:0]	-	Reserved. Do not write to or read from these bits.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.11 SYS_PROC_ID1 Register

The SYS_PROC_ID1 Register characteristics are:

Purpose
Contains identification information about the FPGA image and the LogicTile Express daughterboard fitted to the V2M-Juno motherboard.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

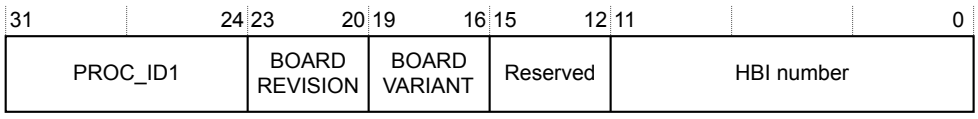

Figure 4-12 SYS_PROC_ID1 Register bit assignments

The following table shows the bit assignments.

Table 4-13 SYS_PROC_ID1 Register bit assignments

Bits	Name	Function
[31:24]	PROC_ID1	Denotes Application note or FPGA image in LogicTile daughterboard.
[23:20]	BOARD REVISION	Denotes the daughterboard revision: • `0x0` A. • `0x1` B. • `0x2` C.
[19:16]	BOARD VARIANT	Denotes the daughterboard variant: • `0x0` A. • `0x1` B. • `0x2` C.
[15:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	HBI board number	Denotes the HBI board number of the LogicTile Express daughterboard: • `0x192` HBI0192. • `0x217` HBI0217. • `0x247` HBI0247.

Related concepts

4.3.1 APB system register summary on page 4-87.

4.3.12 SYS_FAN_DATA Register

The SYS_FAN_DATA Register characteristics are:

Purpose
Contains a value that represents the operating temperature of the Juno SoC. The MCC uses this value to moderate the speed of the cooling fan on the V2M-Juno motherboard.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

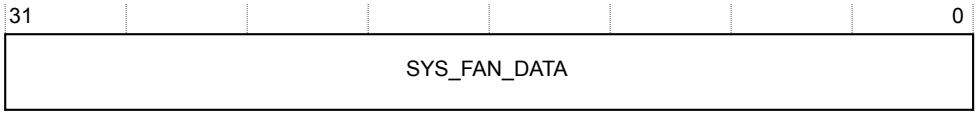

Figure 4-13 SYS_FAN_DATA Register bit assignments

The following table shows the bit assignments.

Table 4-14 SYS_FAN_DATA Register bit assignments

Bits	Name	Function
[31:0]	SYS_FAN_DATA	Operating temperature of the Juno SoC.

4.4 APB system configuration registers

This section describes the APB system configuration registers in the IOFPGA.

This section contains the following subsections:

4.4.1 APB system configuration register summary

This section summarizes the characteristics of the V2M-Juno motherboard APB system configuration registers in the IOFPGA.

The base memory address of the APB system configuration registers is `0x1C010000`. The following table shows the registers in address offset order from the base memory address.

Table 4-15 V2M-Juno motherboard APB system configuration register summary

Offset	Name	Type	Reset	Width	Comment
`0x00A0`	SYS_CFGDATA	RW	`0x00000000`	32	Contains read and write data for communications between the MCC and components on the V2M-Juno motherboard or LogicTile daughterboard.
`0x00A4`	SYS_CFGCTRL	RW	`0x00000000`	32	Control register for read and write operations between the MCC and V2M-Juno motherboard or LogicTile daughterboard components.
`0x00A8`	SYS_CFGSTAT	RW	`0x00000000`	32	Reports the status of read and write operations between the MCC and V2M-Juno motherboard or LogicTile daughterboard components.

4.4.2 SYS_CFGDATA Register

The SYS_CFGDATA_OUT Register characteristics are:

Purpose

The application software in the Juno SoC writes data to the SYS_CFGDATA Register during a write operation. This data represents a value or function that the write operation sends to the addressed component, for example a frequency value to a clock generator.

The MCC or Daughterboard Configuration Controller writes return data to the SYS_CFGDATA Register during a read operation. This data represents a value or function that the read operation receives from the addressed component, for example the frequency value of a clock generator.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

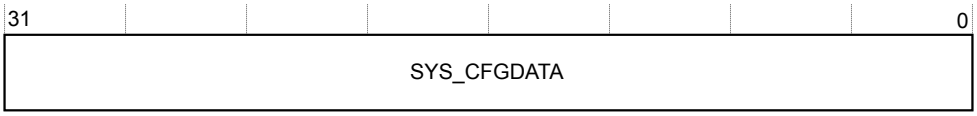

Figure 4-14 SYS_CFGDATA_OUT Register bit assignments

The following table shows the bit assignments.

Table 4-16 SYS_CFGDATA_OUT Register bit assignments

Bits	Name	Function
[31:0]	SYS_CFGDATA	Write-data or read-data.

Related concepts

4.4.1 APB system configuration register summary on page 4-96.

4.4.3 SYS_CFGCTRL Register

The SYS_CFGCTRL Register characteristics are:

Purpose
Controls write and read data transfer between the MCC and the SCC interface in the FPGA.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

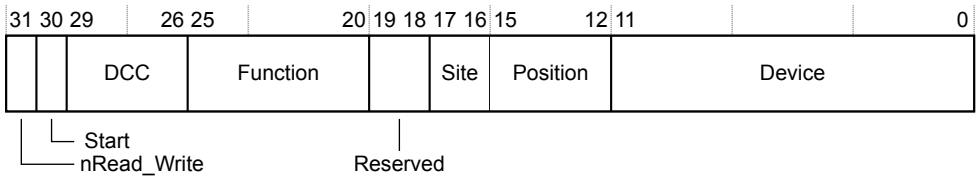

Figure 4-15 SYS_CFGCTRL Register bit assignments

The following table shows the bit assignments.

Table 4-17 SYSCFG_CTRL Register bit assignments

Bits	Name	Function
[31]	Start	Writing to this bit generates an interrupt.
[30]	nRead_Write	• `0b0` Read access. • `0b1` Write access.
[29:26]	DCC	4-bit number that selects Daughterboard Configuration Controller on daughterboard. For example: • `0x0` selects DCC 0. • `0x1` selects DCC 1.

Table 4-17 SYSCFG_CTRL Register bit assignments (continued)

Bits	Name	Function
[25:20]	Function	6-bit value that defines the function of the daughterboard device that the transaction writes to or reads from. These bits support the following functions: • `0b000001` Clock generator. • `0b000100` Temperature. • `0b000101` Daughterboard reset register. • `0b000110` SCC configuration register. • `0b001000` Shut down system. • `0b001001` Reboot system.
[19:18]	-	Reserved. Do not write to these bits.
[17:16]	Site	Selects the board site location of the device to write to or read from. The V2M-Juno motherboard supports the following locations: • `0b00` V2M-Juno motherboard. • `0b01` LogicTile Express daughterboard site.
[15:12]	Position	Selects position of the daughterboard in the stack. For example: • `0x0` V2M-Juno motherboard. • `0x1` Daughterboard at lowest position in stack next to V2M-Juno motherboard. • `0x2` Daughterboard 2 in stack.
[11:0]	Device	12-bit number that denotes the device number. For example: • `0x000` selects device 0. • `0x001` selects device 1.

Related concepts

4.4.1 APB system configuration register summary on page 4-96.

4.4.4 SYS_CFGSTAT Register

The SYS_CFGSTAT Register characteristics are:

Purpose
Contains system configuration status information about read and write operations between the application software in the Juno SoC and a component on a fitted LogicTile Express daughterboard or the V2M-Juno motherboard.

Usage constraints
The SYS_CFGSTAT Register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

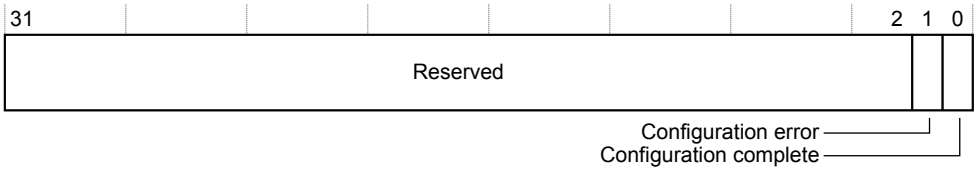

Figure 4-16 SYS_CFGSTAT Register bit assignments

The following table shows the bit assignments.

Table 4-18 SYS_CFGSTAT Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Do not write to these bits.
[1]	Configuration error	A write to SYS_CFGCTRL clears this bit: • `0b0` Configuration successful. • `0b1` Configuration failed.
[0]	Configuration complete	A write to SYS_CFGCTRL clears this bit: • `0b0` Configuration not complete. • `0b1` Configuration complete.

Related concepts

4.4.1 APB system configuration register summary on page 4-96.

4.5 APB energy meter registers

This section describes the APB energy meter registers in the IOFPGA.

This section contains the following subsections:

4.5.1 APB energy register summary

This section summarizes the characteristics of the V2M-Juno motherboard APB energy meter registers in the IOFPGA.

The IOFPGA provides energy registers that measure the instantaneous current consumption, instantaneous voltage supplies, instantaneous power consumption and cumulative energy consumption of the Cortex-A57 cluster, the Cortex-A53 cluster, the Mali-T624 GPU cluster and the fabric of the Juno ARM Development Platform SoC outside the clusters.

The following table shows the energy registers in offset order from the APB registers base memory address of `0x1C010000`.

Table 4-19 V2M-Juno motherboard SCC register summary

Offset	Name	Type	Reset	Width	Comment
`0x00D0`	SYS_ADC_CH0_PM1_SYS	RO	`0x00000000`	32	Instantaneous value of current consumption of the Juno SoC outside the clusters.
`0x00D4`	SYS_ADC_CH1_PM2_A57	RO	`0x00000000`	32	Instantaneous value of current consumption of the Cortex-A57 cluster.
`0x00D8`	SYS_ADC_CH2_PM3_A53	RO	`0x00000000`	32	Instantaneous value of current consumption of the Cortex-A53 cluster.
`0x00DC`	SYS_ADC_CH3_PM4_GPU	RO	`0x00000000`	32	Instantaneous value of current consumption of the Mali-T624 GPU cluster.
`0x00E0`	SYS_ADC_CH4_VSYS	RO	`0x00000000`	32	Instantaneous value of supply voltage of the Juno SoC outside the clusters.
`0x00E4`	SYS_ADC_CH5_VA57	RO	`0x00000000`	32	Instantaneous value of supply voltage of the Cortex-A57 cluster.

Table 4-19 V2M-Juno motherboard SCC register summary (continued)

Offset	Name	Type	Reset	Width	Comment
0x00E8	SYS_ADC_CH6_VA53	RO	0x00000000	32	Instantaneous value of supply voltage of the Cortex-A53 cluster.
0x00EC	SYS_ADC_CH7_VGPU	RO	0x00000000	32	Instantaneous value of supply voltage of the Mali-T624 GPU cluster.
0x00F0	SYS_EN_CH04_SYS	RO	0x00000000	32	Instantaneous value of power consumption of the Juno SoC outside the clusters.
0x00F4	SYS_EN_CH15_A57	RO	0x00000000	32	Instantaneous value of power consumption of the Cortex-A57 cluster.
0x00F8	SYS_EN_CH26_A53	RO	0x00000000	32	Instantaneous value of power consumption of the Cortex-A53 cluster.
0x00FC	SYS_EN_CH37_GPU	RO	0x00000000	32	Instantaneous value of power consumption of the Mali-T624 GPU cluster.
0x0100	SYS_ENM_CH0_L_SYS	RW	0x00000000	32	Lower 32 bits of 64-bit energy meter for the Juno SoC fabric. Stores accumulated value of energy consumed by the Juno SoC outside the clusters.
0x0104	SYS_ENM_CH0_H_SYS	RW	0x00000000	32	Upper 32 bits of 64-bit energy meter for the Juno SoC fabric. Stores accumulated value of energy consumed by the Juno SoC outside the clusters.
0x0108	SYS_ENM_CH1_L_A57	RW	0x00000000	32	Lower 32 bits of the Cortex-A57 64-bit energy meter. Stores accumulated value of energy consumed by the Cortex-A57 cluster.
0x010C	SYS_ENM_CH1_H_A57	RW	0x00000000	32	Upper 32 bits of the Cortex-A57 64-bit energy meter. Stores accumulated value of energy consumed by the Cortex-A57 cluster.
0x0110	SYS_ENM_CH0_L_A53	RW	0x00000000	32	Lower 32 bits of the Cortex-A53 64-bit energy meter. Stores accumulated value of energy consumed by the the Cortex-A53 cluster.
0x0114	SYS_ENM_CH0_H_A53	RW	0x00000000	32	Upper 32 bits of the Cortex-A53 64-bit energy meter. Stores accumulated value of energy consumed by the Cortex-A53 cluster.
0x0118	SYS_ENM_CH0_L_GPU	RW	0x00000000	32	Lower 32 bits of the Mali-T624 GPU 64-bit energy meter. Stores accumulated value of energy consumed by the Mali-T624 GPU cluster.
0x011C	SYS_ENM_CH0_H_GPU	RW	0x00000000	32	Upper 32 bits of the Mali-T624 GPU 64-bit energy meter. Stores accumulated value of energy consumed by the Mali-T624 GPU cluster.

4.5.2 SYS_ADC_CH0_PM1_SYS Register

The SYS_ADC_CH0_PM1_SYS Register characteristics are:

Purpose

Holds a 12-bit representation of the instantaneous current consumption of the Juno SoC outside the clusters.

Usage constraints

This register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

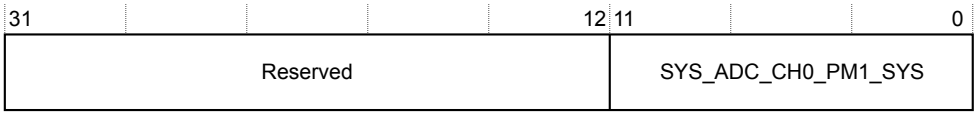

Figure 4-17 SYS_ADC_CH0_PM1_SYS Register bit assignments

The following table shows the bit assignments.

Table 4-20 SYS_ADC_CH0_PM1_SYS Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH0_PM1_SYS	12-bit representation of the instantaneous current consumption of the Juno SoC outside the clusters: • Full scale measurement, 4096, represents 5A. Full scale is FFF. • Measured current = (SYS_ADC_CH0_PM1_SYS+1)/819.2 amperes. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts
4.5.1 APB energy register summary on page 4-100.

4.5.3 SYS_ADC_CH1_PM2_A57 Register

The SYS_ADC_CH1_PM2_A57 Register characteristics are:

Purpose
Holds a 12-bit representation of the instantaneous current consumption of the Cortex-A57 cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

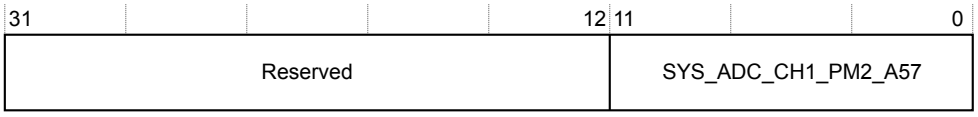

Figure 4-18 SYS_ADC_CH1_PM2_A57 Register bit assignments

The following table shows the bit assignments.

Table 4-21 SYS_ADC_CH1_PM2_A57 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH1_PM2_A57	12-bit representation of current consumption of the Cortex-A57 cluster: • Full scale measurement, 4096, represents 10A. Full scale is FFF. • Measured current = (SYS_ADC_CH1_PM2_A57+1)/409.6 amperes. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.4 SYS_ADC_CH2_PM3_A53 Register

The SYS_ADC_CH2_PM3_A53 Register characteristics are:

Purpose

Holds a 12-bit representation of the instantaneous current consumption of the Cortex-A53 cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

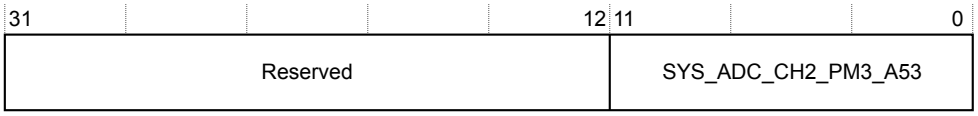

Figure 4-19 SYS_ADC_CH2_PM3_A53 Register bit assignments

The following table shows the bit assignments.

Table 4-22 SYS_ADC_CH2_PM3_A53 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH2_PM3_A53	12-bit representation of current consumption of the Cortex-A53 cluster: • Full scale measurement, 4096, represents 5A. Full scale is FFF. • Measured current = (SYS_ADC_CH2_PM3_A53+1)/819.2 amperes. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.5 SYS_ADC_CH3_PM4_GPU Register

The SYS_ADC_CH3_PM4_GPU Register characteristics are:

Purpose

This register holds a 12-bit representation of the instantaneous current consumption of the Mali-T624 GPU cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

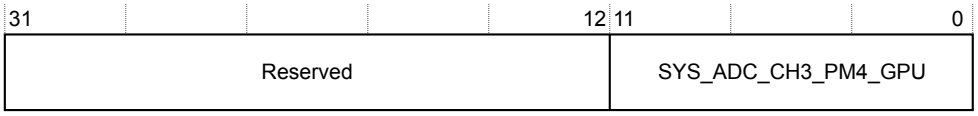

Figure 4-20 SYS_ADC_CH3_PM4_GPU Register bit assignments

The following table shows the bit assignments.

Table 4-23 SYS_ADC_CH3_PM4_GPU Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH3_PM4_GPU	12-bit representation of current consumption of the Mali-T624 GPU cluster: • Full scale measurement, 4096, represents 10A. Full scale is FFF. • Measured current = (SYS_ADC_CH3_PM4_GPU+1)/409.6 amperes. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.6 SYS_ADC_CH4_VSYS Register

The SYS_ADC_CH4_VSYS Register characteristics are:

Purpose

Holds a 12-bit representation of the instantaneous supply voltage of the Juno SoC outside the clusters.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

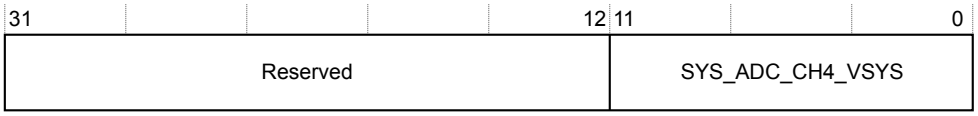

Figure 4-21 SYS_ADC_CH4_VSYS Register bit assignments

The following table shows the bit assignments.

Table 4-24 SYS_ADC_CH4_VSYS Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH4_VSYS	12-bit representation of the instantaneous supply voltage of the Juno SoC outside the clusters: • Full scale measurement, 4096, represents 2V5. Full scale is FFF. • Measured voltage = (SYS_ADC_CH4_VSYS+1)/1638.4 volts. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.7 SYS_ADC_CH5_VA57 Register

The SYS_ADC_CH5_VA57 Register characteristics are:

Purpose

Holds a 12-bit representation of the instantaneous supply voltage of the Cortex-A57 cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

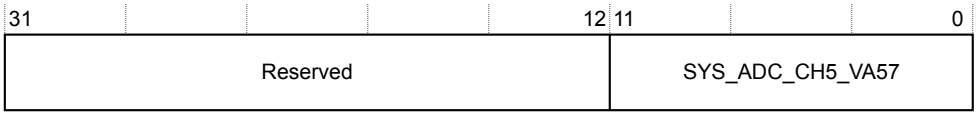

Figure 4-22 SYS_ADC_CH5_VA57 Register bit assignments

The following table shows the bit assignments.

Table 4-25 SYS_ADC_CH5_VA57 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH5_VA57	12-bit representation of the instantaneous supply voltage of the Cortex-A57 cluster: • Full scale measurement, 4096, represents 2V5. Full scale is FFF. • Measured voltage = (SYS_ADC_CH5_VA57+1)/1638.4 volts. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.8 SYS_ADC_CH6_VA53 Register

The SYS_ADC_CH6_VA53 Register characteristics are:

Purpose

Holds a 12-bit representation of the instantaneous supply voltage of the Cortex-A53 cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

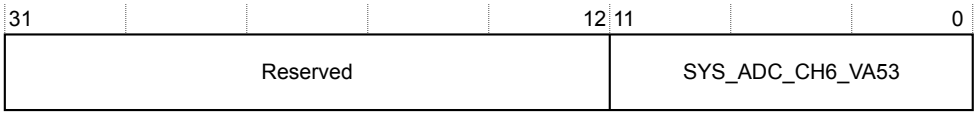

Figure 4-23 SYS_ADC_CH6_VA53 Register bit assignments

The following table shows the bit assignments.

Table 4-26 SYS_ADC_CH6_VA53 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH6_VA53	12-bit representation of the instantaneous supply voltage of the Cortex-A53 cluster: • Full scale measurement, 4096, represents 2V5. Full scale is FFF. • Measured voltage = (SYS_ADC_CH6_VA53+1)/1638.4 • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.9 SYS_ADC_CH7_VGPU Register

The SYS_ADC_CH7_VGPU Register characteristics are:

Purpose
Holds a 12-bit representation of the instantaneous supply voltage of the Mali-T624 GPU cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

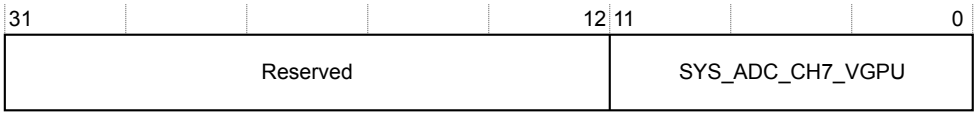

Figure 4-24 SYS_ADC_CH7_VGPU Register bit assignments

The following table shows the bit assignments.

Table 4-27 SYS_ADC_CH7_VGPU Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Do not write to or read from these bits.
[11:0]	SYS_ADC_CH7_VGPU	12-bit representation of the instantaneous supply voltage of the Mali-T624 GPU cluster: • Full scale measurement, 4096, represents 2V5. Full scale is FFF. • Measured voltage = (SYS_ADC_CH7_VGPU+1)/1638.4 volts. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.10 SYS_POW_CH04_SYS Register

The SYS_POW_CH04_SYS Register characteristics are:

Purpose

Holds a 24-bit representation of the instantaneous power consumption of the Juno SoC outside the clusters.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

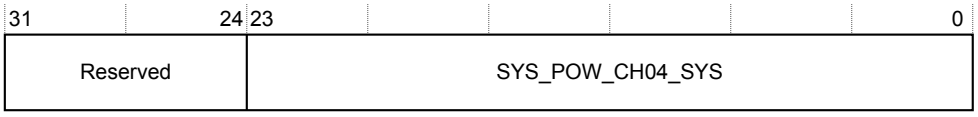

Figure 4-25 SYS_POW_CH04_SYS Register bit assignments

The following table shows the bit assignments.

Table 4-28 SYS_POW_CH04_SYS Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. Do not write to or read from these bits.
[23:0]	SYS_POW_CH04_SYS	24-bit representation of the instantaneous power consumption of the Juno SoC outside the clusters: • The value of these bits represents [SYS_ADC_CH0_PM1_SYS(I) x SYS_ADC_CH4_VSYS(V)]/1342177.28 watts. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.11 SYS_POW_CH15_A57 Register

The SYS_POW_CH15_A57 Register characteristics are:

Purpose

Holds a 24-bit representation of the instantaneous power consumption of the Cortex-A57 cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

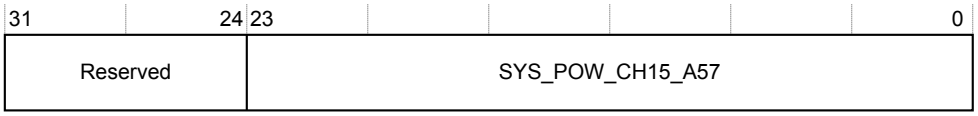

Figure 4-26 SYS_POW_CH15_A57 Register bit assignments

The following table shows the bit assignments.

Table 4-29 SYS_POW_CH15_A57 Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. Do not write to or read from these bits.
[23:0]	SYS_POW_CH15_A57	24-bit representation of the instantaneous power consumption of the Cortex-A57 cluster: • The value of these bits represents [SYS_ADC_CH1_PM2_A57(I) x SYS_ADC_CH5_VA57(V)]/671088.64 watts. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.12 SYS_POW_CH26_A53 Register

The SYS_POW_CH26_A53 Register characteristics are:

Purpose

Holds a 24-bit representation of the instantaneous power consumption of the Cortex-A53 cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

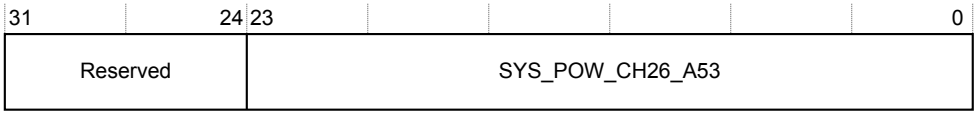

Figure 4-27 SYS_POW_CH26_A53 Register bit assignments

The following table shows the bit assignments.

Table 4-30 SYS_POW_CH26_A53 Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. Do not write to or read from these bits.
[23:0]	SYS_POW_CH26_A53	24-bit representation of the instantaneous power consumption of the Cortex-A53 cluster: • The value of these bits represents [SYS_ADC_CH2_PM3_A53 (I) x SYS_ADC_CH6_VA53(V)]/1342177.28 watts. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.13 SYS_POW_CH37_GPU Register

The SYS_POW_CH37_GPU Register characteristics are:

Purpose

Holds a 24-bit representation of the instantaneous power consumption of the Mali-T624 GPU cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

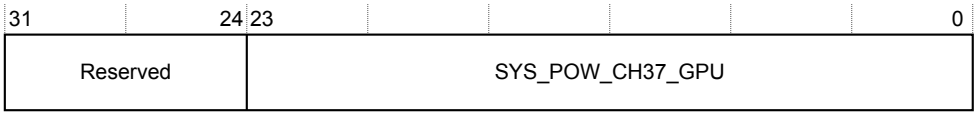

Figure 4-28 SYS_POW_CH37_GPU Register bit assignments

The following table shows the bit assignments.

Table 4-31 SYS_POW_CH37_GPU Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. Do not write to or read from these bits.
[23:0]	SYS_POW_CH37_GPU	24-bit representation of the instantaneous power consumption of the Mali-T624 GPU cluster: • The value of these bits represents [SYS_ADC_CH3_PM4_GPU (I) x SYS_ADC_CH7_VGPU(V)]/671088.64 watts. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.14 SYS_ENM_CH0_SYS Register

The SYS_ENM_CH0_SYS Register characteristics are:

Purpose

Holds a 64-bit representation of the accumulated energy consumption of the fabric of the Juno SoC outside the clusters.

Usage constraints

Writing to this register clears the 64-bit value.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

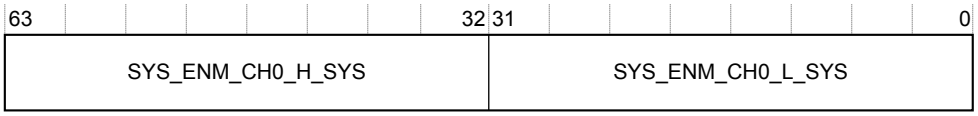

Figure 4-29 SYS_ENM_CH0_SYS Register bit assignments

The following table shows the bit assignments.

Table 4-32 SYS_ENM_CH0_SYS Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_CH0_H_SYS	Most significant 32 bits of a 64-bit representation of the accumulated energy energy consumption of the fabric of the Juno SoC outside the clusters: • The memory address offset of these bits is `0x0104`. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset. • See Function description for bits[31:0] for information on the 64-bit energy measurement.
[31:0]	SYS_ENM_CH0_L_SYS	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the fabric of the Juno SoC outside the clusters: • The memory address offset of these bits is `0x0100`. • Accumulated energy in Joules = (SYS_ENM_CH0_H_SYS:SYS_ENM_CH0_SYS)/13421772800 • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.15 SYS_ENM_CH1_A57 Register

The SYS_ENM_CH1_A57 Register characteristics are:

Purpose

Holds a 64-bit representation of the accumulated energy consumption of the Cortex-A57 cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

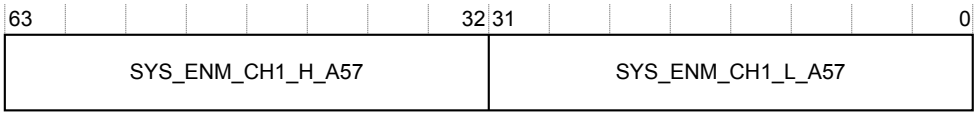

Figure 4-30 SYS_ENM_CH1_A57 Register bit assignments

The following table shows the bit assignments.

Table 4-33 SYS_ENM_CH1_A57 Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_CH1_H_A57	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Cortex-A57 cluster: • The memory address offset of these bits is `0x010C`. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset. • See Function description for bits[31:0] for information on the 64-bit energy measurement.
[31:0]	SYS_ENM_CH1_L_A57	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Cortex-A57 cluster: • The memory address offset of these bits is `0x0108`. • Accumulated energy in = (SYS_ENM_CH1_H_A57:SYS_ENM_CH1_A57)/ 6710886400 joules. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.16 SYS_ENM_CH0_A53 Register

The SYS_ENM_CH0_A53 Register characteristics are:

Purpose
Holds a 64-bit representation of the accumulated energy consumption of the Cortex-A53 cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

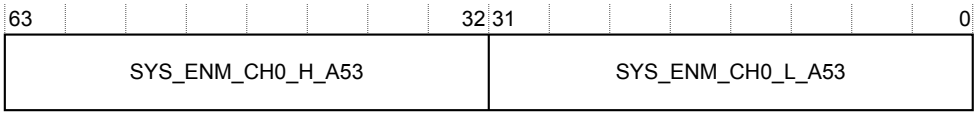

Figure 4-31 SYS_ENM_CH0_A53 Register bit assignments

The following table shows the bit assignments.

Table 4-34 SYS_ENM_CH0_A53 Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_CH0_H_A53	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of Cortex-A53 cluster: • The memory address offset of these bits is `0x0114`. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset. • See Function description for bits[31:0] for information on the 64-bit energy measurement.
[31:0]	SYS_ENM_CH0_L_A53	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of Cortex-A53 cluster: • The memory address offset of these bits is `0x0110`. • Accumulated energy = (SYS_ENM_CH0_H_A53:SYS_ENM_CH0_L_A53)/ 13421772800 joules. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

4.5.17 SYS_ENM_CH0_GPU Register

The SYS_ENM_CH0_GPU Register characteristics are:

Purpose

Holds a 64-bit representation of the accumulated energy consumption of the Mali-T624 GPU cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno motherboard configurations.

The following figure shows the bit assignments.

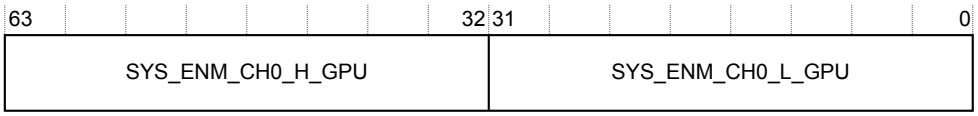

Figure 4-32 SYS_ENM_CH0_GPU Register bit assignments

The following table shows the bit assignments.

Table 4-35 SYS_ENM_CH0_GPU Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_CH0_H_GPU	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Mali-T624 GPU cluster: • The memory address offset of these bits is `0x011C`. • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset. • See Function description for bits[31:0] for information on the 64-bit energy measurement.
[31:0]	SYS_ENM_CH0_L_GPU	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Mali-T624 GPU cluster: • The memory address offset of these bits is `0x0118`. • Accumulated energy in = (SYS_ENM_CH0_H_GPU:SYS_ENM_CH0_L_GPU)/6710886400 joules • The reset signal **CB_nRST** resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-100.

Appendix A.1
Signal Descriptions

This appendix describes the signals present at the interface connectors of the Versatile Express V2M-Juno motherboard.

It contains the following sections:

A.1.1 Debug connectors

This section describes the debug connectors on the V2M-Juno motherboard and lists their signals.

This section contains the following subsections:

P-JTAG connector

The V2M-Juno motherboard provides one P-JTAG connector.

The P-JTAG connector also supports *Serial Wire Debug* (SWD).

The V2M-Juno motherboard labels the P-JTAG connector as *CS_JTAG*.

The following figure shows the P-JTAG connector, J25.

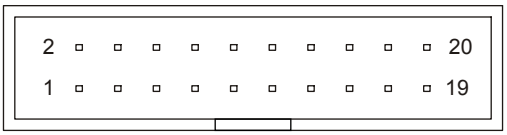

Figure A-1 P-JTAG connector

The following table shows the pin mapping for the P-JTAG signals on the P-JTAG connector, J25.

Table A-1 P-JTAG connector, J25, signal list

Pin	Signal	Pin	Signal
1	**VTREFC (1V8)**	2	**CS_BS_VSUPPLY (1V8)**
3	**nTRST**	4	**GND**
5	**TDI**	6	**GND**
7	**SWDIO/TMS**	8	**GND**
9	**SWDCLK/TCK**	10	**GND**
11	**GND/RTCK**	12	**GND**
13	**SWO/TDO**	14	**GND**
15	**nSRST**	16	**GND**
17	No connection/**EDBGRQ**	18	**GNDDETECT**
19	No connection/**DBGACK**	20	**GND**

Note

- Pins 9 and 17 have pulldown resistors to 0V.
- Pin 11 has a pulldown resistor to 0V. V2M-Juno motherboard does not support adaptive clocking.
- Pins 3, 5, 7, 13, 15, and 19 have pullup resistors to 1V8.
- Pins 7 and 9 are dual-mode pins that enable the Juno SoC to support both the JTAG and SWD protocols.

Related concepts

2.16 Debug and trace on page 2-56.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

Trace connectors

The V2M-Juno motherboard provides two debug connectors that together support 32-bit trace.

The Juno ARM Development Platform SoC supports up to 32-bit trace output from the *CoreSight Trace Port Interface Unit* (TPIU) and enables connection of a compatible trace unit. Two MICTOR trace connectors, labeled *TRACEA-SINGLE* and *TraceB DUAL*, connect to the TPIU.

The two connectors support 32-bit trace when you use them together. The *TRACEA-SINGLE* connector, when you use it alone, supports 16-bit trace.

The connectors also support *Serial Wire Debug* (SWD).

Note

- *DSTREAM* is an example of a trace module that you can use.
- All trace and SWD signals operate at 1.8V.
- The trace connectors cannot supply power to a trace unit.

The following figure shows the MICTOR 38 connector.

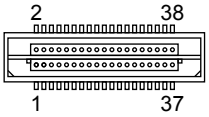

Figure A-2 MICTOR 38 connector, J27 and J28

The following table shows the pin mapping for the Trace and SWD signals on the *TRACEA-SINGLE* connector, J28.

Table A-2 TraceA-SINGLE connector, J28, signal list

Pin	Signal	Pin	Signal
1	No connection	2	No connection
3	No connection	4	No connection
5	**GND**	6	**TRACE_CLKA**
7	**EDBGRQ**	8	**DBGACK**
9	No connection/**nSRST**	10	**GND**
11	**TDO/SWO**	12	**1V8** reference
13	**RTCK**	14	**1V8_OUT**
15	**TCK/SWCLK**	16	**TRACEDATA[7]**
17	**TMS/SWDIO**	18	**TRACEDATA[6]**
19	**TDI**	20	**TRACEDATA[5]**
21	**nTRST**	22	**TRACEDATA[4]**
23	**TRACEDATA[15]**	24	**TRACEDATA[3]**
25	**TRACEDATA[14]**	26	**TRACEDATA[2]**
27	**TRACEDATA[13]**	28	**TRACEDATA[1]**

Table A-2 TraceA-SINGLE connector, J28, signal list (continued)

Pin	Signal	Pin	Signal
29	**TRACEDATA[12]**	30	**GND**
31	**TRACEDATA[11]**	32	**GNDDETECT**
33	**TRACEDATA[10]**	34	**1V8** reference
35	**TRACEDATA[9]**	36	**TRACECTL**
37	**TRACEDATA[8]**	38	**TRACEDATA[0]**

Note

- The trace connector cannot supply power to a trace unit.
- The interface does not support the **TRACECTL** signal. The Juno SoC always drives this signal LOW.

The following table shows the pin mapping for the Trace signals on the *TraceB DUAL* connector, J27.

Table A-3 Trace B connector, J27, signal list

Pin	Signal	Pin	Signal
1	No connection	2	No connection
3	No connection	4	No connection
5	**GND**	6	**TRACE_CLKB**
7	No connection	8	No connection
9	No connection	10	No connection
11	No connection	12	**1V8** reference
13	No connection	14	No connection
15	No connection	16	**TRACEDATA[23]**
17	No connection	18	**TRACEDATA[22]**
19	No connection	20	**TRACEDATA[21]**
21	No connection	22	**TRACEDATA[20]**
23	**TRACEDATA[31]**	24	**TRACEDATA[19]**
25	**TRACEDATA[30]**	26	**TRACEDATA[18]**
27	**TRACEDATA[29]**	28	**TRACEDATA[17]**
29	**TRACEDATA[28]**	30	**GND**
31	**TRACEDATA[27]**	32	**GND**
33	**TRACEDATA[26]**	34	**1V8** reference
35	**TRACEDATA[25]**	36	No connection
37	**TRACEDATA[24]**	38	**TRACEDATA[16]**

Related concepts

2.16 Debug and trace on page 2-56.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.2 Configuration 10Mbps Ethernet and dual-USB connector

The V2M-Juno motherboard provides one connector that supports 10Mbps Ethernet access to the microSD card and provides two of the four general-purpose dual-USB 2.0 ports on the board.

The configuration 10Mbps Ethernet connects to the Ethernet LAN controller in the MCC. You can use the configuration 10Mbps Ethernet port to perform Drag-and-Drop configuration file editing in the V2M-Juno motherboard microSD card.

The two USB 2.0 ports connect to the USB 4-port hub. They provide two of the four general-purpose USB 2.0 ports on the V2M-Juno motherboard.

The following figure shows the configuration 10Mbps Ethernet and dual-USB 2.0 connector, J40.

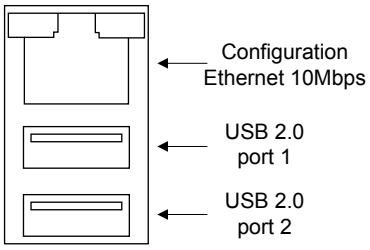

Figure A-3 Configuration 10Mbps Ethernet and dual-USB 2.0 connector, J40

Related concepts

2.11 USB 2.0 interface on page 2-50.

3.3.1 Overview of configuration files and microSD card directory structure on page 3-68.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.3 Dual-USB connector

The V2M-Juno motherboard provides a combined connector that provides two of the four general-purpose USB 2.0 ports on the board.

The two USB 2.0 ports connect to the USB 4-port hub. They provide two of the four general-purpose USB 2.0 ports on the V2M-Juno motherboard.

Note

ARM reserves the use of the Ethernet connector in the combined connector. Do not attempt to use the Ethernet connector.

The following figure shows the dual-USB 2.0 connector, J37.

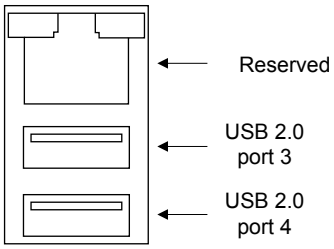

Figure A-4 Dual-USB 2.0 connector, J37

Related concepts

2.11 USB 2.0 interface on page 2-50.

V2M-Juno with PCI Express - Gigabit Ethernet port.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.4 SMC 10/100 Ethernet connector

The V2M-Juno motherboard provides one SMC 10/100 Ethernet connector.

The following figure shows the SMC 10/100 Ethernet connector, J50.

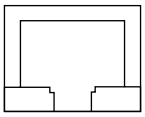

Figure A-5 SMC 10/100 Ethernet connector, J50

A.1.5 Configuration USB connector

The configuration USB connector provides access to the root directory and subdirectories of the microSD card.

You can use the configuration USB port to perform Drag-and-Drop configuration file editing in the V2M-Juno motherboard configuration microSD card.

The following figure shows the configuration USB 2.0 connector, J48.

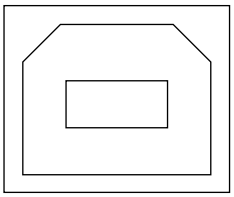

Figure A-6 Configuration USB 2.0 connector, J48

Related concepts

3.3.1 Overview of configuration files and microSD card directory structure on page 3-68.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.6 Header connectors

Two high-density header connectors enable you to fit a LogicTile FPGA board to the daughterboard site on the V2M-Juno motherboard.

Header X, J1, routes the Thin Links buses between the Juno ARM Development Platform SoC on the V2M-Juno motherboard and the FPGA on the LogicTile daughterboard fitted in the daughterboard site.

Header Y, J4, routes the buses and power interconnect between the V2M-Juno motherboard and the LogicTile FPGA daughterboard.

The constraints file `an415_rapper.xdc`, available in *Application Note AN415 Example LogicTile Express 20MG design for a V2M-Juno Motherboard*, lists the header signals.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.7 Keyboard and Mouse (KMI) connector

The V2M-Juno motherboard provides a dual mini-DIN connector that supports PS/2 keyboard and mouse input to the Juno ARM Development Platform SoC.

The following figure shows the dual-mini-DIN KMI connector, J59.

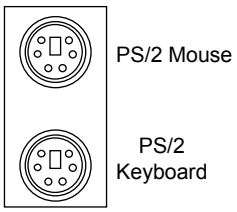

Figure A-7 Dual mini-DIN KMI connector, J59

Related concepts

2.14 Keyboard and mouse interface on page 2-53.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.8 HDMI connectors

The V2M-Juno motherboard provides two female HDMI connectors that provide digital video and digital audio to external displays.

The following figure shows the HDMI connectors, J53 and J54.

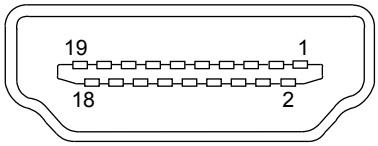

Figure A-8 HDMI connector

The following table shows the pin mapping for the HDMI signals, that include encoded I^2S digital audio, on the HDMI connectors.

Table A-4 HDMI connectors, J53 and J54, signal list

Pin	Signal	Pin	Signal
1	**DVI_TX2P**	2	**GND**
3	**DVI_TX2N**	4	**DVI_TX1P**
5	**GND**	6	**DVI_TX1N**
7	**DVI_TX0P**	8	**GND**
9	**DVI_TX0N**	10	**DVI_TXCP**
11	**GND**	12	**DVI_TXCN**
13	**DVI_CECAO**	14	No connection
15	**DVI_DSCLO**	16	**DVI_DSDAO**
17	**GND**	18	**DVI_5V0**
19	**DVI_HPDO**	-	-

Related concepts

2.9 HDLCD interface on page 2-45.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.9 Dual UART connector

The V2M-Juno motherboard provides one dual-UART connector that provides access to the MCC.

The UART port enables you to access the command-line interface in the MCC and perform application software debugging.

Note

The UART IO voltage at the connectors is 3.3V.

The following figure shows the dual UART connector, J57.

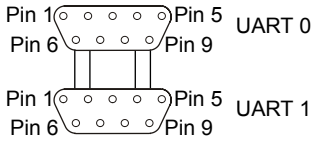

Figure A-9 Dual UART connector, J57

The following table shows the pin mapping for UART 0, the top connector of the dual UART connector, J57A.

Table A-5 UART 0 connector, J57A, signal list

Pin	Signal
A1	No connection
A2	**SER0_RX**
A3	**SER0_TX**
A4	**SER0_DTR**
A5	**GND**
A6	**SER0_DSR**
A7	**SER0_RTS**
A8	**SER0_CTS**
A9	No connection

The following table shows the pin mapping for UART 1, the bottom connector of the dual UART connector, J57B.

Table A-6 UART 1 connector, J57B, signal list

Pin	Signal
A1	No connection
A2	**SER1_RX**
A3	**SER1_TX**
A4	**SER1_DTR**
A5	**GND**
A6	**SER1_DSR**

Table A-6 UART 1 connector, J57B, signal list (continued)

Pin	Signal
A7	**SER1_RTS**
A8	**SER1_CTS**
A9	No connection

Related concepts

2.13 UART interface on page 2-52.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.10 Secure keyboard and user push buttons connector

This mini-DIN 9-pin connector provides support for additional key entry to the V2M-Juno motherboard.

The following figure shows the secure keyboard and user push buttons connector, J58.

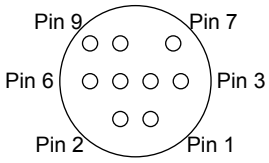

Figure A-10 Secure keyboard connector, J58

The following table shows the pin mapping for the secure keyboard and user push buttons connector, J58.

Table A-7 Secure keyboard and user push buttons connector, J58, signal list

Pin	Signal
1	**SEC_DF**
2	**SEC_PB0**
3	**GND**
4	**SEC_PB1**
5	**5V_KMI**
6	**SEC_CF**
7	**SEC_PB2**
8	**SEC_PB3**
9	**SEC_PB4**

Related concepts

2.15 Additional user key entry on page 2-54.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

A.1.11 ATX power connector

The V2M-Juno motherboard provides one power connector that enables connection of a unit that ARM supplies with the V2M-Juno motherboard. This unit converts AC mains power to DC power to supply the board.

The following figure shows the ATX power connector, J20.

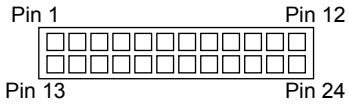

Figure A-11 ATX power connector, J20

The following table shows the pin mapping for the ATX power connector, J20, on the V2M-Juno motherboard.

Table A-8 ATX power connector, J20, signal list

Pin	Signal	Pin	Signal
1	**3V3**	13	**3V3**
2	**3V3**	14	**-12V**
3	**GND**	15	**GND**
4	**5V**	16	**nATXON**
5	**GND**	17	**GND**
6	**5V**	18	**GND**
7	**GND**	19	**GND**
8	**PWOK**	20	No connection
9	**SB_5V**	21	**5V**
10	**12V**	22	**5V**
11	**12V**	23	**5V**
12	**3V3**	24	**GND**

Related concepts

2.3 External power on page 2-24.

Related references

1.3 Location of components on the V2M-Juno motherboard on page 1-15.

Appendix B.2
Prototype V2M-Juno motherboard

This appendix describes the Versatile Express V2M-Juno motherboard that provides two SMC USB 2.0 ports.

It contains the following sections:

B.2.1 Overview of the prototype V2M-Juno motherboard

The prototype version of the V2M-Juno motherboard provides two SMC USB 2.0 ports that the production version does not provide.

The two SMC USB 2.0 ports connect to the SMC bus through the IOFPGA and have a dedicated chip select, CS5. The prototype board also provides all the features of the production version.

B.2.2 Location of components on the prototype V2M-Juno motherboard

The following figure shows the physical layout of the upper face of the prototype V2M-Juno motherboard.

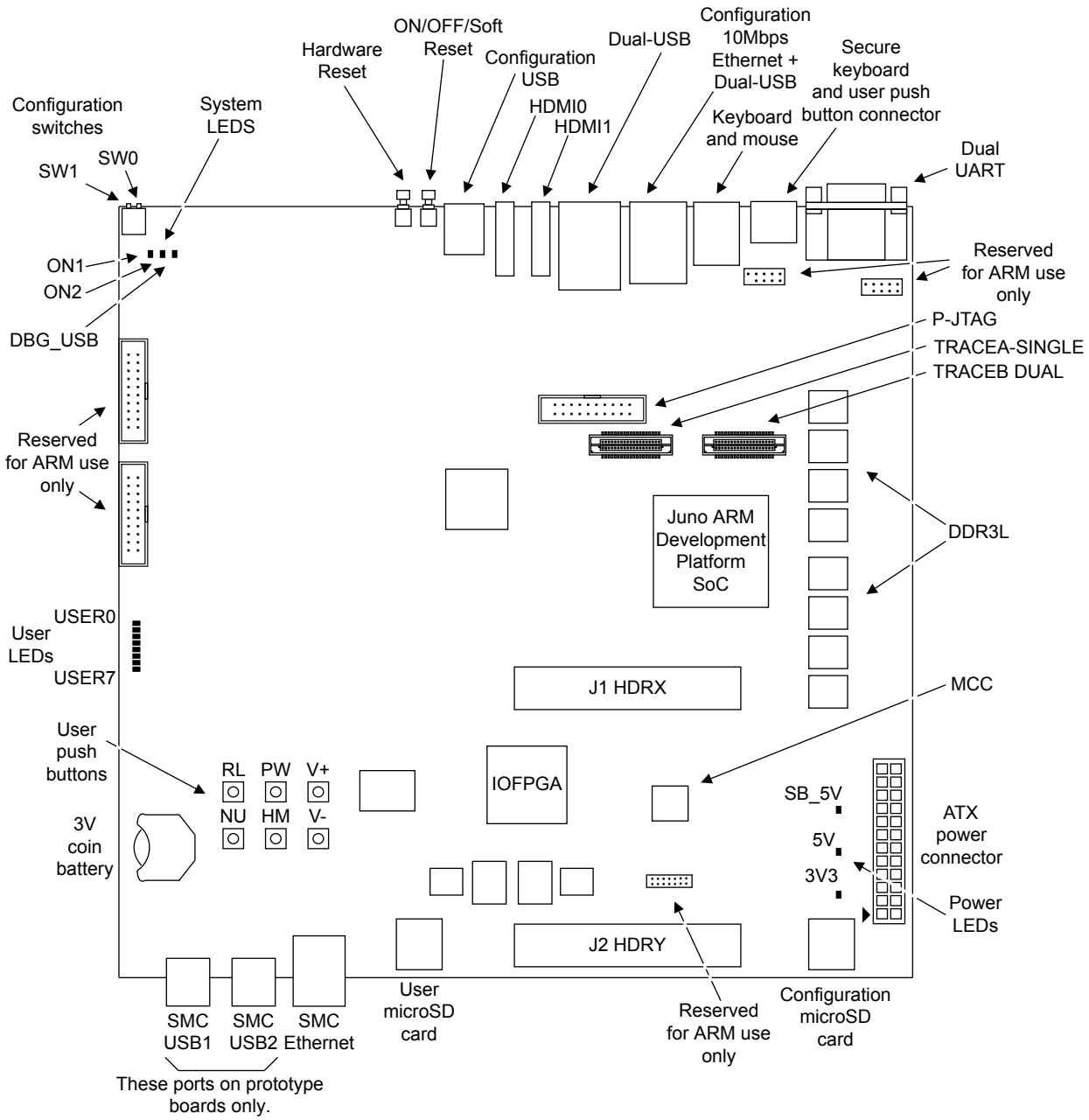

Figure B-1 Prototype V2M-Juno motherboard layout, upper face

B.2.3 IOFPGA internal architecture with SMC USB ports

The following figure shows the internal architecture, with SMC USB 2.0 ports, of the IOFPGA on the prototype V2M-Juno motherboard.

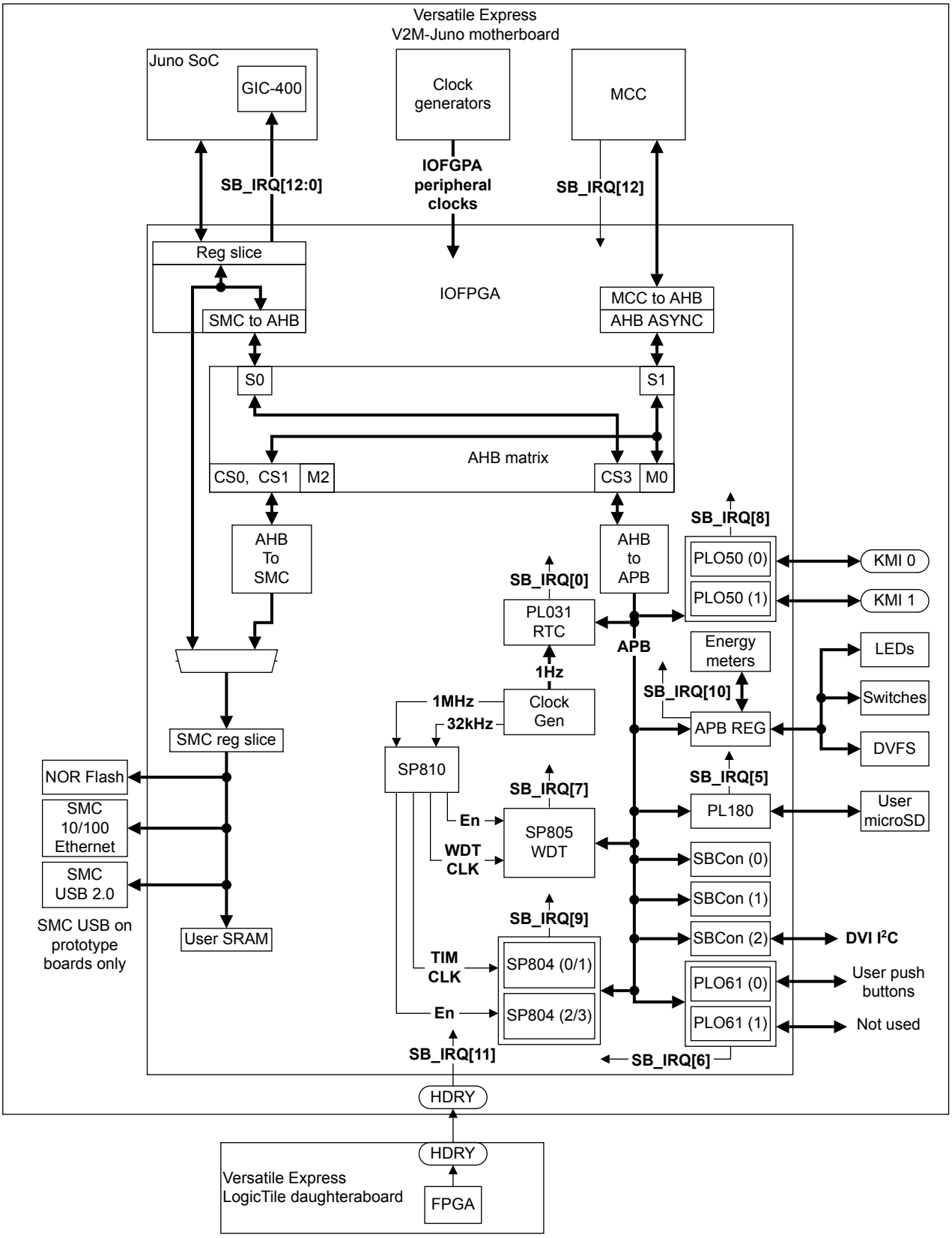

Figure B-2 Internal architecture of the IOFPGA, with SMC USB 2.0 ports, on the prototype V2M-Juno motherboard

B.2.4 SMC memory map of the prototype V2M-Juno motherboard

The following figure shows the SMC memory map of the prototype V2M-Juno motherboard that includes the CS5 chip selects.

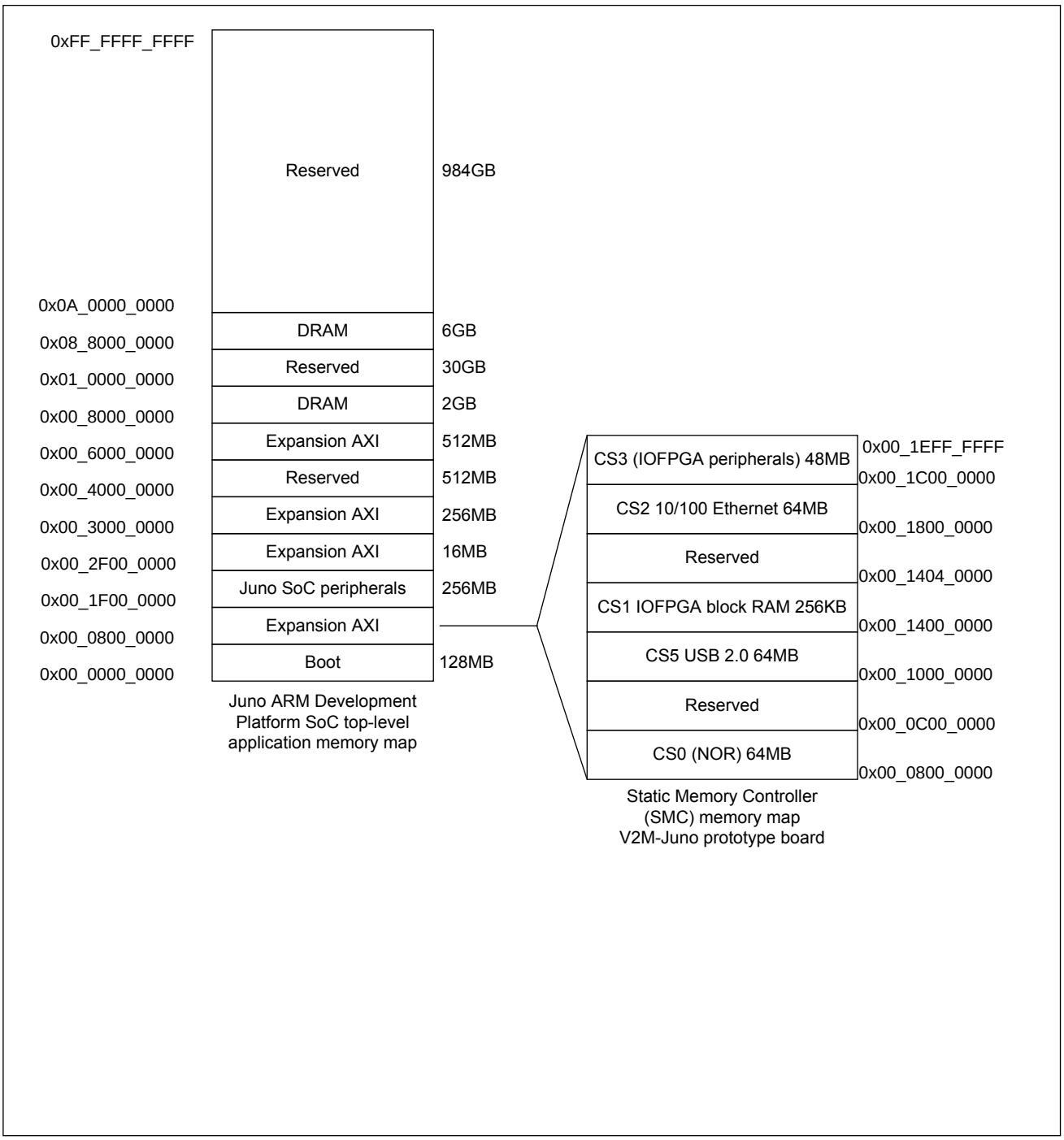

Figure B-3 SMC memory map of the prototype V2M-Juno motherboard

The following table shows the SMC memory map of the production V2M-Juno motherboard.

Table B-1 SMC interface memory map of production V2M-Juno motherboard

Address range	Size	Description
0x00_0800_0000 - 0x00_0BFF_FFFF	64MB	CS0-Motherboard NOR Flash.
0x00_0C00_0000 - 0x00_0FFF_FFFF	64MB	Reserved. Do not write to or read from these addresses.
0x00_1000_0000 - 0x00_13FF_FFFF	64MB	CS5-USB 2.0.
0x00_1400_0000 - 0x00_1403_FFFF	256KB	CS1-256KB internal IOFPGA block RAM.
0x00_1404_0000 - 0x00_17FF_FFFF	65535.75KB	Reserved. Do not write to or read from these addresses.
0x00_1800_0000 - 0x00_1BFF_FFFF	64MB	CS2-10/100 Ethernet.
0x00_1C00_0000 - 0x00_1EFF_FFFF	48MB	CS3-IOFPGA peripherals.

B.2.5 SMC USB 2.0 connectors

The prototype V2M-Juno motherboard provides two SMC USB 2.0 connectors.

The following figure shows the SMC USB 2.0 connectors, J51 and J52.

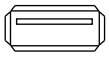

Figure B-4 SMC USB 2.0 connectors, J51 and J52

Appendix C.3
Specifications

This appendix contains the electrical specifications of the Versatile Express V2M-Juno motherboard

It contains the following sections:

C.3.1 Electrical specification

This section provides information on the current characteristics of the Versatile Express V2M-Juno motherboard.

Appendix D.4
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following sections:

D.4.1 Revisions

This following table describes the technical changes between released issues of this book.

Table D-1 Issue A

Change	Location	Affects
No changes, first release	-	-