Supercharging the Embedded Device: ARM® Cortex®-M7

Ian Johnson
Senior Product Manager, ARM
ARM® Cortex® Processors across the Embedded Market

**Cortex®-M processors**
- MCU + DSP
- Smallest footprint / lowest power

**Cortex®-R processors**
- RTOS
- Highest performance / real-time

**Cortex®-A processors**
- Rich OS
- Highest performance
ARM Cortex-M: Trusted Choice for Embedded Intelligence

8 Billion
Units shipped to date

240+
Licenses

3000+
Catalog Parts
Taking the Cortex-M Series to the Next Level

Scalable & Compatible Architecture

Cortex-M0
- Lowest Area

Cortex-M0+
- 90 µm

Cortex-M3
- 15 years

Cortex-M4
- Blended MCU and DSP

Cortex-M7
- Highest Performance

CoreMark per MHz

Highest Energy Efficiency

Energy-Performance Balance
Cortex-M7 Overview

- **Performance**
  - Achieving 5 CoreMark/MHz – 2000 CoreMark* in 40LP
  - Typical 2x DSP performance of Cortex-M4

- **Versatility**
  - Highly flexible system and memory interfaces
  - Designed for functional safety implementations

- **Scalability and compatibility**
  - Enables simple migration from any Cortex-M processor
  - Widest third-party tools, RTOS, middleware support

* CoreMark 1.0 : IAR Embedded Workbench v7.30.1 --endian=little --cpu=Cortex-M7 -e -Ohs --use_c++_inline --no_size_constraints / Code in TCM - Data in TCM
Cortex-M7 Key Features (1)

- **High performance core with DSP capabilities**
  - Six-stage dual-issue pipeline
  - Powerful DSP instructions and SP/DP Floating Point
  - Best-in-class core for high-end MCU, or replace MCU+DSP with Cortex-M7

- **Flexible, memory system**
  - Tightly-coupled memories for real-time determinism
  - 64-bit AXI AMBA4 memory interface with I-cache and D-cache for efficient access to external resources
  - Build MCU with access to large external memories and powerful peripherals

* SP – Single Precision, DP – Double Precision
Cortex-M7 Key Features (2)

- **ARMv7E-M architecture**
  - 100% binary forwards compatibility from Cortex-M4
  - Key Cortex-M family processor characteristics: Ease of use, excellent interrupt latency
  - **Fast interrupt response for real-time systems, reuse code and system design from existing products to reduce development costs**

- **Safety features**
  - Memory ECC (SEC-DED), MPU, MBIST, lock-step operation, full data trace, safety manual
  - **Enables entry into safety-critical markets.**
Cortex-M7 Target Applications

- Powerful processor for advanced audio/visual sensor hub processing
- Power-efficient local processor for IoT devices such as an edge router
- Flexible and reliable processor for industrial and motor control
Enabling Smarter Systems Without the Complexity

2x More performance delivering enhanced functionality

- More displays
- More motors
- Advanced touch sensing
- Multiple connectivity options
- Enhanced voice controls

ARM
Helping Drive Richer Audio Experiences

2x More performance delivering advanced sound processing

Cortex-M7 160 MHz
- Dolby Digital (with post processing)
- 7.1 Multi-channel audio support
- More speaker EQ processing
- Capacity for decoders
- More connectivity options

Cortex-M4 130 MHz
- Dolby Digital

Cortex-M7 in Automotive

**Trends and challenges:**
- Safety certification mandated in more regions
- Convergence of functionality into fewer MCUs/ASSPs
- Increasing user requirements and expectations

**Typical Applications**
- Dashboard in medium-range cars
- Voice recognition (for Multimedia control functions)
- Character recognition (eg Kanji)
- “Convenience” features
- Chassis, electric power steering, “steer-by-wire”
- Automotive audio

**Cortex-M7 Advantages:**
- High performance core with fast DSP
- Safety features built in and safety manual
- Determinism with high performance
- Full trace via ETM
Cortex-M7 in Industrial Control

- **Trends and challenges**
  - High performance control functions
  - Safety, reliability and conformance will become mandatory
  - 80-90% of cost is software, Cortex-M offers scalability and protects software investment

- **Typical applications:**
  - Factory Automation
    - Inverters, Servos
    - Programmable Logic Controllers
    - High-speed comms
  - Intelligent motor control

**Cortex-M7 Advantages:**
- Increased DSP performance for control functions
- Safety features built-in
- In-order pipeline gives performance with predictability
- TCMs and low interrupt latency: Interrupt response within 100ns required
- Scalability from Cortex-M3 through Cortex-M7 up to Cortex-A53
Cortex-M7 in Sensor Fusion

**Trends and challenges**
- Increased sophistication of fusion algorithm
- Increase in number and variety of sensors
- Image sensors / processing

**Typical applications:**
- Sensor fusion hubs
- Sensor control and sensor signal fusion

**Cortex-M7 Advantages:**
- Increased DSP performance for fusion and control operations
- Software support by the top three fusion algorithm developers
Cortex-M7 CPU Performance
Cortex-M7 Breaks the Embedded Barriers

Performance

~4000 CoreMark
Cortex-M7 MCU in 28nm

~2000 CoreMark
Cortex-M7 MCU in 40nm

~1000 CoreMark
Cortex-M7 MCU in 90nm

~600 CoreMark

Historical moderate increase limited by process shrink

Unparalleled range of applications

MByte

GByte

Memory

ARM
ARM Cortex-M7: Built for Performance

- Fast compute for demanding embedded applications
  - Six-stage superscalar pipeline with branch prediction
  - Single and double precision floating point unit

- Flexible memory system
  - 64-bit AXI AMBA4 interconnect
  - I-cache and D-cache for efficient memory operation

- Ultra-fast responsiveness for control
  - 12 cycles interrupt latency
  - Tightly coupled memories for real-time determinism

Source: CoreMark.org, ARM for Cortex-M7
EEMBC IPC Comparison

- Results are geo-mean of EEMBC IPC relative to baseline (quantified as ‘1’)
- Measured on comparable memory systems (in this case, WB caches on Cortex-M7)

![Bar chart showing IPC comparison across different sectors]
FP Benchmarking Status

- Cortex-M7 floating point performance relative to Cortex-R5 and Cortex-M4 processors

Assumes all processors running at the same clock frequency
Based on EEMBC FPMark benchmarks using "small" data-sets
Performance relative to Cortex-R5 in the same system
Benchmarks compiled with ARM tool-chain (v5.04)
Cortex-M7: Competitive with Popular DSPs

- **Essential DSP features**
  - Parallel execution of loads, stores and MAC
  - SIMD support, single-cycle MAC
  - Single and double precision floating point unit
  - Minimal loop overhead (branch predictor/BTAC)
  - Consistently good performance across key DSP functions

- **Optimized DSP libraries**

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### Normalized cycles, lower = better

<table>
<thead>
<tr>
<th>DSP Function</th>
<th>Cortex-M7 32-bit</th>
<th>Cortex-M7 32-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Biquad Cascade</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>FIR Filter</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Real FFT</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Complex FFT</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

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**ARM® Cortex®-M7**

- Nested Vectored Interrupt Controller
- WIC
- FPU
- CPU
- ARMv7-M
- I Cache
- D Cache
- Data TCM
- Instr TCM
- AXI-M
- AHB-P
- AHB-S

**Debug**

**ETM**

**ECC**

**MPU**

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**ARM**
Cortex-M7 – Replacement for MCU+DSP

**Trends:**
- Convergence of MCU+DSP to DSC for cost reduction
- Increased processing demands
- Increasing consumer expectation of quality in portable devices

**Example applications:**
- Multi-channel audio / Dolby Audio
- Advanced Motor Control
- Factory Automation
- Automotive
- Image processing
- Power conversions

**Cortex-M7 Advantages:**
- High performance core with fast DSP
- Compatibility with existing Cortex-M4 designs
- Flexible memory system
Cortex-M7 DSP Performance

Paul Beckmann
## The Evolution of the Cortex-M Series

<table>
<thead>
<tr>
<th>Feature</th>
<th>Cortex-M3</th>
<th>Cortex-M4</th>
<th>Cortex-M7</th>
<th>Traditional DSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single cycle MAC</td>
<td></td>
<td>Fixed-point only</td>
<td>Fixed and floating-point</td>
<td>Y</td>
</tr>
<tr>
<td>Floating-point</td>
<td></td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Fractional and saturating math</td>
<td></td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>SIMD operations</td>
<td></td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Load and store in parallel with math</td>
<td></td>
<td></td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Zero overhead loops</td>
<td></td>
<td></td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Accumulator with guard bits</td>
<td></td>
<td></td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Circular and bit-reversed addressing</td>
<td></td>
<td></td>
<td></td>
<td>Y</td>
</tr>
</tbody>
</table>
Load / Store Improvement

**Cortex-M4**
- Single load or store instructions take 2 cycles
- N consecutive loads or stores take N+1 cycles
- Approach – group as many loads and stores together

**Cortex-M7**
- Load and store operations can occur in parallel with math
- Memory access possible without penalty
- Approach – interleave memory accesses with computation

### Cortex-M4

\[
\begin{align*}
X_{n1} &= pIn[0]; \\
X_{n2} &= pIn[1] ; \\
X_{n3} &= pIn[2]; \\
X_{n4} &= pIn[3] ; \\
X_{n5} &= pIn[4]; \\
X_{n6} &= pIn[5] ; \\
X_{n7} &= pIn[6] ;
\end{align*}
\]

\[
\begin{align*}
acc1 &= b0 * X_{n1} + d1; \\
d1 &= b1 * X_{n1} + d2; \\
d2 &= b2 * X_{n1}; \\
d1 &= a1 * acc1; \\
d2 &= a2 * acc1;
\end{align*}
\]

### Cortex-M7

\[
\begin{align*}
X_{n1} &= pIn[0]; \\
X_{n2} &= pIn[1] ; \\
X_{n3} &= pIn[2]; \\
X_{n4} &= pIn[3] ; \\
X_{n5} &= pIn[4]; \\
X_{n6} &= pIn[5] ; \\
X_{n7} &= pIn[6] ;
\end{align*}
\]

\[
\begin{align*}
acc1 &= b0 * X_{n1} + d1; \\
d1 &= b1 * X_{n1} + d2; \\
d2 &= b2 * X_{n1}; \\
d1 &= a1 * acc1; \\
d2 &= a2 * acc1;
\end{align*}
\]
Floating-Point MAC Improvement

Cortex-M4
- Multiplication or addition takes 1 or 2 cycles depending upon whether the result is used in the next instruction
- MAC requires 2 to 4 instructions
- Approach – use individual multiplies or adds and reorder to avoid stalls

Cortex-M7
- Multiplication or addition takes 1 or 2 cycles depending upon whether the result is used in the next instruction
- MAC requires 1 cycle
- Approach – use MACs whenever possible

Cortex-M4
\[
\begin{align*}
Xn1 & = pln[0]; \\
Xn2 & = pln[1]; \\
Xn3 & = pln[2]; \\
Xn4 & = pln[3]; \\
Xn5 & = pln[4]; \\
Xn6 & = pln[5]; \\
Xn7 & = pln[6]; \\
\end{align*}
\]
\[
\begin{align*}
acc1 & = b0 \times Xn1; \\
tmp1 & = b1 \times Xn1; \\
acc1 & += d1; \\
d1 & += d2; \\
d2 & = b2 \times Xn1; \\
tmp1 & = d1 \times acc1; \\
tmp2 & = a2 \times acc1; \\
d1 & += tmp1 \\
d2 & += tmp2;
\end{align*}
\]

Cortex-M7
\[
\begin{align*}
Xn1 & = pln[0]; \\
Xn2 & = pln[1]; \\
Xn3 & = pln[2]; \\
acc1 & = b0 \times Xn1 + d1; \\
Xn4 & = pln[3]; \\
d1 & = b1 \times Xn1 + d2; \\
Xn5 & = pln[4]; \\
d2 & = b2 \times Xn1; \\
Xn6 & = pln[5]; \\
d1 & += a1 \times acc1; \\
Xn7 & = pln[6]; \\
d2 & += a2 \times acc1;
\end{align*}
\]
2x Performance Improvement over the Cortex-M4

- Measurements using the CMSIS DSP Library
- Available free of charge from ARM
- Now optimized for the Cortex-M7

Note: combines architectural improvements with expected core clock increase.
The code was compiled using the ARM C Compiler (armcc) 5.04
Comparison was made on an FPGA on a Versatile Express motherboard
Implications for Product Developers

- Connected products require an MCU
  - USB
  - Wi-Fi / Ethernet
  - Etc.
- Signal processing needs for multimedia products are growing
  - Audio, video, microphones, etc.
- IoT products packed with sensors

Cortex-M7 Advantage:
- Reduced BOM cost
- Compatibility with existing Cortex-M4 designs
- Ease of development
Implications for Audio Products

Cortex-M4

Cortex-M7

2 x performance
5.1 Channel Automotive System

- Volume and tone controls
- Fader / balance
- Stereo upmix to 5.1 channels
- Perceptual volume leveler
- Speaker EQs – over 60 Biquads
- Delays, gains, mutes per channel
- Limiter
- 48 kHz operation

216 MHz on Cortex-M4
144 MHz on Cortex-M7

- Designed using Audio Weaver from DSP Concepts
Cortex-M7 CPU Advanced Features
Cortex-M7: Extending the Cortex-M Advantage

- Retaining the benefits of Cortex-M DNA
  - Easy to use Cortex-M programming model
  - Leading-edge interrupt latency
  - Flexible low-power modes

- Expanding Cortex-M capabilities
  - AXI, TCM and caches
  - Dual precision FPU
  - Full data trace

- Enhanced support for safety critical markets
  - Lock-step operation
  - Memory interfaces with ECC
  - Safety documentation
Cortex-M7 has the same powerful instruction set as Cortex-M4:

- MAC instructions are all single-cycle
- SIMD instructions can work on 8-/16-bit quantities packed in to a 32-bit word
- Arithmetic can be signed/unsigned, saturating/non-saturating
Designed for High Energy Efficiency

- **Low power processor design**
  - Extensive clock and power gating
  - 3 separate power domains (interrupts, processor, cache RAM)
  - Enables MCU vendors to customise their design and minimise power consumption

- **Power-saving sleep modes:**
  - Sleep and Deep Sleep modes, with WFI/WFE instructions to put processor to sleep, or sleep on exit from ISR
  - Signals exported to MCU to allow peripherals to be powered down on sleep
  - Enables MCU vendors to create energy efficient chipsets
Cortex-M7 Safety Features

- Cortex-M7 specific
  - Cache ECC
  - Dual core lock-step with delay
  - External TCM ECC interface
  - On-line MBIST interface
- ARMv7-M architecture based
  - Memory protection unit (MPU)
  - Exception logic

- These features will be included in the Cortex-M7 Safety Documentation Package:
  - Safety Manual
  - FMEA Report
  - Development Interface Report
Cortex-M7 Overview

- Nested Vectored Interrupt Controller (NVIC) 1 to 240 interrupts + NMI
- Floating Point Unit (optional) Single and double precision
- 32-bit AHB slave Debug access to complete memory map
- ETM (optional) Full instruction and data trace (ETMv4)
- 32-bit APB master CoreSight Debug Peripherals
- Memory Protection Unit (optional) 8 or 16 regions
- Data cache (optional) Up to 64kB, WT/WB cache
- Instruction cache (optional) Up to 64kB, WT/WB cache

**Processor Core**
- I TCM
- D TCM
- TCM arbiter and interface
- MPU
- FPU
- D Cache
- Ctrl

**External Memory System**
- AXI Master
- AHB Slave
- NVIC
- Debug I/F
- Trace I/F
- EPPB I/F

**Interrupts**
- 64-bit Instruction TCM (optional) SRAM/ Accelerated Flash
- 2x32-bit Data TCM Fast on-chip SRAM
- 32-bit AHB slave interface DMA Engine access to TCM
- 64-bit AMBA4 AXI master interface Slow Flash / off-chip instruction memory / off-chip memory i.e. DDR / Slow peripherals

**Additional Features**
- Slow Flash / off-chip instruction memory / off-chip memory i.e. DDR / Slow peripherals
## Cortex-M7 Pipeline

- **6 stage, in order, superscalar pipeline**
- **Integer pipe:**
  - Dual shifters, dual ALUs, one MAC-capable
- **Float pipe:**
  - FP instrs can be dual issued with integer instrs
- **Branch Target Address Cache + branch predictor boosts performance**

### Diagram

- **Load/Store Pipeline**
  - Load Store #1
  - Load Store #2
  - Load Store #3
- **Main / ALU #1 Pipeline**
  - Fetch
  - Decode (1st dec)
  - Issue (2nd dec)
  - Execute #1
  - Execute #2
  - Write / Store
  - Retire / ETM trace
- **ALU #2 Pipeline**
  - Execute #2
  - Write / Store
- **Multiply Accumulate Pipeline**
  - MAC #1
  - MAC #2
- **Float Point Pipeline (optional)**
  - F1
  - F2
  - F3
  - F4
Tightly Coupled Memory (TCM)

- All TCMs:
  - Support wait-states
  - Can be used at boot-up time
  - Support up to 16MB of memory
- Provide deterministic performance
  - Dedicated store buffering
- Instruction TCM (ITCM)
  - 64-bit interface
- Data TCM (DTCM)
  - 2 X 32-bit interface: D0TCM and D1TCM, SSRAM protocol to enable direct integration with memories
  - Supports dual-issue of loads when bit[2] of address is different
AHB Peripheral port (AHBP)

- 32-bit AHB-Lite interface
  - Enables re-use of peripherals from existing Cortex-M systems
- Designed specifically for peripherals rather than memory
- Designed to simultaneously:
  - Minimise both read and write access latency to peripherals
  - Support 1 write/cycle to zero wait-state slaves
- Tightly coupled into processor pipeline
- Expect to be connected to low-latency peripherals
DMA interface (AHBS)

- 32-bit AHB-Lite slave interface
- Provides system access to ITCM and DTCM
- 2 arbitration schemes to TCM are supported:
  - Round robin – for ‘fair’ sharing of TCM bandwidth
  - SW has priority – for real-time critical code.
- Separate clock: DMA interface available whilst processor is sleeping
- Support for holding the processor idle out of reset to enable DMA into TCM for boot code.
  - Supports boot from volatile TCM memory
Caches - Overview

- Harvard arrangement for optimum performance
- I-cache 2-way associative, D-cache 4-way associative, pseudo-random replacement policy
- I and D both optional, configurable sizes (4kB – 64kB each)
- Extensions defined for the ARMv7-M system architecture
  - Addition of cache maintenance operations
- Full support for the following attributes
  - Write Through, no write allocate (WT)
  - Write-back, no write allocate (WBRA)
  - Write-back, write allocate (WBWA)
Simple Microcontrollers

- The minimal design (system level, debug system not shown)
Simple Microcontroller with Flash Access Accelerator

- The minimal design (system level, debug system not shown)
High Performance Microcontrollers

- **SRAM (32-bit)**
- **SRAM (32-bit)**
- **SRAM (64-bit)**

**AHB Bus Matrix**
- **AHB Slave Mux**
- **AHB to APB**
- **APB slave multiplexer**

**D0-TCM**
- **D1-TCM**
- **I-TCM**

**Cortex-M7**

**I cache**

**DMA Controller (AHB)**

**AHB Slave Port**

**Flash**

**Slower peripherals**

**AXI interconnect (e.g. NIC-400)**

**APB port for configuration**
Cortex-M7: Unlock and Unleash Software Productivity

- Focus on application development
  - Exploit optimally tuned range of processors
  - Utilize richer variety of peripherals
  - Harness advanced proven runtime environments

- Spend less time on code optimization
  - More capable hardware resources
  - Optimized and proven libraries

- Develop and deploy software faster
Cortex-M7: Extended Support for Turn Key Enablement

Added support for Cortex-M7 available today

Keil MDK Version 5.12

ARM C/C++ Compiler
µVision Debugger with Trace

CMSIS v4.2 Pack
Extended

CMSIS-DSP library for floating point unit
Keil CMSIS-RTOS RTX support

Versatile Express MPS2 Fast Models
ARM Artisan libraries

Cortex-M Prototyping System
FPGA image with matching Device Family Pack

SoC system design enablement
With support for the new Cortex-M7 processor, we are further strengthening our leading market position by delivering development tools for ARM with an outstanding benchmark score of 5.04 CoreMark/MHz

- Stefan Skarin, IAR Systems

Our robust embedded software components are designed to be used in high performance applications targeted by Cortex-M7, including industrial control, safety and IoT

- Jean Labrosse, Micrium

ARM Cortex-M7 will bring substantially more computing power to embedded applications, and SEGGER will continue to innovate new products and features for each new generation of ARM processors

- Rolf Segger, SEGGER
“The Cortex-M7 is well positioned between Atmel’s Cortex-M based MCUs and Cortex-A based MPUs enabling Atmel to offer an even greater range of processing solutions. Customers using the Cortex-M based MCU will be able to scale up performance and system functionality, while keeping the Cortex-M class ease-of-use and maximizing software reuse. We see the ARM Cortex-M7 addressing high-growth markets like IoT and wearables, as well as automotive and industrial applications that can leverage its performance and power efficiency” – Reza Kazerounian, Atmel

“Freescale Cortex-M7-based solutions dramatically extend MCU performance, opening new opportunities for our business. Our solutions will enable significant innovation and system-level efficiency in areas such as motor control, industrial automation and power conversion. These are rapidly growing markets where the high performance of the Cortex-M7 core eliminates the need for additional DSPs and microcontrollers” - Geoff Lees, Freescale

“Offering customers more intelligence and processing power on our STM32 microcontrollers is a major objective for ST, and the Cortex-M7 delivers that impressively. The Cortex-M7 core supports upwardly-scalable compatibility with our existing wide range of 500 Cortex-M STM32 microcontrollers, associated tools and software ecosystem, allowing developers to rapidly adopt our next-generation STM32 Cortex-M7-based MCUs” - Daniel Colonna, STMicroelectronics
Supercharge Cortex-M based solutions
Develop versatile, scalable solutions
Address safety critical applications
Harness the broadest ecosystem
A panel discussion will follow with Cortex-M7’s lead partners....