ICCAD 2017 Tutorial

Standard Cell Design and Optimization Methodology for ASAP7 PDK

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Outline

ASAP7 PDK

Standard Cell Library Design and Optimization

Design Synthesis and Exploration

How to Download and Use

Summary

ASAP7 PDK

Predictive 7nm Process Design Kit – Arm and ASU: http://asap.asu.edu/asap/

- FinFET with discrete transistor sizing

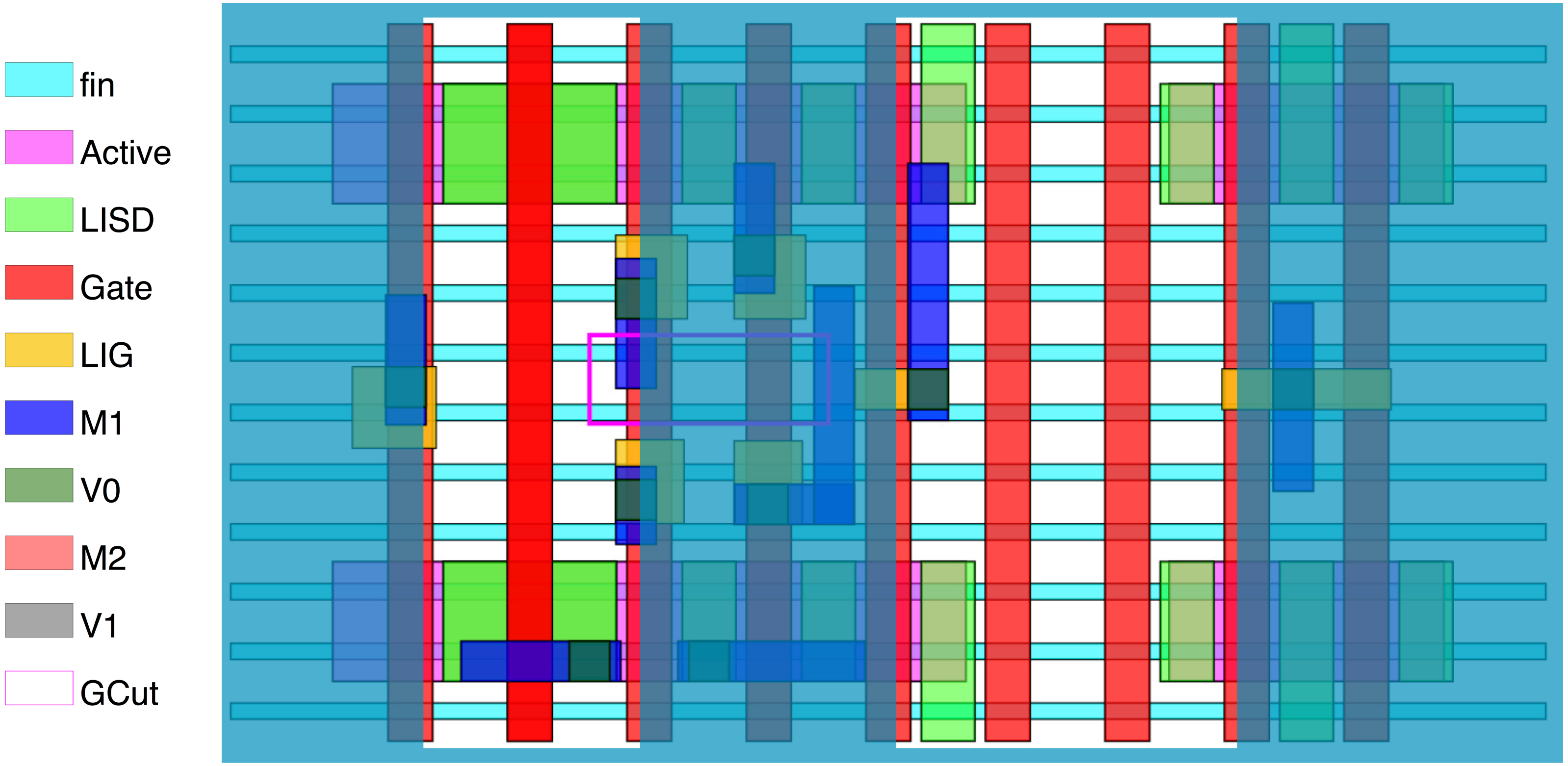
Transistor geometries

- 20/54nm gate length/pitch, 27nm fin pitch.

Key design rules

- 18/36nm metal-1 width/pitch (two-dimensional layout with EUV)
- Metal minimum tip-to-tip 31nm, metal minimum tip-to-side: 25nm
- Minimum horizontal distance between diff-net active areas: 92nm

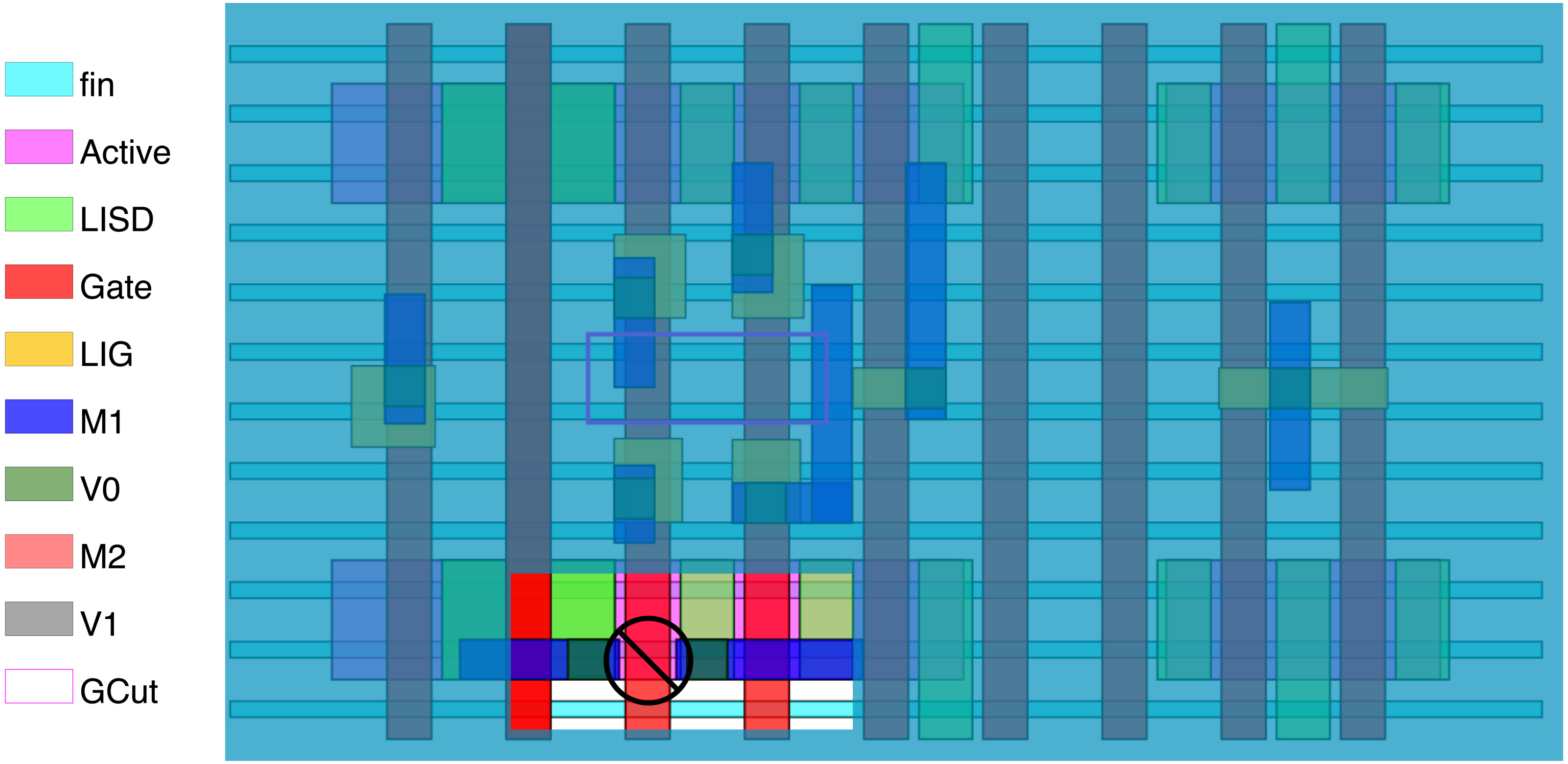
Key Implications on Layout Design



Key design-rule constraints:

- Diffusion break
- Horizontal metal routing
- Vertical metal routing
- Gate contact
- Gate cut usage

Key Implications on Layout Design



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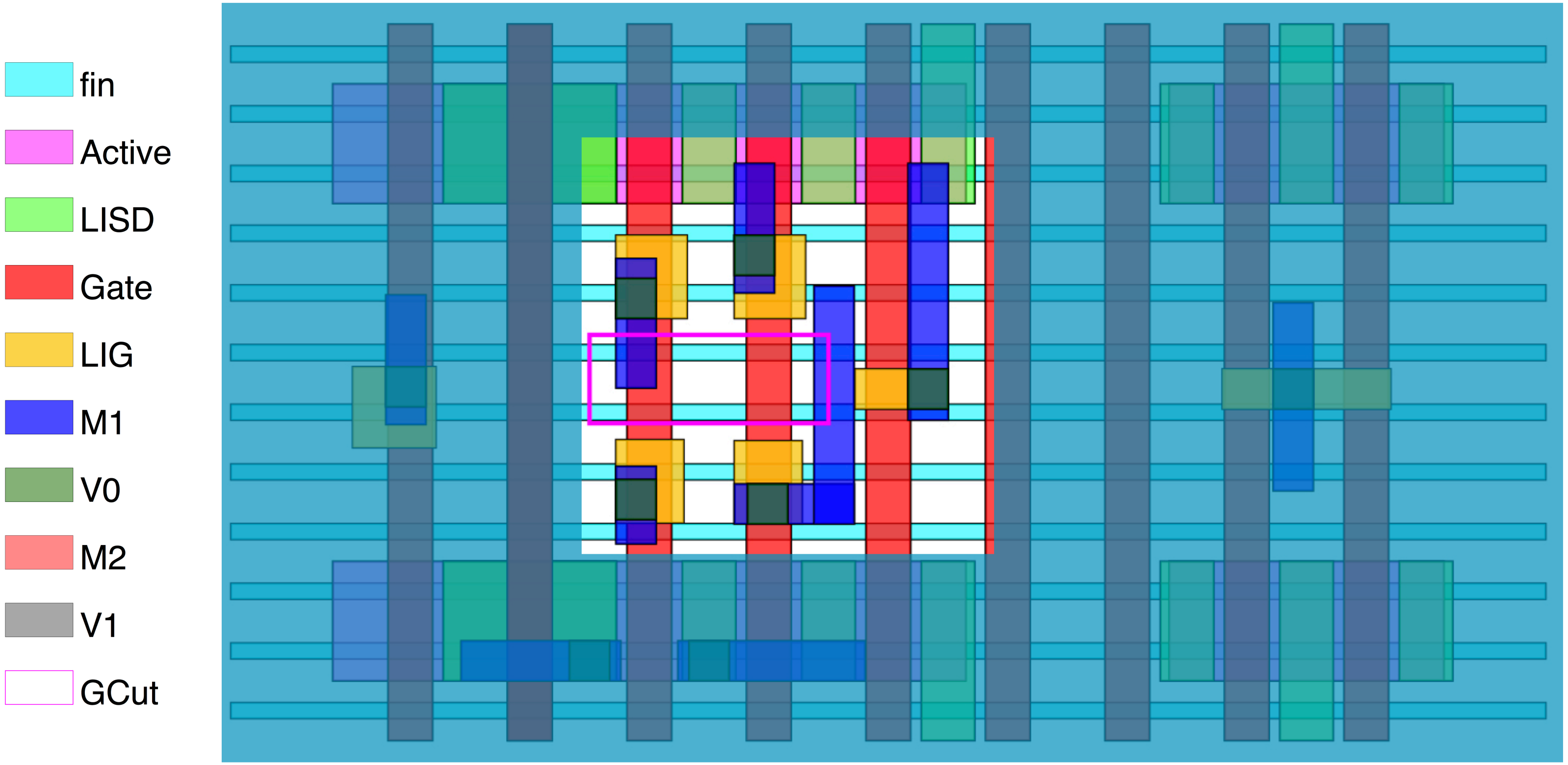

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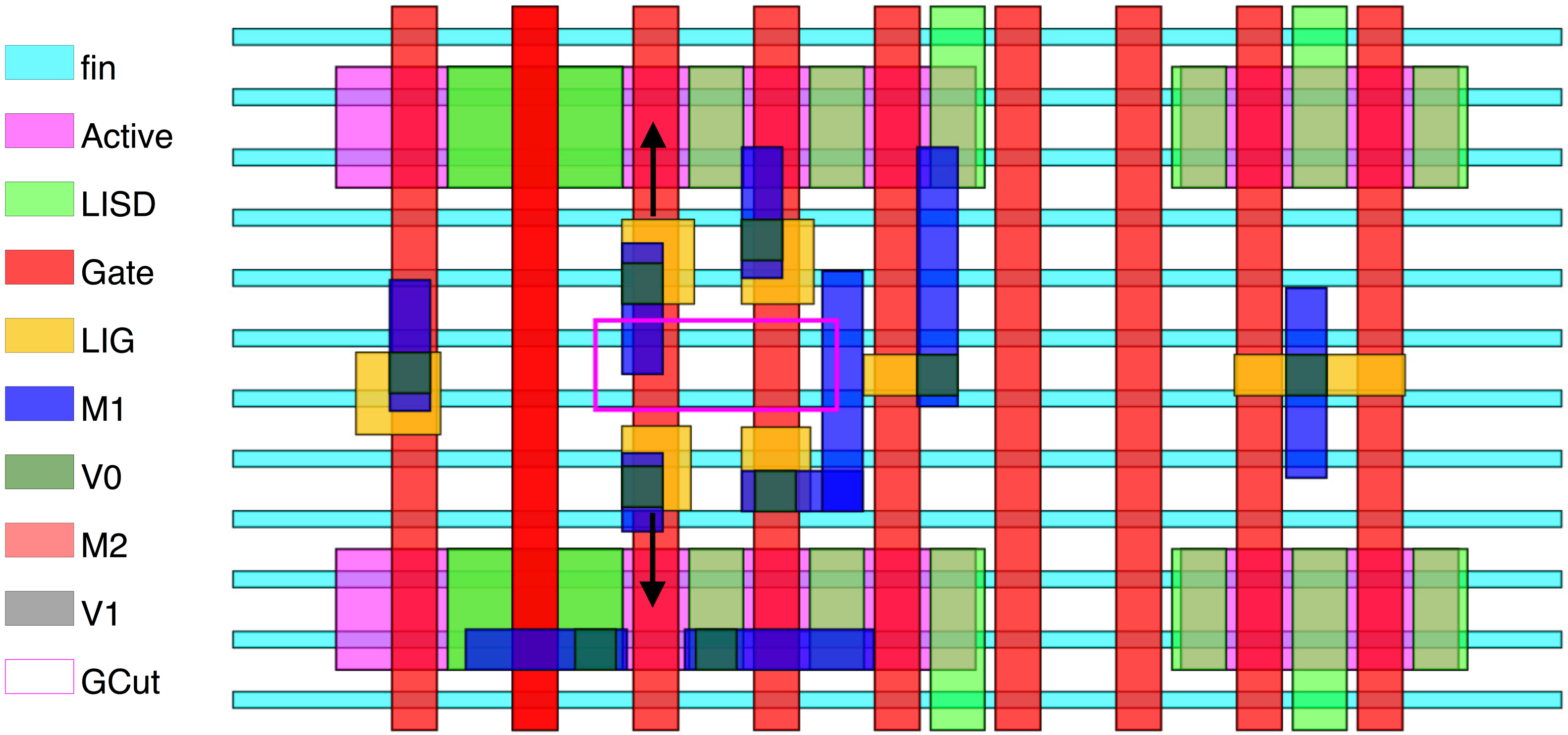

Key design-rule constraints:

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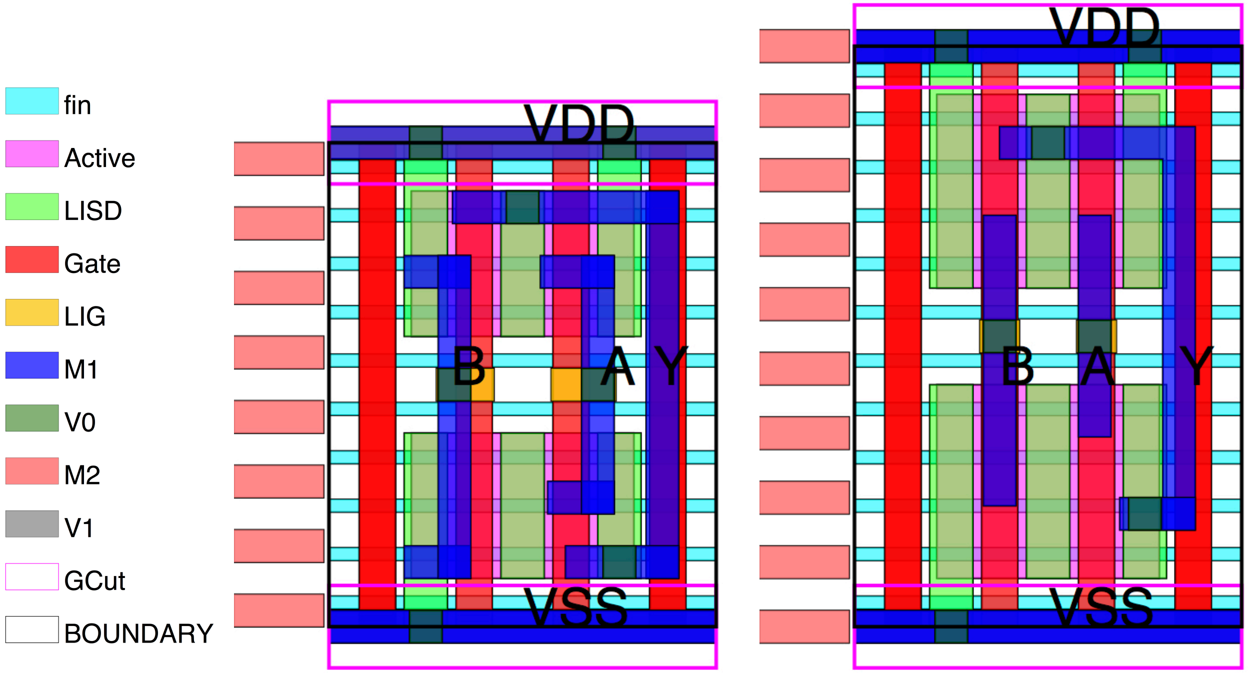
Standard Cell Library Design and Optimization

Standard Cell Architecture

9-Track and 7.5-Track

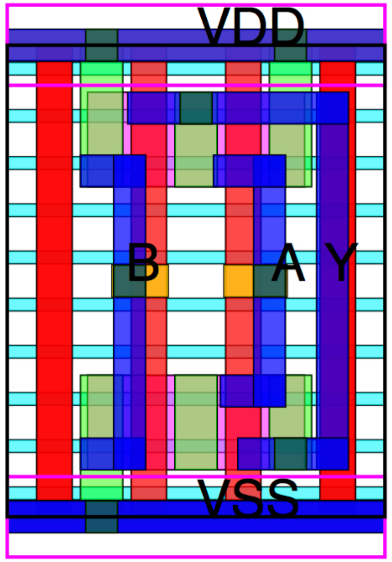


SC architecture	9-track	7.5-track
Total # of fins	12	10
# of fins per transistor	4	3
# of metal-1 tracks for signal routing	8	5.5
# of metal-2 track for signal routing	8	6
metal-2 and metal-1 track offset (nm)	0	9

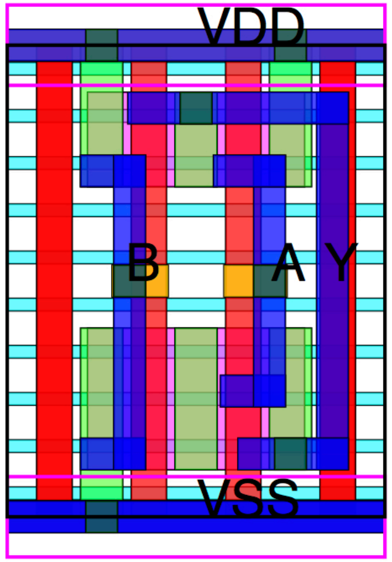
Exhaustive Transistor Sizing

NAND2_X1N under 7.5-track architecture

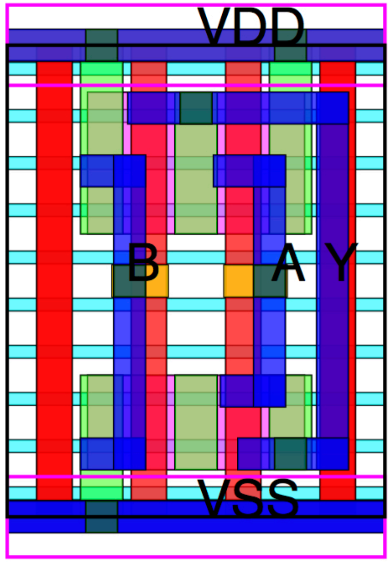
- Exhaustive timing simulations to choose the balanced rising and falling slew/delay
- NAND2_X1R and NAND2_X1F, rising/falling dominated cells



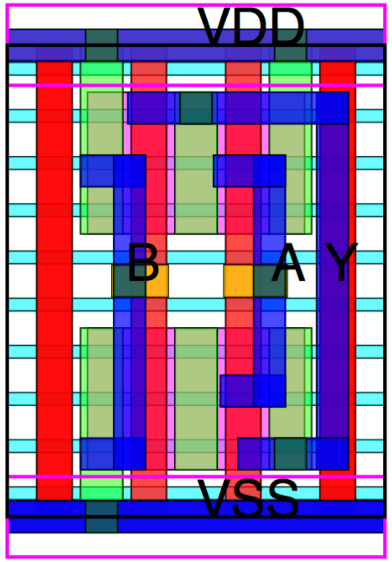
(2p, 2n)



(2p, 3n)

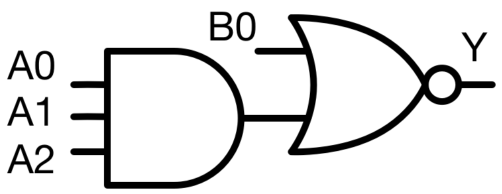


(3p, 2n)

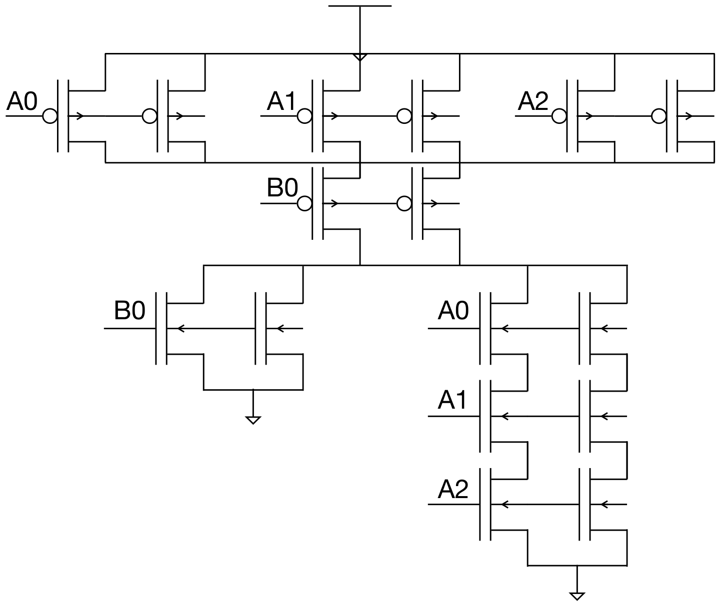


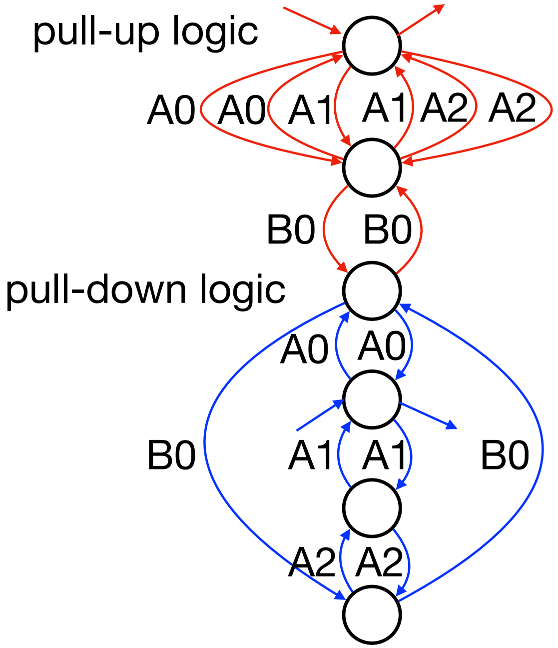
(3p, 3n)

Transistor Placement

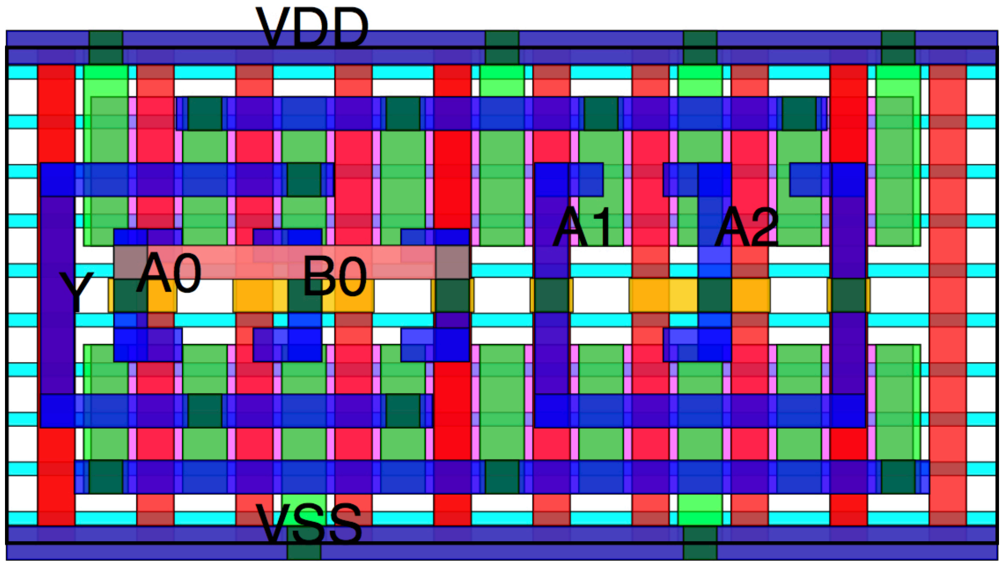


AOI31_X2N: consistent Euler path for pull-up and pull-down logic



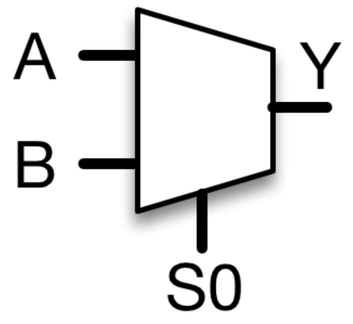


(A0, B0, B0, A0, A1, A2, A2, A1)



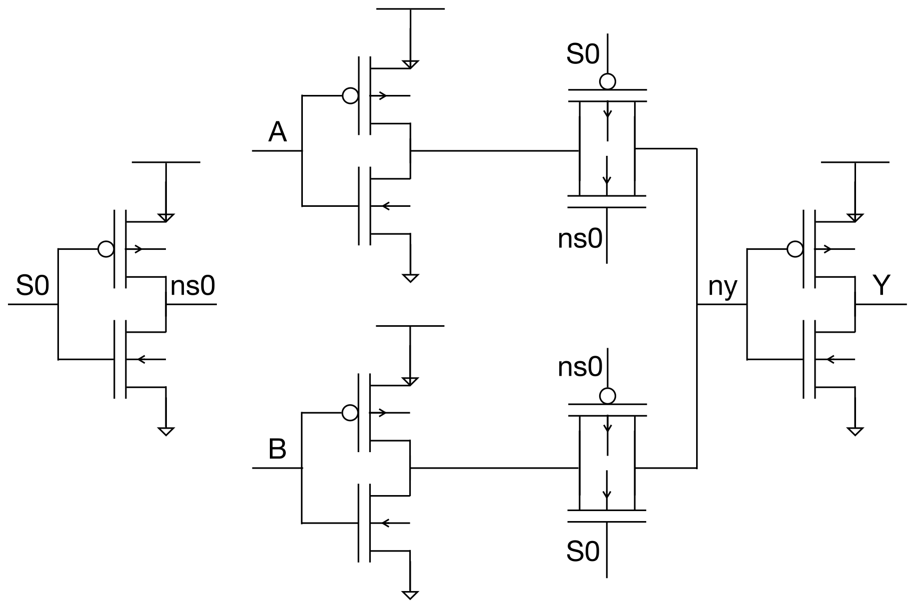
[Uehara+, DAC'1979] [Maziasz+, DAC'1987]

Generalized Euler Path

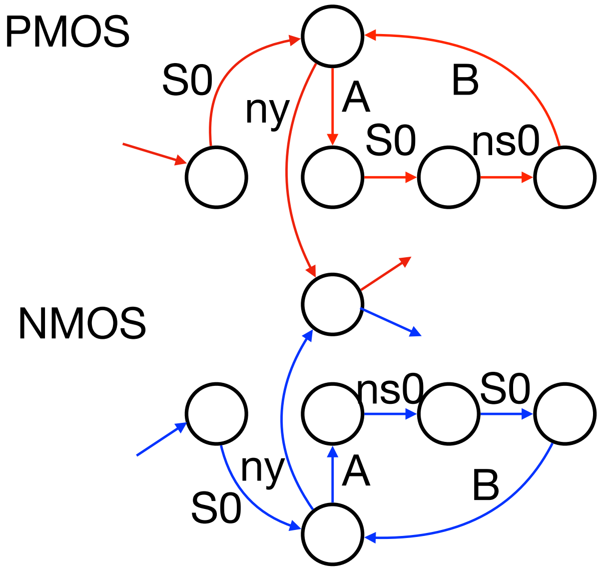


MXT2_X1N: pass-gate-based multiplexer

- Multigraphs for PMOS/NMOS are no longer dual

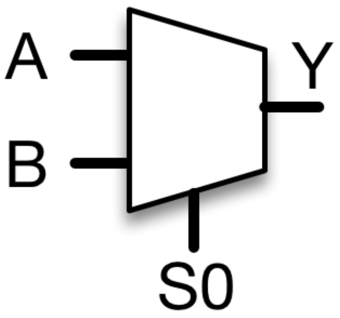


(S0, A, S0, ns0, B, ny)



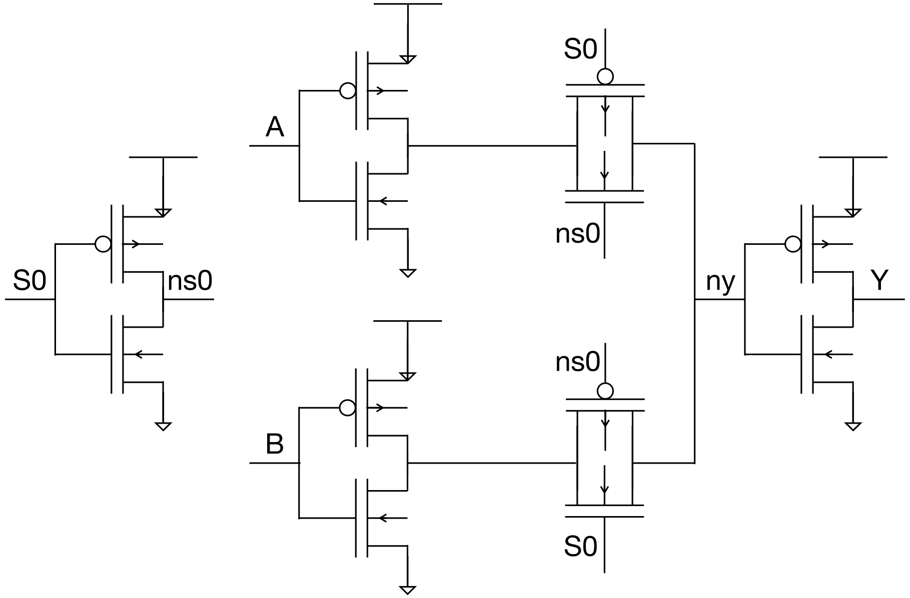
(S0, A, ns0 ,S0, B, ny)

Generalized Euler Path

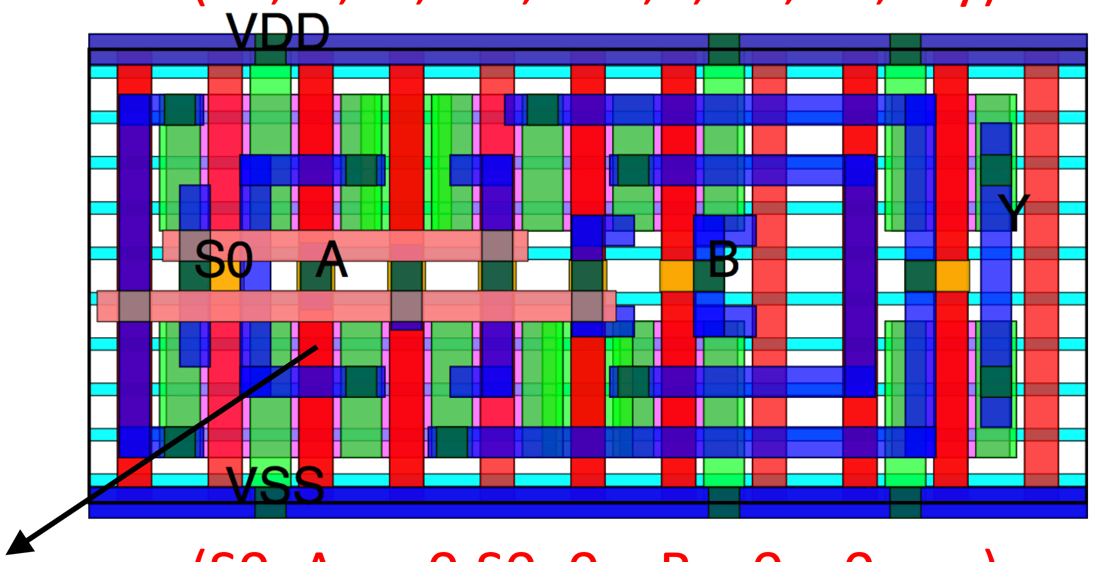


MXT2_X1N: pass-gate-based multiplexer

- Area-compact placement leads to routability issues: pin A is blocked



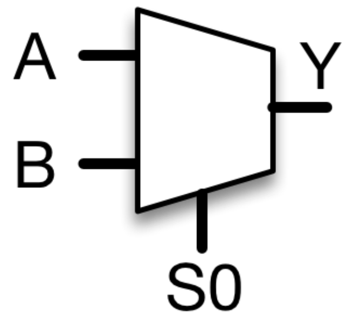
(S0, A, 0, S0, ns0,B,   0,   0, ny)



Pin A

(S0, A, ns0,S0, 0,   B,   0,   0, ny)

Generalized Euler Path



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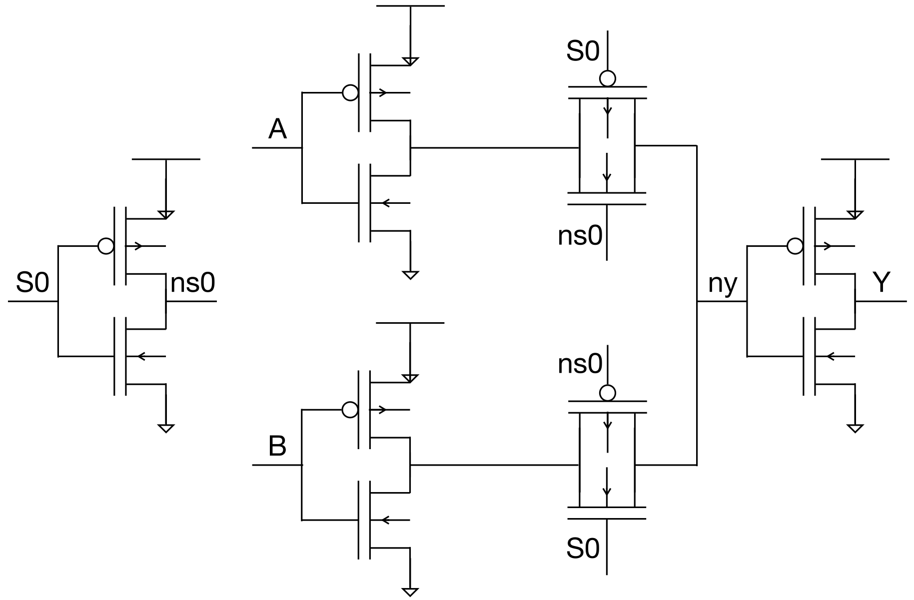
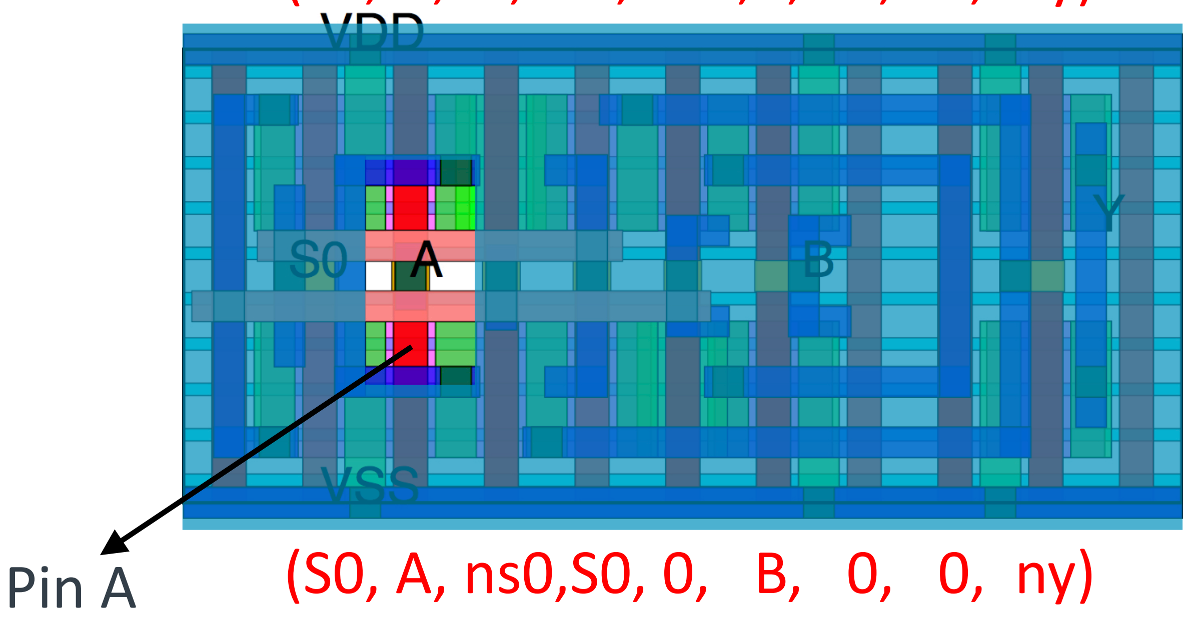
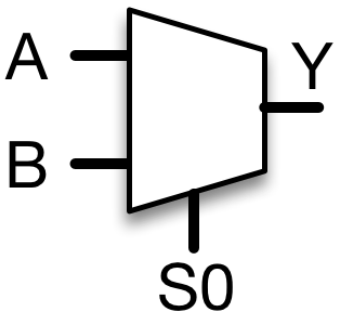


(S0, A, 0, S0, ns0,B, 0, 0, ny)



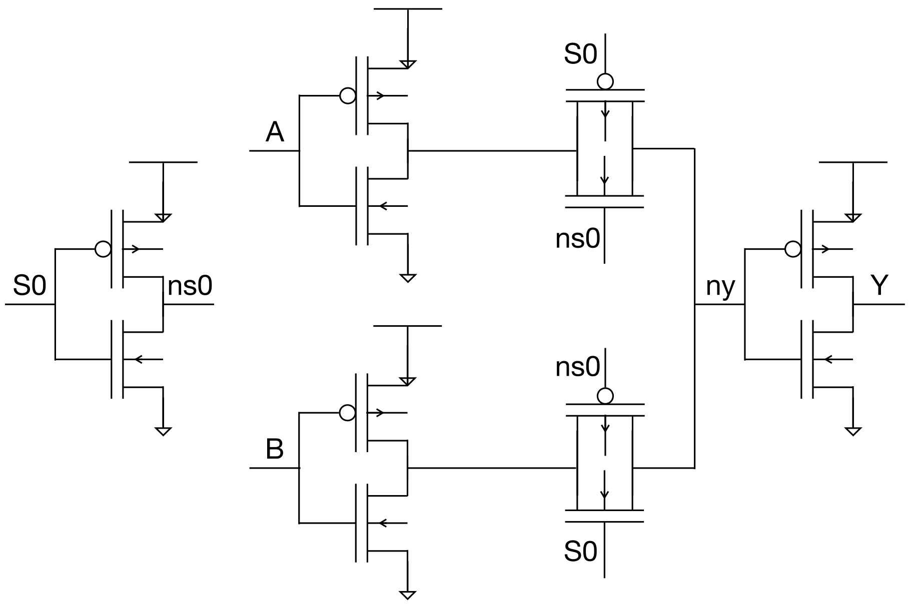
(S0, A, ns0,S0, 0, B, 0, 0, ny)

Generalized Euler Path

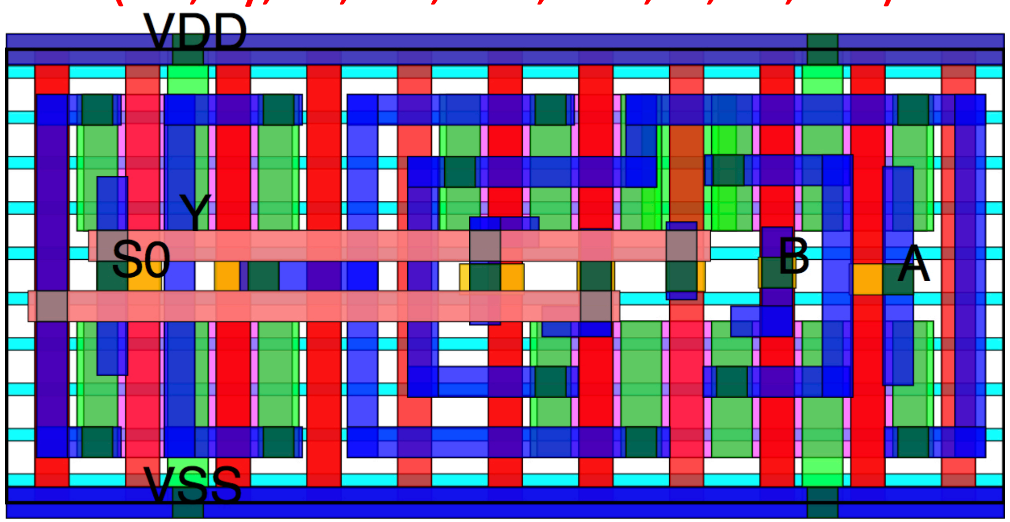


MXT2_X1N: pass-gate-based multiplexer

- A different area-compact placement solution: pin A is accessible



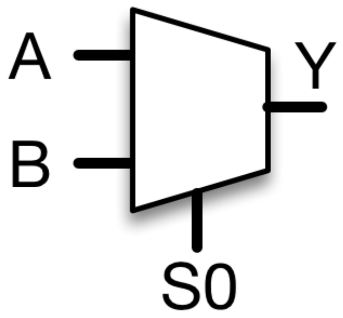
(S0,ny, 0, 0, S0,ns0, 0, B, A)



(S0,ny, 0, 0, 0, ns0,S0, B, A)

A different path

Generalized Euler Path



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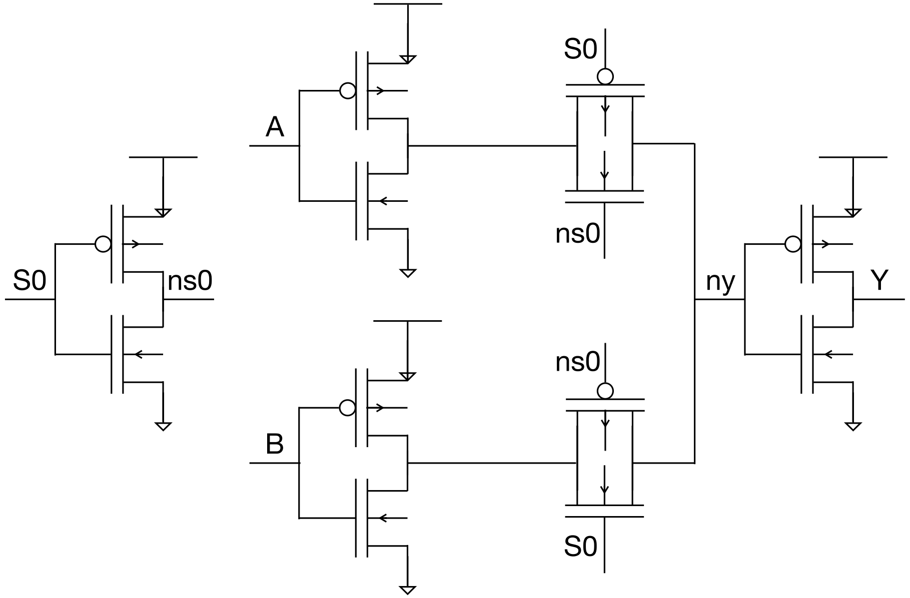
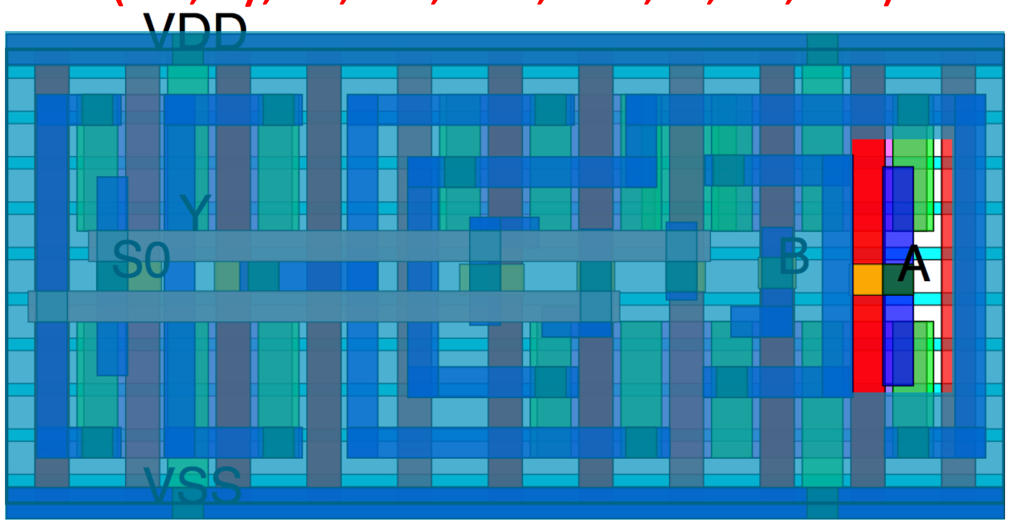


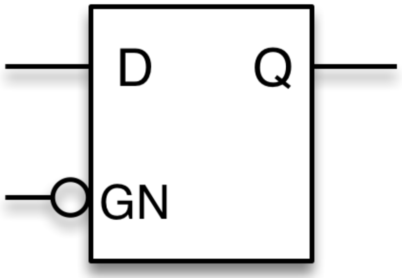
(S0,ny, 0, 0, S0,ns0, 0, B, A)



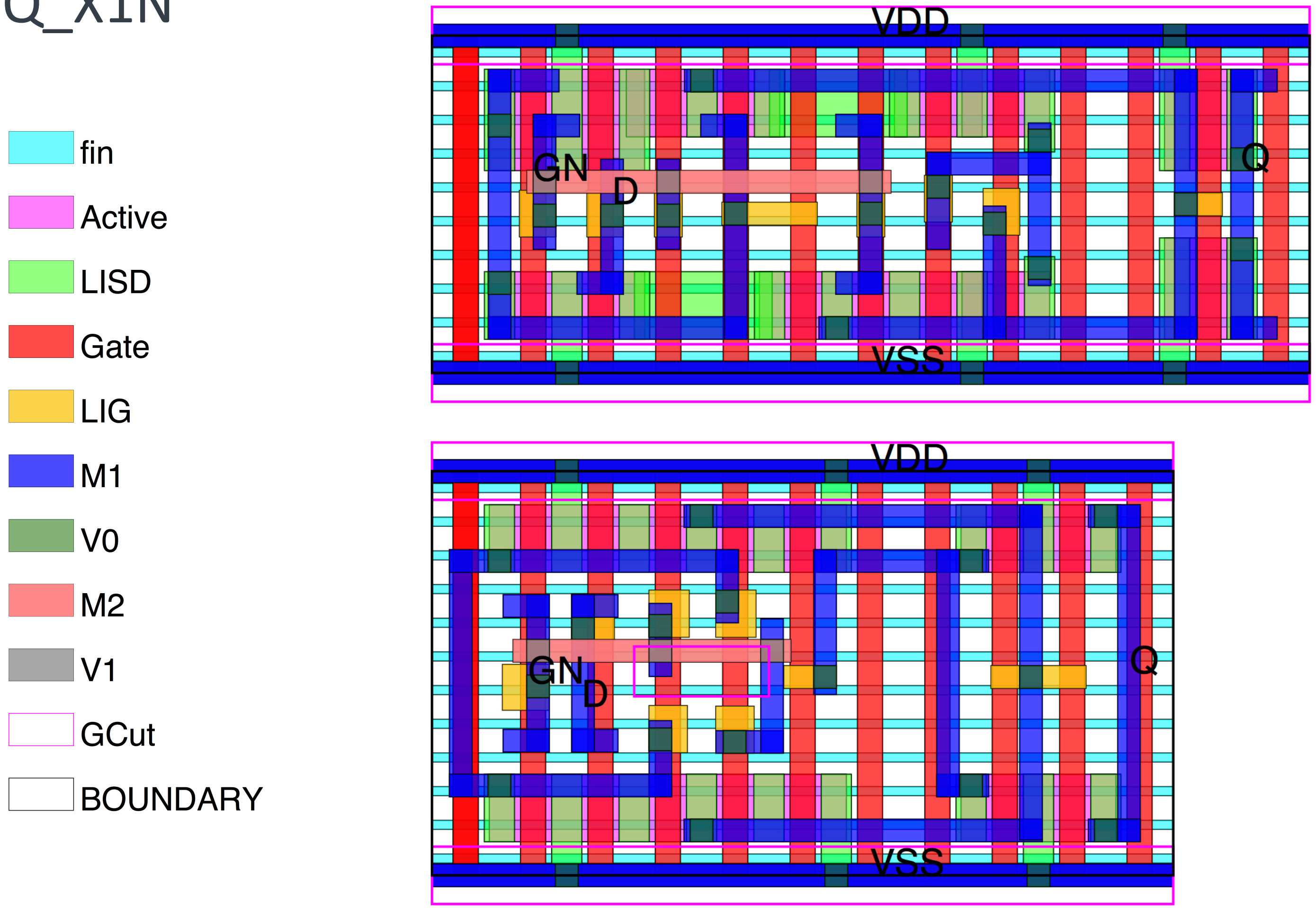
(S0,ny, 0, 0, 0, ns0,S0, B, A)

A different path

Cell Layout Comparisons



LATNQ_X1N



7.5-track: 13 poly-pitch wide

Normalized area: 97.5

Single gate diffusion

9-track:11 poly-pitch wide

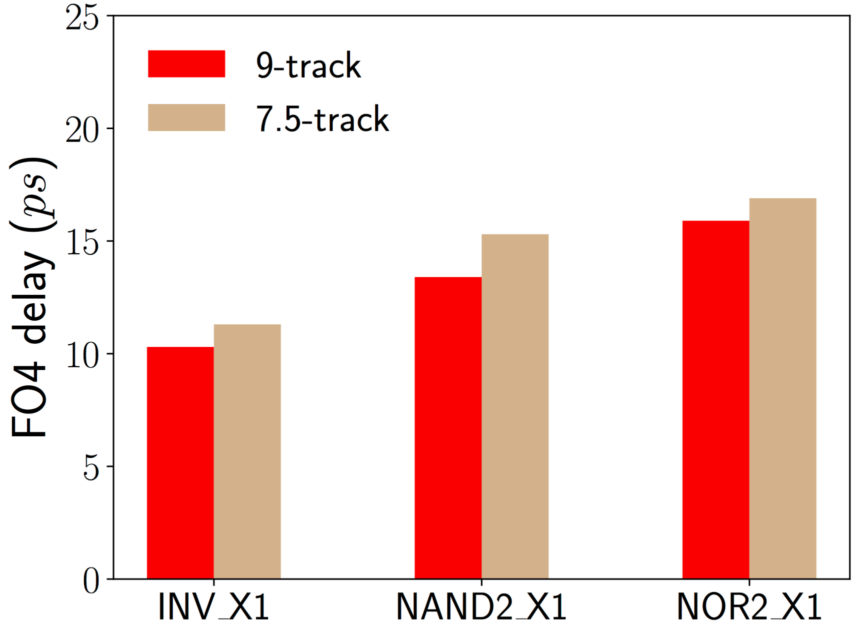
Normalized area: 99

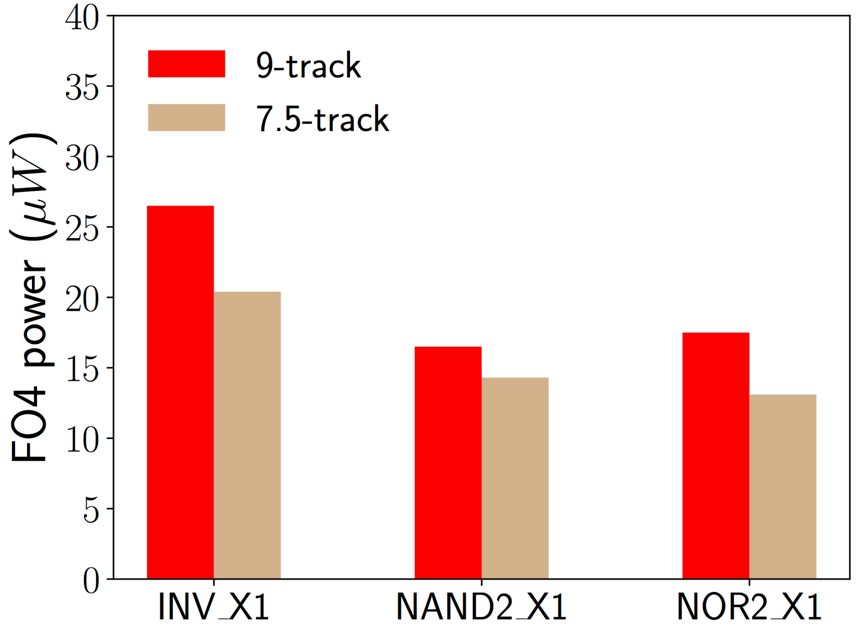
Gate cut usage

FO4 Comparisons

Fan-out-4 (FO4) for basic logic cells

- 9-track cells provide smaller delay by consuming higher power/area





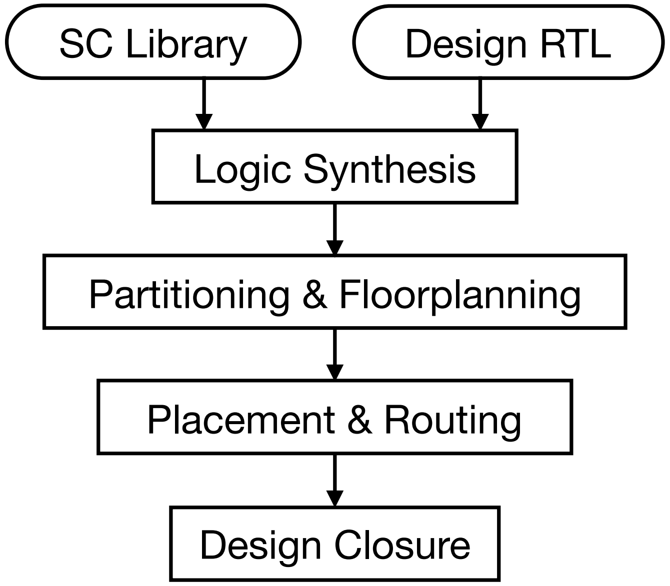
Design Synthesis and Exploration

Design Synthesis Flow

Arm® Cortex®- M0 processor from Arm DesignStart™ portal

7.5-track/9-track minimum/alpha SC library

Cadence® Genus™ Synthesis Solution, v15.12 & Innovus™ Implementation System, v15.10



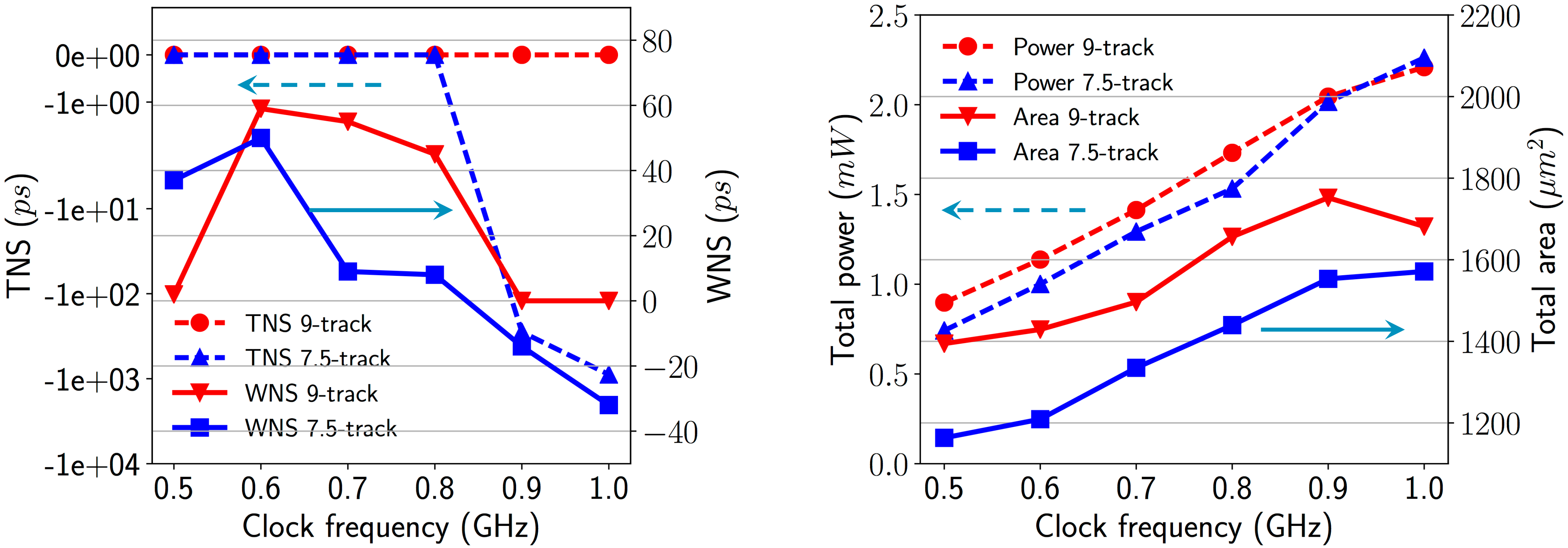
Cadence Reference Flow: up-to postrouting stage

Evaluation metrics:

- Frequency, Power, Leakage, WNS
- TNS, Utilization, gate count and area

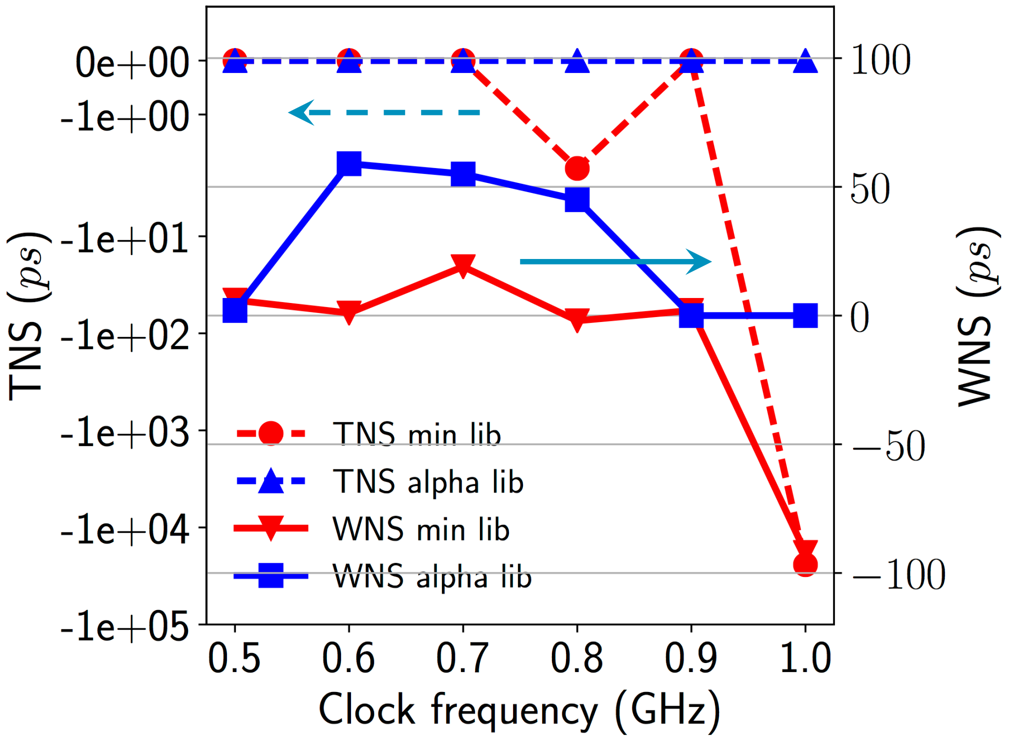
Explore Standard Cell Architecture

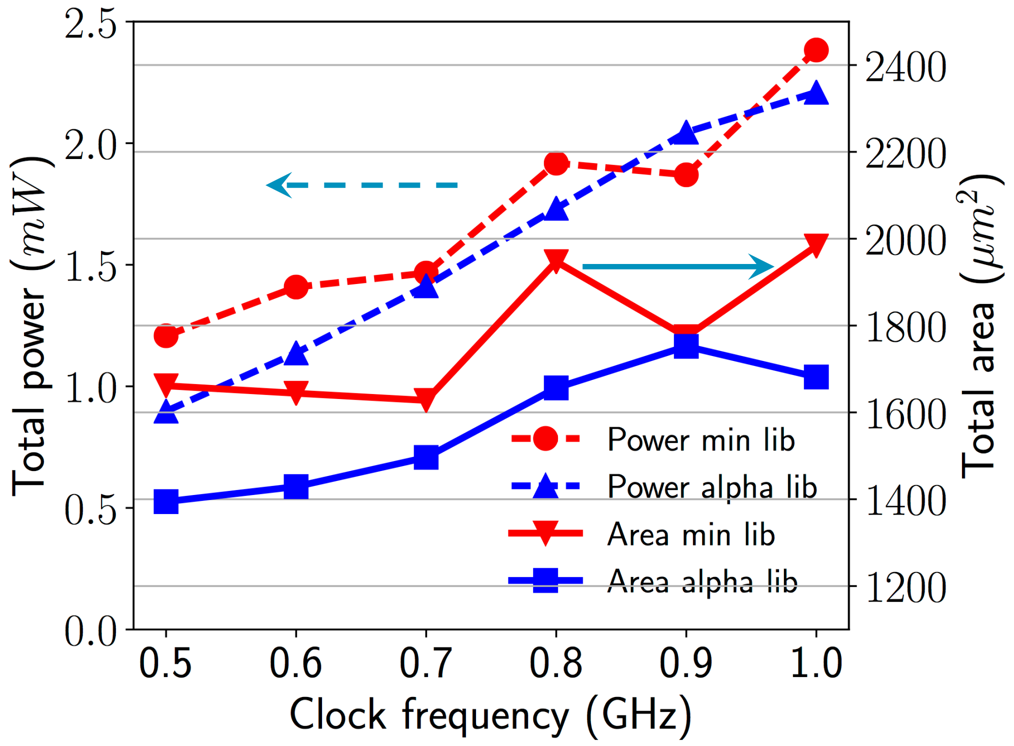
Total negative slack (TNS) and worst negative slack (WNS): 9-track lib pushes the frequency



Explore Library Richness - 9-track libraries

Total negative slack (TNS) and worst negative slack (WNS): alpha lib pushes the frequency



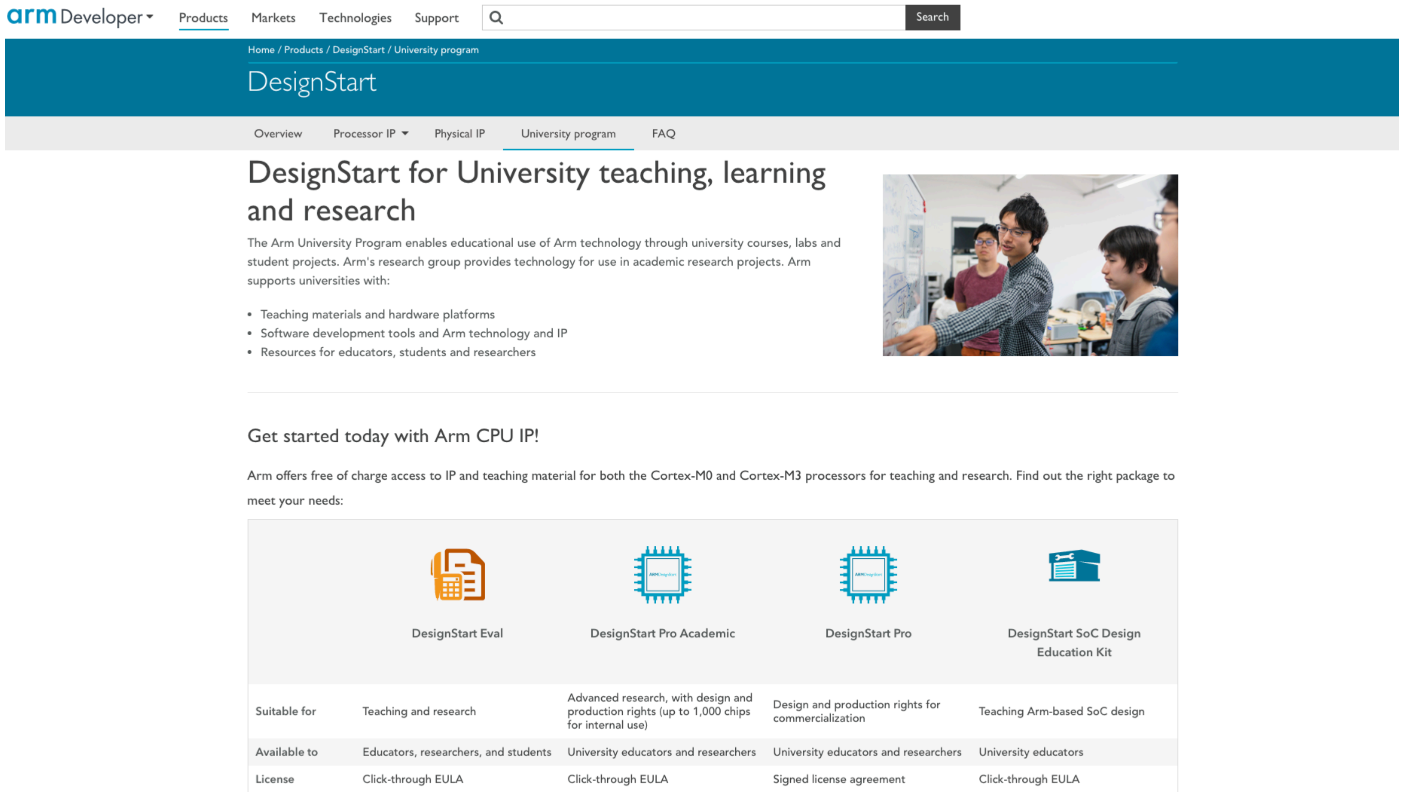


How to Download

Arm DesignStart Portal

Arm DesignStart – University Program

https://developer.arm.com/products/designstart/university-program



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DesignStart

Overview Processor IP Physical IP University program FAQ

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The Arm University Program enables educational use of Arm technology through university courses, labs and student projects. Arm's research group provides technology for use in academic research projects. Arm supports universities with:

- Teaching materials and hardware platforms
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- Resources for educators, students and researchers

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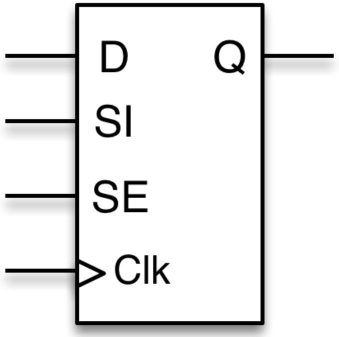
Suitable for	Teaching and research	Advanced research, with design and production rights (up to 1,000 chips for internal use)	Design and production rights for commercialization	Teaching Arm-based SoC design
Available to	Educators, researchers, and students	University educators and researchers	University educators and researchers	University educators
License	Click-through EULA	Click-through EULA	Signed license agreement	Click-through EULA

Coming soon !!!

Suggested Research Topics with the ASAP7 Standard Cell Library

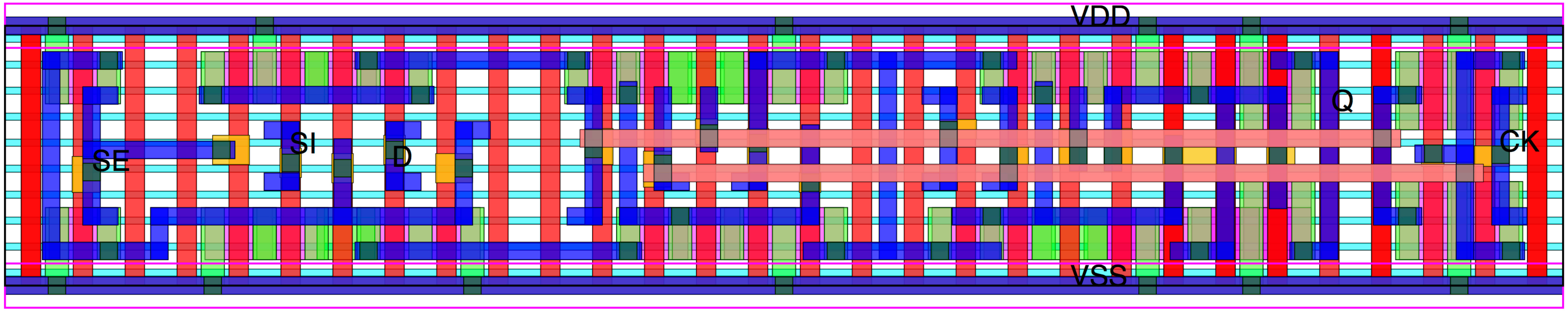
arm

Sizing with One-Fin Transistor



Current libraries are designed with minimum 2 fins per transistor

- One-fin transistor has variation concerns but benefits cell timing/power



Resize the SDFFQ_X1N with one-fin transistor

- Setup time: 11.8ps → 9.6ps (18.6%), Clock-to-Q delay: 42.1ps → 40.0ps (5%)
- Energy delay product (EDP): 8.15 → 7.13 (10^{-17} J*s) (12.5%)

Research Topics for Standard Cell Design Methodology

Transistor sizing

- How to avoid brute-force efforts for transistor sizing?
- What is the library-level advantage of enabling one-fin transistor?

Squeeze the track height

- How far can you reduce the track height?
- 5-track cells – IMEC at IEDM 2016

Multi-row height cells – design and design automation

- How to place and route transistors across multiple rows?
- What set of cells (not just flops) should be designed across multiple rows?

Broader Research Topics

Automatic Cell Synthesis

- the multigraph is not always Eulerian
- the “best” transistor placement is not always routable
- the “best” solution could be technology/architecture-dependent
- Automatic cell synthesis to beat our “alpha” quality in terms of PPA?

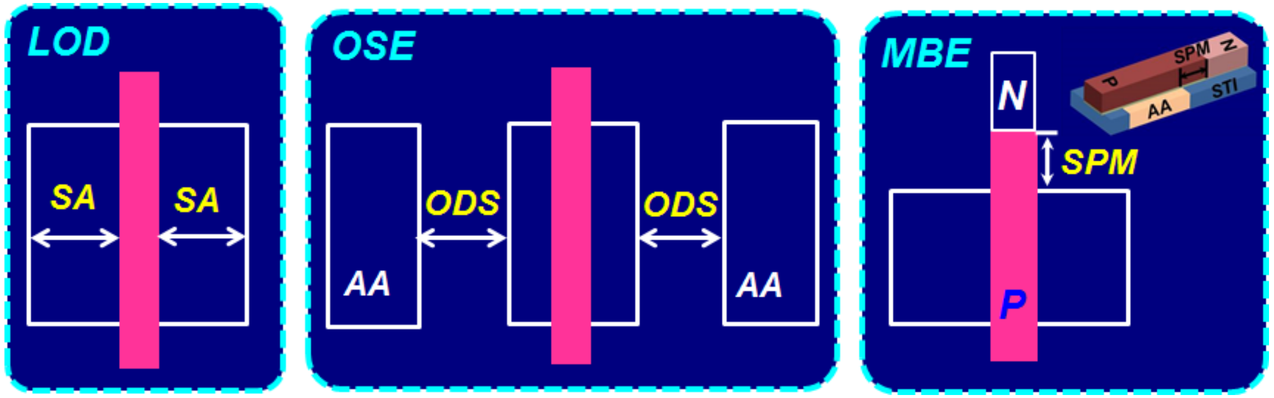
Technology-independent stick diagram generation

- placement and routing are co-optimized under lexical cost formulation
- generate more-than-one solution to break technology/architecture dependence

Design-technology co-optimization, reliability, hardware security and accelerator designs

A Successful and Published Example for Aging Research

Layout-dependent aging behaviors



[Ren+, IEDM’2015]

SA – Length between gate and edge of diffusion
ODS – Active to active spacing
SPM – Poly extension from active

SA ↓	NBTI, HCI&PBTI↑
ODS ↓	NBTI, HCI&PBTI↑
SPM ↓	NBTI ↓

Aging mitigation for critical-path timing

- Aging models w/ ASAP7 PDK - Peking University
- Aging optimization with detailed placement - UTDA
- Che-Lun Hsu et. al, “Layout-Dependent Aging Mitigation for Critical-Path Timing” at ASP-DAC 2018

Summary

Standard cell library design and optimization methodology

- Transistor sizing, placement and routing
- Front-end and back-end views built, tested and freely available for academic usages

Vt options	Track heights	PVT corners	Cell views
RVT LVT SLVT	7.5-track 9-track	ff_typical_max_0p77v_25c ff_typical_max_0p77v_m40c ss_typical_max_0p63v_125c ss_typical_max_0p63v_25c tt_typical_max_0p70v_25c	cdl, db, db-ccs-tn gds2, gds2-ascii, LEF, lib, lib-ccs-tn, spice, verilog

Summary

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Design Synthesis and Exploration

- Library architecture and richness explorations

Freq. (GHz)	SC arch.	TNS (ps)	Power (mW)	Gate area (um^2)
1.0	7.5.track	-893	2.26	1537.9
	9-track	0	2.21	1646.9
0.7	7.5-track	0	1.29	1306.9
	9-track	0	1.41	1463.5

How to Download and Use

- Arm DesignStart portal – university program
- Multiple research topics of interest and a successful/published research study ☺

Thank You!

Danke!

Merci!

谢谢!

ありがとう!

Gracias!

Kiitos!

감사합니다

धन्यवाद